avalanchetechnology
Spin Programmable Storage Solutions

High Performance Serial Persistent SRAM Memory Model Manual

Version 2.0

Table of Contents

1. Revision History

Revision No.	Date	History
1.0	09/20/2019	Initial Release
2.0	05/13/2020	Add DPI, QPI feature. Status Register Config register features

2. Overview

The zipped archive contains the model files for Avalanche High Performance Serial Persistent SRAM Memory

These models support

- Write Enable/Write disable commands in SPI (1-1-1), DPI (2-2-2) and QPI (4-4-4) modes
- Read/Write Status register in SPI (1-1-1), DPI (2-2-2) and QPI (4-4-4) modes
- Read/Write Config register in SPI (1-1-1), DPI (2-2-2) and QPI (4-4-4) modes
- Write Memory Array in SPI (1-1-1), DPI (2-2-2) and QPI (4-4-4) modes
- Read Memory Array in SPI (1-1-1), DPI (2-2-2) and QPI (4-4-4) modes
- Latency feature

3. Model Contents

The file SPSRAM_MODEL_v2.0_05132020.tar.gz once un-zipped contains the following

TOP DIRECTORY: SPSRAM_MODEL_v2.0_05132020

SUB-DIRECTORY 1: model

FILE 1: spsram_as3016206.v

SUB-DIRECTORY 2: ref

FILE 1: test.v

FILE 2: task.v

FILE 3: stimulus.v

4. Verilog Model

The file spsram_as3016286.v is located in the model directory, contains the behavioral model of 16Mb SPSRAM device. No other files are needed to instantiate and use the model.

Example below shows the instantiation of the model.

```
spsram_as3016204    M0 (
        .IO3        (IO3),
        .WPn_IO2    (WPn_IO2),
        .SO_IO1     (SO_IO1),
        .SI_IO0     (SI_IO0),
        .CSn        (CSn),
        .CLK        (CLK));
```

Table below lists the datasheet names and model pin names.

Signal	Type	Model pin name
IO3	Bidirectional	IO3
WP# / IO[2]	Bidirectional	WPn_IO2
SO / IO[1]	Bidirectional	SO_IO1
SI / IO[0]	Bidirectional	SI_IO0
CS#	input	CSn
CLK	Input	CLK

5. Commands and features supported

The table below shows the commands and mode of operations supported

	Instruction name	Command	Opcode
1	No Operation	NOP	00h
2	Write Enable	WREN	06h
3	Write Disable	WRDI	04h
4	Read Status Register	RDSR	05h
5	Read Configuration Register 1,2,3,4	RDCX	46h
6	Write Status Register	WSR	01h
7	Write Configuration Register 1,2,3,4	WCR	87h
8	Write Memory Array - SDR	WRITE	02h
9	Read Memory Array - SDR	READ	03h
10	Fast Read Memory Array - SDR	RDFT	0Bh
11	SPI Enable	SPIE	FFh
12	DPI Enable	DPIE	37h
13	QPI Enable	QPIE	38h

6. Sample Simulation

The directory ref contains sample Verilog files which can be used to run a simulation to check the functionality of the model. The descriptions of files are as below

- test.v – top level testbench which instantiates the spsram model, stimulus module
- task.v – This file contains a set of predefined tasks that can be used to create a stimulus to check various operations
- stimulus.v – Sample stimulus using tasks defined in task.v to run basic checks on the model
- run – Sample run script for cadence Verilog simulator XCELIUM

Two simulators XCELIUM (cadence) and VCS(SYNOPSYS) have been used to check the functionality of the model.

7. Timing Checks

The following datasheet timings are checked in the model. Warnings are printed if these timings are not met.

Parameter	Symbol	Type of Check
Clock Low Time	tCL	$width
Clock High Time	tCH	$width
CS# High Time	tCS3	$width
CS# Setup time (w.r.t CLK)	tCSS	$setup
CS# Hold time (w.r.t CLK)	tCSH	$hold
Data Setup Time (w.r.t CLK) - SDR	tSU	$setup
Data Hold Time (w.r.t CLK) - SDR	tHD	$hold

8. Support

Please contact us about any questions, suggestions or further requests