Space-Grade High-Performance Serial Persistent SRAM Memory

(AS1016A04, AS3016A04)

Features

- Interface
  - Serial Peripheral Interface QSPI (4-4-4)
    - Single Data Rate Mode: 54MHz
- Technology
  - 40nm pMTJ STT-MRAM
    - Virtually unlimited Endurance and Data Retention (see ***Endurance & Retention*** on page 39)
- Density
  - 16Mb
- Operating Voltage Range
  - V_{CC}: 1.71V – 2.00V
  - V_{CC}: 2.70V – 3.60V
- Operating Temperature Range
  - Industrial Extended -40°C to 125°C
- Packages
  - 8-pad WSON (5.0mm x 6.0mm)
  - 8-pin SOIC (5.2mm x 5.2mm)
- Data Protection
  - Hardware Based
    - Write Protect Pin (WP#)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect[2:0])
- Identification
  - 64-bit Unique ID
  - 64-bit User Programmable Serial Number
- Augmented Storage Array
  - 256-byte User Programmable with Write Protection
- Supports JEDEC Reset
- 48-hour burn-in at 125°C
- RoHS & REACH Compliant

Performance

Device Operation	Typical Values	Units
Frequency of Operation	54 (maximum)	MHz
Standby Current	160 (typical)	µA
Deep Power Down Current	5 (typical)	µA
Hibernate Current	0.1 (typical)	µA
Active Read Current – (4-4-4) SDR @ 54MHz	19 (typical)	mA
Active Write Current – (4-4-4) SDR @ 54MHz	38 (typical)	mA

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General Description

ASx016A04 is a magneto-resistive random-access memory (MRAM). It is offered in 16Mbit density. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with 10^{16} write cycles endurance and 1000 years data retention at 85°C.

Figure 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

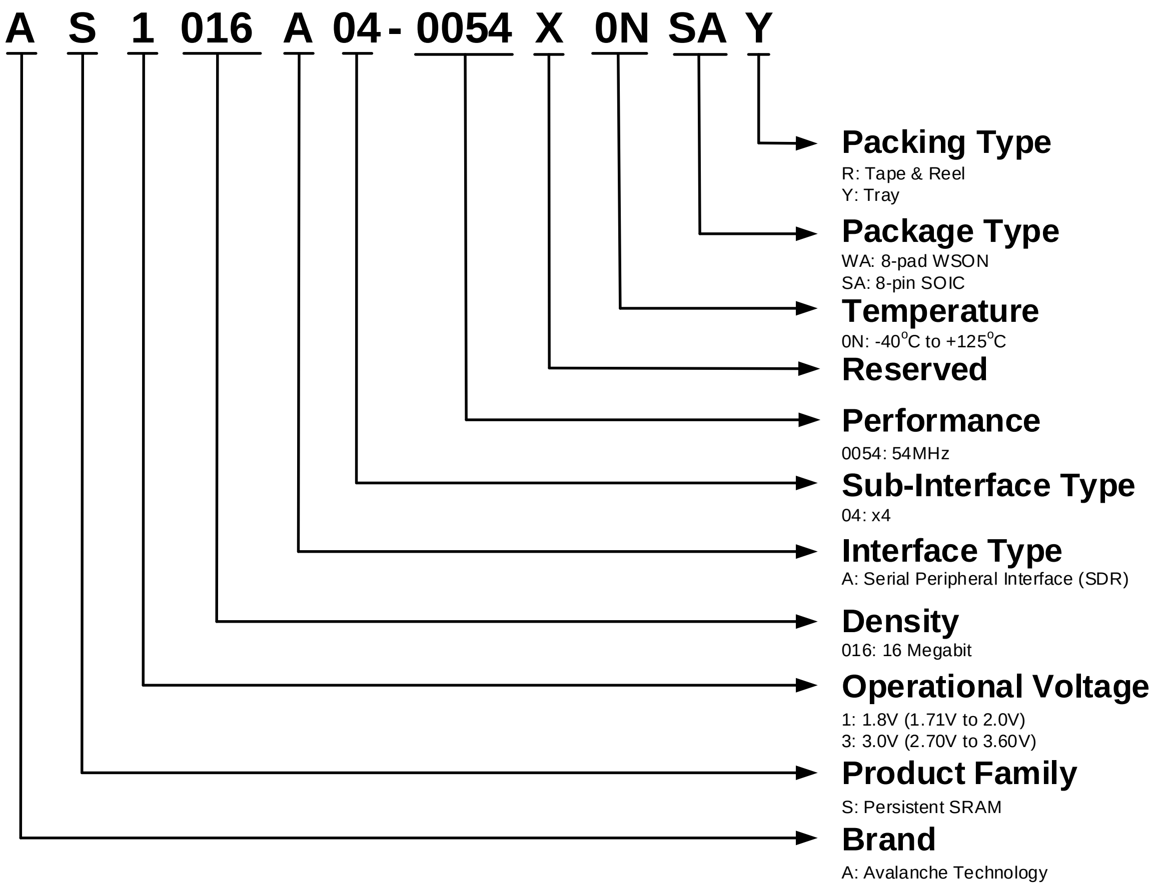
ASx016A04 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

ASx016A04 is available in small footprint 8-pad WSON and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

ASx016A04 has been tested at -40°C to 125°C operating temperature range and 48-hour burn-in at 125°C.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:



Valid Combinations — Space-Grade

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1: Valid Combinations List

Valid Combinations – 54MHz				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS1016A04-0054X	0N	WA, SA	R, Y	AS1016A04-0054X0NWAR
				AS1016A04-0054X0NWAY
				AS1016A04-0054X0NSAR
				AS1016A04-0054X0NSAY
AS3016A04-0054X	0N	WA, SA	R, Y	AS3016A04-0054X0NWAR
				AS3016A04-0054X0NWAY
				AS3016A04-0054X0NSAR
				AS3016A04-0054X0NSAY

Signal Description and Assignment

Figure 2: Device Pinout

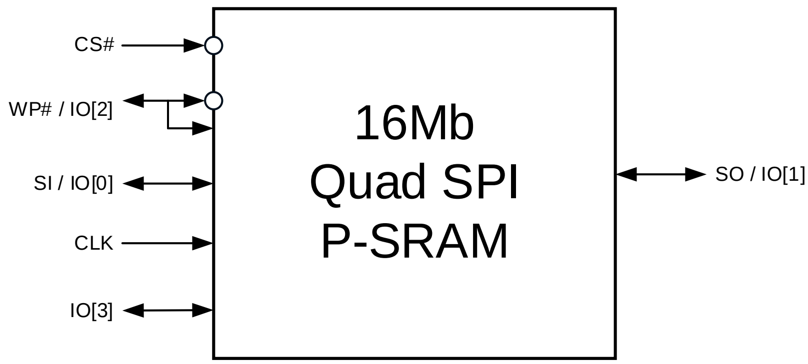


Table 2: Signal Description

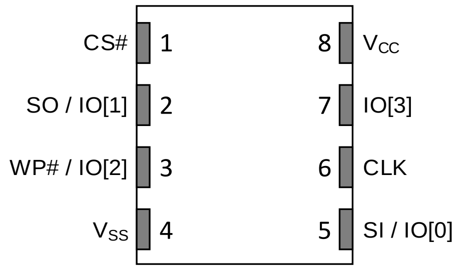
Signal	Type	Description
CS#	Input	**Chip Select:** When CS# is driven High, the device will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS# Low enables the device, placing it in the active mode. After power-up, a falling edge on CS# is required prior to the start of any instructions.
WP# / IO[2]	Input / Bidirectional	**Write Protect (SPI):** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. **Bidirectional Data 2 (DPI/QPI):** The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes.
CLK	Input	**Clock:** Provides the timing for the serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only

Signal	Type	Description
IO[3]	Bidirectional	**Bidirectional Data 3 (DPI/QPI):** The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes.
SI / IO[0]	Input / Bidirectional	**Serial Data Input (SPI):** The unidirectional I/O transfers data into the device on the rising edge of the clock in Single SPI mode. **Bidirectional Data 0 (DPI/QPI):** The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes.
SO / IO[1]	Output / Bidirectional	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of the device on the falling edge of the clock in Single SPI mode. **Bidirectional Data 1 (DPI/QPI):** The bidirectional I/O that transfers data into and out of the device in Dual and Quad SPI modes.
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.

Package Options

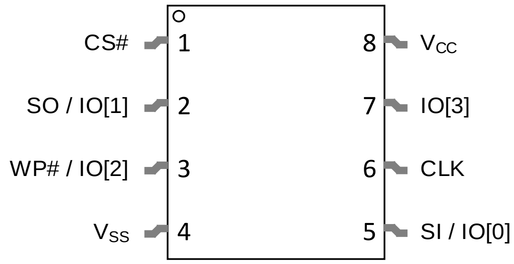
8-Pad WSON (Top View)

Figure 3: 8-Pad WSON



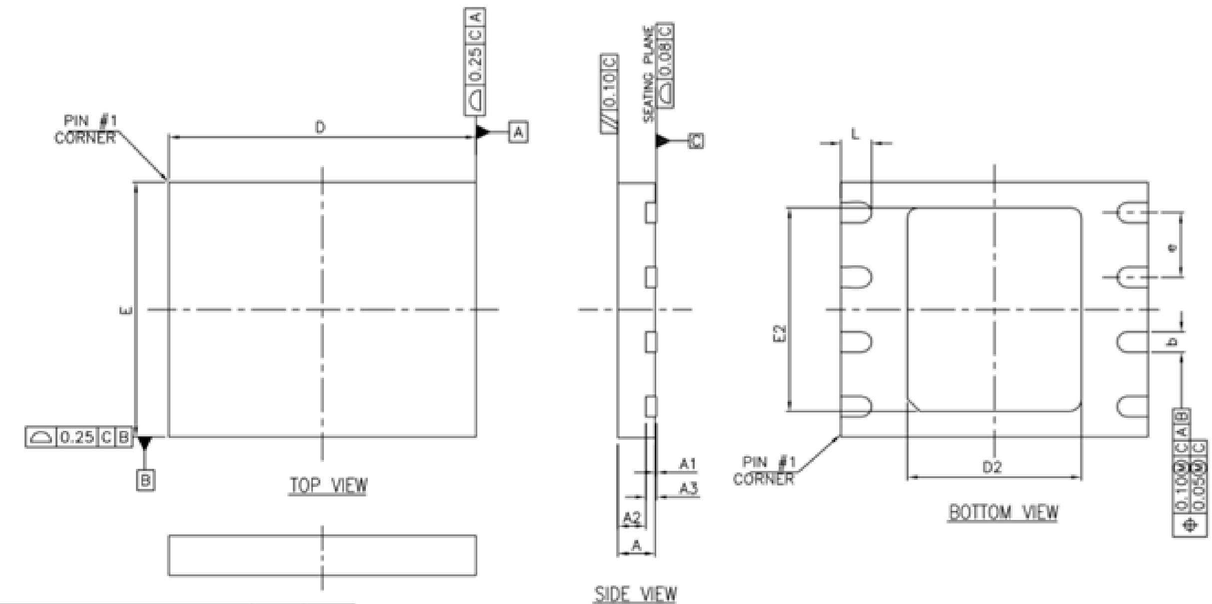
8-Pin SOIC (Top View)

Figure 4: 8-Pin SOIC



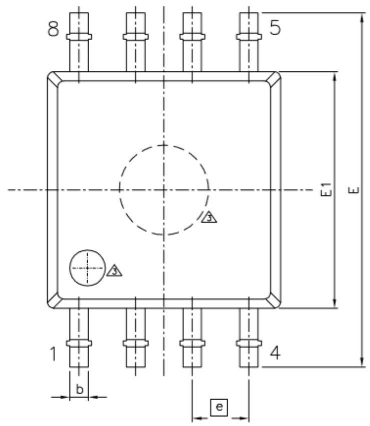
Package Drawings

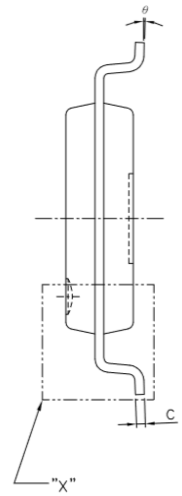
8-Pad WSON



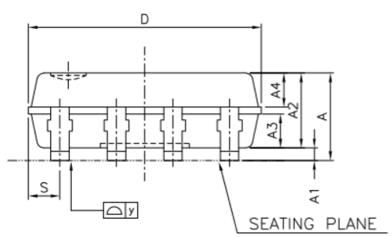
	SYMBOL	MIN.	NOM	MAX.
Total thickness	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.52	0.55	0.58
Lead thickness	A3	0.20 REF.		
Body size	D	5.90	6.00	6.10
	E	4.90	5.00	5.10
Lead width	b	0.35	0.40	0.45
Exposed pad width	D2	3.35	3.40	3.45
Exposed pad length	E2	3.95	4.00	4.05
Lead pitch	e	1.27 BSC		
Lead length	L	0.55	0.60	0.65
Lead count	N	8L		

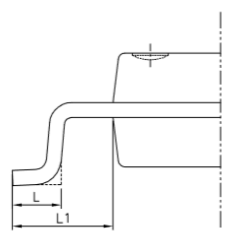
8-Pin SOIC





SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	———	———	2.16	———	———	85.04
A1	0.05	0.15	0.25	1.97	5.91	9.84
A2	1.70	1.80	1.91	66.93	70.87	75.20
A3	0.773	0.798	0.823	30.43	31.42	32.40
A4	0.773	0.798	0.823	30.43	31.42	32.40
b	0.36	0.41	0.51	14.17	16.14	20.08
C	0.19	0.20	0.25	7.48	7.87	9.84
D	5.13	5.23	5.33	201.97	205.91	209.84
E	7.70	7.90	8.10	303.15	311.02	318.90
E1	5.18	5.28	5.38	203.94	207.87	211.81
e	1.27 BSC			50 BSC		
L	0.50	0.65	0.80	19.69	25.59	31.50
L1	1.27	1.37	1.47	50.00	53.94	57.87
S	0.62	0.74	0.88	24.41	29.13	34.65
θ	0°	5°	8°	0°	5°	8°
y	———	———	0.075	———	———	2.95





DETAIL "X"

NOTE:

1. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6mil) PER SIDE.
2. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUS SHALL NOT EXCEED 0.25mm (10 mil) PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER

Architecture

ASx016A04 is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running at 54MHz, eXecute-In-Place (XIP) functionality, and hardware/software based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

ASx016A04 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. In Single SPI mode, the device is accessed via the SI / IO[0] pin. In Dual and Quad SPI modes, IO[0:1] and IO[0:3] are used to access the device respectively. ***Table 3*** summarizes all the different interface modes supported and their respective I/O usage. ***Table 4*** shows the clock edge used for each instruction component.

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 1-4-4 represents command being sent on a single I/O (SI / IO[0]) and address/data being sent on four I/Os (IO[3:0]).

Table 3: Interface Modes of Operations

Instruction Component	Single SPI (1-1-1)	Dual Input Output SPI (1-1-2)	Dual I/O SPI (1-2-2)	DPI (2-2-2)	Quad Input Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[0]	SI / IO[0]	SI / IO[0]	IO[1:0]	SI / IO[0]	SI / IO[0]	IO[3:0]
Address	SI / IO[0]	SI / IO[0]	IO[1:0]	IO[1:0]	SI / IO[0]	IO[3:0]	IO[3:0]
Data Input	SI / IO[0]	IO[1:0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[3:0]
Data Output	SO / IO[1]	IO[1:0]	IO[1:0]	IO[1:0]	IO[3:0]	IO[3:0]	IO[3:0]

Table 4: Clock Edge Used for instructions in SDR and DDR modes

Instruction Type	Command	Address	Data Input	Data Output
(1-1-1) SDR	R	R	R	F [1]
(1-1-2) SDR	R	R	R	F [1]
(1-2-2) SDR	R	R	R	F [1]
(2-2-2) SDR	R	R	R	F [1]
(1-1-4) SDR	R	R	R	F [1]
(1-4-4) SDR	R	R	R	F [1]
(4-4-4) SDR	R	R	R	F [1]

Notes:
R: Rising Clock Edge
F: Falling Clock Edge

1: Data output from ASx016A04 always begins on the falling edge of the clock.

ASx016A04 supports eXecute-In-Place (XIP) which allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. Thus, XIP mode saves command overhead and reduces random read & write access time. A special XIP byte must be entered after the address bits to enable/disable (Axh/Fxh) XIP.

ASx016A04 offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

ASx016A04 has a 256-byte Augmented Storage Array which is independent from the main memory array. It is user programmable and can be write protected against inadvertent writes.

Two lower power states are available in ASx016A04, namely Deep Power Down and Hibernate. Data is not lost while the device is in either of these two low power states. Moreover, the device maintains all its configurations.

Figure 5: Functional Block Diagram

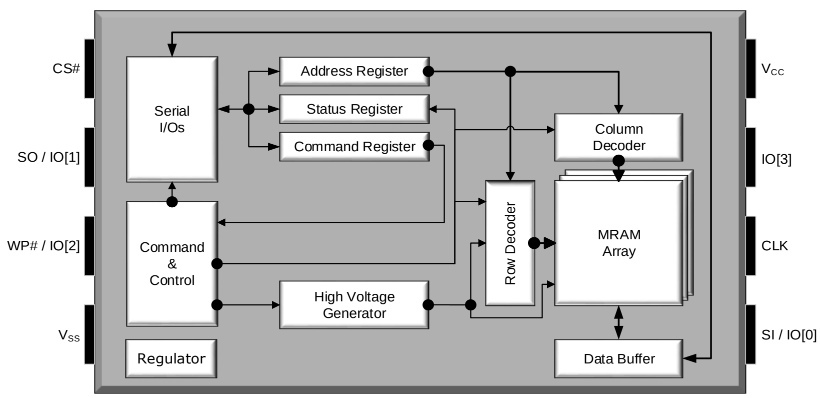


Table 5: Modes of Operation

Mode	Current	CS#	CLK	SI / IO[3:0]	SO / IO[3:0]
Standby	I_{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I_{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I_{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z
Deep Power Down	I_{DPD}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Hibernate	I_{HBN}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z

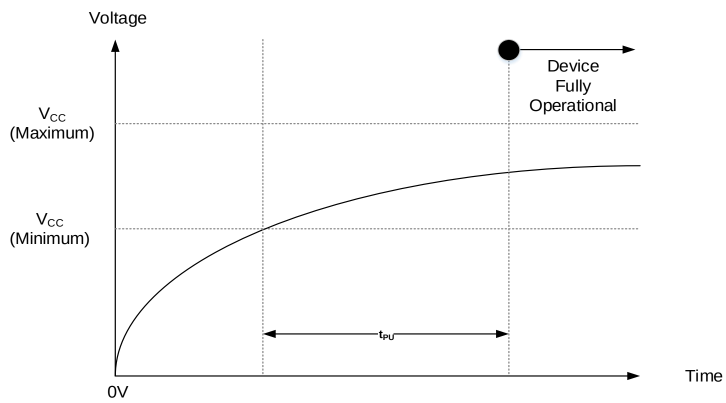
Notes:
H: High (Logic '1')
L: Low (Logic '0')
Hi-Z: High Impedance

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp up V_{CC} (R_{VR})
- CS# must follow V_{CC} during power-up (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- During initial power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences
- Upon Power-up, the device is in Standby mode

Figure 6: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- Ramp down V_{CC} (R_{VF})
- CS# must follow V_{CC} during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- The Power-up timing needs to be observed after V_{CC} goes above V_{CC} (minimum)

Figure 7: Power-Down Behavior

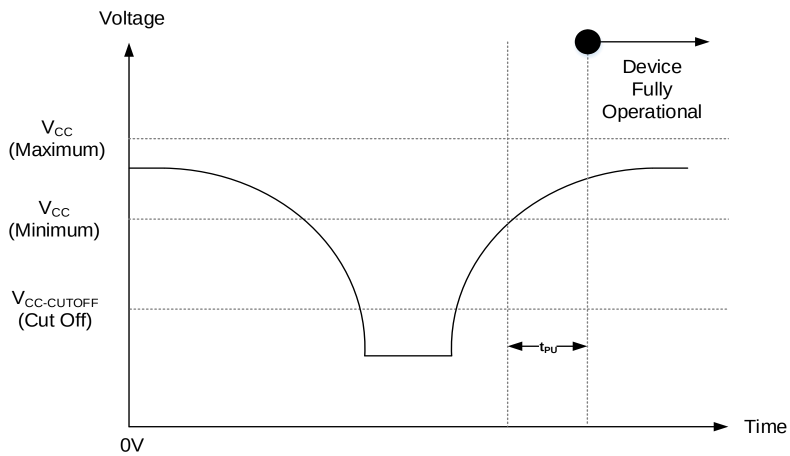


Table 6: Power Up/Down & Voltage Timing – 3.0V

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range	V_{CC}	All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		250	-	-	µs
V_{CC} Cutoff – Must Initialize Device	$V_{CC-CUTOFF}$		1.6	-	-	V
Time to Enter Deep Power Down	t_{EDPD}		-	-	3	µs
Time to Exit Deep Power Down	t_{EXDPD}		-	-	400	µs
Time to Enter Hibernate	t_{ENTHIB}		-	-	3	µs
Time to Exit Hibernate	t_{EXHIB}		-	-	450	µs
CS# Pulse Width	t_{CSDPD}		50	-	-	ns

Table 7: Power Up/Down & Voltage Timing – 1.8V

Parameter	Symbol	Test Conditions	1.8V			
			Minimum	Typical	Maximum	Units
V_{CC} Range	V_{CC}	All operating voltages and temperatures	1.71	-	2.0	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		250	-	-	µs
V_{CC} Cutoff – Must Initialize Device	$V_{CC-CUTOFF}$		1.6	-	-	V
Time to Enter Deep Power Down	t_{EDPD}		-	-	3	µs
Time to Exit Deep Power Down	t_{EXDPD}		-	-	400	µs
Time to Enter Hibernate	t_{ENTHIB}		-	-	3	µs
Time to Exit Hibernate	t_{EXHIB}		-	-	450	µs
CS# Pulse Width	t_{CSDPD}		50	-	-	ns

Memory Map

Table 8: Memory Map

Density	Address Range	24-bit Address [23:0]	
1Mb	000000h – 01FFFFh	[23:17] – Logic '0'	[16:0] - Addressable
4Mb	000000h – 07FFFFh	[23:19] – Logic '0'	[18:0] - Addressable
8Mb	000000h – 0FFFFFh	[23:20] – Logic '0'	[19:0] - Addressable
16Mb	000000h – 1FFFFFh	[23:21] – Logic '0'	[20:0] - Addressable

Augmented Storage Array Map

Table 9: Augmented Storage Array Map

Density	Address Range	24-bit Address [23:0]	
1Mb	000000h – 0000FFh [1]	[23:8] – Logic '0'	[7:0] - Addressable
4Mb	000000h – 0000FFh [1]	[23:8] – Logic '0'	[7:0] - Addressable
8Mb	000000h – 0000FFh [1]	[23:8] – Logic '0'	[7:0] - Addressable
16Mb	000000h – 0000FFh [1]	[23:8] – Logic '0'	[7:0] - Addressable

Notes:
1: The 256-byte augmented storage array is divided into 8 individually readable and writeable sections (32 bytes per section). After an individual section is programmed, it can be write protected to prevent further programming.

Table 10: Individual Section Address Range

Section	Address Range	24-bit Address [23:0]	
0	000000h – 00001Fh	[23:8] – Logic '0'	[7:0] - Addressable
1	000020h – 00003Fh	[23:8] – Logic '0'	[7:0] - Addressable
2	000040h – 00005Fh	[23:8] – Logic '0'	[7:0] - Addressable
3	000060h – 00007Fh	[23:8] – Logic '0'	[7:0] - Addressable
4	000080h – 00009Fh	[23:8] – Logic '0'	[7:0] - Addressable
5	0000A0h – 0000BFh	[23:8] – Logic '0'	[7:0] - Addressable
6	0000C0h – 0000DFh	[23:8] – Logic '0'	[7:0] - Addressable
7	0000E0h – 0000FFh	[23:8] – Logic '0'	[7:0] - Addressable

Register Addresses

Table 11: Register Addresses

Register Name	Address
Status Register	0x000000h
Configuration Register 1	0x000002h
Configuration Register 2	0x000003h
Configuration Register 3	0x000004h
Configuration Register 4	0x000005h
Device Identification Register	0x000030h
Unique Identification Register	0x000040h

Notes:

1: Register address space is different from the memory array and augmented storage array.

2: The Status and Configuration registers need to be re-initialized after a solder reflow process. Refer to application note AN000008 for the detailed description.

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

Table 12: Status Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	SNPEN	Serial Number Protection Enable/Disable	R/W	0	1: S/N Write protected - protection enabled 0: S/N Writable - protection disabled
SR[5]	TBSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits (Table 13, ***Table 14***)
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Protection Enable/Disable	R	0	1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Table 13: Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb
0	**0**	**0**	None	None	None	None	None
0	**0**	**1**	Upper 1/64	01F800h – 01FFFFh	07E000h – 07FFFFh	0FC000h – 0FFFFFh	1F8000h – 1FFFFFh
0	**1**	**0**	Upper 1/32	01F000h – 01FFFFh	07C000h – 07FFFFh	0F8000h – 0FFFFFh	1F0000h – 1FFFFFh
0	**1**	**1**	Upper 1/16	01E000h – 01FFFFh	078000h – 07FFFFh	0F0000h – 0FFFFFh	1E0000h – 1FFFFFh
1	**0**	**0**	Upper 1/8	01C000h – 01FFFFh	070000h – 07FFFFh	0E0000h – 0FFFFFh	1C0000h – 1FFFFFh
1	**0**	**1**	Upper 1/4	018000h – 01FFFFh	060000h – 07FFFFh	0C0000h – 0FFFFFh	180000h – 1FFFFFh
1	**1**	**0**	Upper 1/2	010000h – 01FFFFh	040000h – 07FFFFh	080000h – 0FFFFFh	1F0000h – 1FFFFFh
1	**1**	**1**	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh

Table 14: Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb
0	0	0	None	None	None	None	None
0	0	1	Lower 1/64	000000h – 0007FFFh	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh
0	1	0	Lower 1/32	000000h – 00FFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh
0	1	1	Lower 1/16	000000h – 001FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh
1	0	0	Lower 1/8	000000h – 003FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh
1	0	1	Lower 1/4	000000h – 007FFFh	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh
1	1	0	Lower 1/2	000000h – 00FFFFh	000000h – 03FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh
1	1	1	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh

Table 15: Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status & Configuration Registers	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	Low	Protected	Protected	Unprotected
1	1	High	Unprotected	Protected	Unprotected

Notes:
High: Logic ‘1’
Low: Logic ‘0’
X: Don’t Care – Can be Logic ‘0’ or ‘1’
Protected: Write protected
Unprotected: Writable
1: Memory address range protection based on Block Protection Bits

Augmented Storage Array Protection Register (Read/Write)

Augmented Storage Array Protection register contains options for enabling/disabling data protection for eight 32-byte sections.

Table 16: Augmented Storage Array Protection Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
ASP[7]	ASPS[7]	ASA Section 7 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[6]	ASPS[6]	ASA Section 6 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[5]	ASPS[5]	ASA Section 5 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[4]	ASPS[4]	ASA Section 4 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[3]	ASPS[3]	ASA Section 3 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[2]	ASPS[2]	ASA Section 2 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[1]	ASPS[1]	ASA Section 1 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled
ASP[0]	ASPS[0]	ASA Section 0 Write Protection Enable/Disable	R/W	0	1: Protection Enabled 0: Protection Disabled

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 17: Device Identification Register – Read Only

Bits	Avalanche Manufacturer's ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temp	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0000-HP QSPI	0001 - 3V	0010 - -40ºC-125ºC	0101 - 16Mb	00000010 - 54MHz
		0010 - 1.8V			

Serial Number Register (Read/Write)

Serial Number register is user writable.

Table 18: Serial Number Register – Read and Write

Bits	Name	Description	Read / Write	Default State [1]	Selection Options
SN[63:0]	SN	Serial Number Value	R/W	0000000000000000h	Value stored is based on the customer

Notes:
1: The default value is how the device is shipped from the factory.

Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 19: Unique ID Register – Read Only

Bits	Name	Description	Read / Write	Selection Options
UID[63:0]	UID	Unique Identification Number Value	R	Value stored is written in the factory and is device specific

Configuration Register 1 (Read/Write)

Configuration Register 1 controls locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register.

Table 20: Configuration Register 1 – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR1[7]	RSVD	Reserved	R	0	Reserved for future use
CR1[6]	RSVD	Reserved	R	0	Reserved for future use
CR1[5]	RSVD	Reserved	R	0	Reserved for future use
CR1[4]	RSVD	Reserved	R	0	Reserved for future use
CR1[3]	RSVD	Reserved	R	0	Reserved for future use
CR1[2]	MAPLK	Status Register Lock Enable/Disable (TBSEL, BPSEL[2:0]	R/W	0	1: Lock TBSEL and BPSEL[2:0] 0: Unlock TBSEL and BPSEL[2:0]
CR1[1]	RSVD	Reserved	R	0	Reserved for future use
CR1[0]	ASPLK	Augmented Storage Array Data Protection	R/W	0	1: Write Protect Augmented Storage Array 0: Not Write Protect Augmented Storage Array

Configuration Register 2 (Read/Write)

Configuration Register 2 controls the interface type along with memory array access latency.

Table 21: Configuration Register 2 – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR2[7]	RSVD	Reserved	R	0	Reserved for future use
CR2[6]	QPISL	Quad SPI (QPI 4-4-4) Interface Mode Enable/Disable	R[2]	0	1: Quad SPI (QPI 4-4-4) Enabled 0: Single SPI (SPI 1-1-1) Enabled
CR2[5]	RSVD	Reserved	R	0	Reserved for future use
CR2[4]	DPISL	Dual SPI (DPI 2-2-2) Interface Mode Enable/Disable	R[2]	0	1: Dual SPI (DPI 2-2-2) Enabled 0: Single SPI (SPI 1-1-1) Enabled
CR2[3]	MLATS[3]	Memory Array Read Latency Selection [1]	R/W	0	0000: 0 Cycles - Default 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles
CR2[2]	MLATS[2]			0	

Bits	Name	Description	Read / Write	Default State	Selection Options
CR2[1]	MLATS[1]			0	0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycle 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[0]	MLATS[0]			0	

Notes:
1: Latency is frequency dependent. Please consult ***Table 22*** and ***Table 23***.
2: These interface options can only be set through instructions.

Table 22: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

Read Type	Latency	Max Frequency ASxxxx2x054xx
(1-1-1) SDR	8-15	54MHz
(1-1-2) SDR		54MHz
(1-2-2) SDR		54MHz
(2-2-2) SDR		54MHz
(1-1-4) SDR	12-15	54MHz
(1-4-4) SDR		54MHz
(4-4-4) SDR		54MHz

Table 23: Memory Read Latency Cycles vs. Maximum Clock Frequency (without XIP)

Read Type	Latency	Max Frequency ASxxxx2x054xx
(1-1-1) SDR	8-15	54MHz
(2-2-2) SDR	8-15	54MHz
(4-4-4) SDR	8-15	54MHz

Table 24: Augmented Storage Array Read Latency Cycles vs. Maximum Clock Frequency

Read Type	Latency	Max Frequency ASxxxx2x054xx
(1-1-1) SDR	8-15	40MHz

Table 25: Read Any Register Command Latency Cycles vs. Maximum Clock Frequency

Read Type	Max Frequency	Latency Cycles
(1-1-1) SDR	54MHz	8
(2-2-2) SDR	54MHz	4
(4-4-4) SDR	54MHz	2

Configuration Register 3 (Read/Write)

Configuration Register 3 controls the output driver strength along with read data wrap selection.

Table 26: Configuration Register 3 – Read and Write

Bits	Name	Description	Read / Write	Default 1.8V	Default 3.0V	Selection Options
CR3[7]	ODSEL[2]	Output Driver Strength Selector	R/W	0	0	1.8V 3.0V 000: 45Ω[1] 35Ω 001: 120Ω 75Ω 010: 90Ω 60Ω 011: 70Ω 45Ω[1] 100: 45Ω 35Ω 101: 60Ω 40Ω 110: 30Ω 20Ω 111: 20Ω 15Ω
CR3[6]	ODSEL[1]			0	1	
CR3[5]	ODSEL[0]			0	1	
CR3[4]	WRAPS	Read WRAP Enable / Disable (16/32/64/128/256 Byte)	R/W	0		1: Read Data Wrap Enabled 0: Read Data Wrap Disabled
CR3[3]	RSVD	Reserved	R	0		Reserved for future use
CR3[2]	WRPLS[2]	Wrap Length Selector[2]	R/W	0		000: 16-byte Boundary 001: 32-byte Boundary 010: 64-byte Boundary 011: 128-byte Boundary 100: 256-byte Boundary 101: Reserved 110: Reserved 111: Reserved
CR3[1]	WRPLS[1]			0		
CR3[0]	WRPLS[0]			0		

Notes:
1: Default Setting (V_{CC} dependent).
2: If Wrap is enabled, the read data wraps within an aligned 16/32/64/128/256-byte boundary at any address. The starting address entered selects the group of bytes and the first data returned is the addressed byte. Bytes are then read sequentially until the end of the group boundary is reached. If read continues, the address wraps to the beginning of the group and continues to read sequentially.

Configuration Register 4 (Read/Write)

Configuration Register 4 controls Write Enable protection (WREN – Status Register) reset functionality during memory array writing[1]. This functionality makes SPI MRAM compatible to other SPI devices.

Table 27: Configuration Register 4 – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR4[7]	RSVD	Reserved	R/W	0	Reserved for future use
CR4[6]	RSVD	Reserved		0	Reserved for future use
CR4[5]	RSVD	Reserved		0	Reserved for future use
CR4[4]	RSVD	Reserved		0	Reserved for future use
CR4[3]	RSVD	Reserved		0	Reserved for future use
CR4[2]	RSVD	Reserved		1	Reserved[2]
CR4[1]	WRENS[1]	WREN Reset Selector (Memory & Augmented Storage Array Write Functionality)		0	00: Normal: WREN is prerequisite to all Memory Array Write instruction. (WREN is reset after CS# goes High) 01: SRAM: WREN is not a prerequisite to Memory Array Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset once CS# goes High) 11: Illegal - Reserved for future use
CR4[0]	WRENS[0]			1	

Notes:

1: Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 4 settings. In other words, all register write instructions require WREN to be set and WREN resets once CS# goes High for the write instruction.

2: Must be set to “1”. Writing a “0” to this bit may impact device functionality.

Instruction Set

Table 28: Instruction Set

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-2)	(1-2-2)	(2-0-0)	(2-0-2)	(2-2-2)	(1-1-4)	(1-4-4)	(4-0-0)	(4-0-4)	(4-4-4)	XIP	SDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite
1	**No Operation**	NOOP 00h	•					•					•				•			54 MHz	
2	**Write Enable**	WREN 06h	•					•					•				•			54 MHz	
3	**Write Disable**	WRDI 04h	•					•					•				•			54 MHz	
4	**Enable DPI**	DPIE 37h	•										•				•			54 MHz	
5	**Enable QPI**	QPIE 38h	•					•									•			54 MHz	
6	**Enable SPI**	SPIE FFh						•					•				•			54 MHz	
7	**Enter Deep Power Down**	DPDE B9h	•					•					•				•			54 MHz	
8	**Enter Hibernate**	HBNE BAh	•					•					•				•			54 MHz	
9	**Software Reset Enable**	SRTE 66h	•					•					•				•			54 MHz	
10	**Software Reset**	SRST 99h	•					•					•				•			54 MHz	SRTE
11	**Exit Deep Power Down**	DPDX ABh	•					•					•				•			54[7] MHz	
12	**Read Status Register**	RDSR 05h		•					•					•			•		1	54 MHz	

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-2)	(1-2-2)	(2-0-0)	(2-0-2)	(2-2-2)	(1-1-4)	(1-4-4)	(4-0-0)	(4-0-4)	(4-4-4)	XIP	SDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite
13	**Read Configuration Register 1**	RDC1 35h		•					•					•			•		1	54 MHz	
14	**Read Configuration Register 2**	RDC2 3Fh		•					•					•			•		1	54 MHz	
15	**Read Configuration Register 3**	RDC3 44h		•					•					•			•		1	54 MHz	
16	**Read Configuration Register 4**	RDC4 45h		•					•					•			•		1	54 MHz	
17	**Read Configuration Register 1, 2, 3, 4**	RDCX 46h		•					•					•			•		4	54 MHz	
18	**Read Device ID**	RDID 9Fh		•					•					•			•		4	54 MHz	
19	**Read Unique ID**	RUID 4Ch		•					•					•			•		8	54 MHz	
20	**Read Serial Number Register**	RDSN C3h		•					•					•			•		8	54 MHz	
21	**Read Augmented Array Protection Register**	RDAP 14h		•					•					•			•		1	54 MHz	
22	**Read Any Register - Address Based**	RDAR 65h			•					•					•		•	•	1 to 8	54 MHz	
23	**Write Status Register**	WRSR 01h		•					•					•			•		1	54 MHz	WREN
24	**Write Configuration Registers 1, 2, 3, 4**	WRCX 87h		•					•					•			•		4	54 MHz	WREN
25	**Write Serial Number Register**	WRSN C2h		•					•					•			•		8	54 MHz	WREN

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-2)	(1-2-2)	(2-0-0)	(2-0-2)	(2-2-2)	(1-1-4)	(1-4-4)	(4-0-0)	(4-0-4)	(4-4-4)	XIP	SDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite
26	**Write Augmented Array Protection Register**	WRAP 1Ah		•					•					•			•		1	54 MHz	WREN
27	**Write Any Register - Address Based**	WRAR 71h			•					•					•		•		1 to 8	54 MHz	WREN
28	**Read Memory Array - SDR**	READ 03h			•												•		1 to ∞	50 MHz	
29	**Fast Read Memory Array - SDR**	RDFT 0Bh			•					•					•	•	•	•	1 to ∞	54 MHz	
30	**Read Dual Output Memory Array - SDR**	RDDO 3Bh				•										•	•	•	1 to ∞	54 MHz	
31	**Read Quad Output Memory Array - SDR**	RDQO 6Bh									•					•	•	•	1 to ∞	54 MHz	
32	**Read Dual I/O Memory Read - SDR**	RDDI BBh					•									•	•	•	1 to ∞	54 MHz	
33	**Read Quad I/O Memory Read - SDR**	RDQI EBh										•				•	•	•	1 to ∞	54 MHz	
34	**Write Memory Array - SDR**	WRTE 02h			•												•		1 to ∞	54 MHz	WREN
35	**Fast Write Memory Array - SDR**	WRFT DAh			•					•					•	•	•		1 to ∞	54 MHz	WREN
36	**Write Dual Input Memory Array - SDR**	WDUI A2h				•										•	•		1 to ∞	54 MHz	WREN
37	**Write Quad Input Memory Array - SDR**	WQDI 32h									•					•	•		1 to ∞	54 MHz	WREN
38	**Write Dual I/O Memory Array - SDR**	WDIO A1h					•									•	•		1 to ∞	54 MHz	WREN

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-2)	(1-2-2)	(2-0-0)	(2-0-2)	(2-2-2)	(1-1-4)	(1-4-4)	(4-0-0)	(4-0-4)	(4-4-4)	XIP	SDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite
39	**Write Quad I/O Memory Array - SDR**	WQIO D2h										•				•	•		1 to ∞	54 MHz	WREN
40	**Read Augmented Storage Array - SDR**	RDAS 4Bh			•												•	•	1 to 256	50 MHz	
41	**Write Augmented Storage Array - SDR**	WRAS 42h			•												•		1 to 256	54 MHz	WREN

Notes:

1: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 1-4-4 represents command being sent on a single I/O (SI / IO[0]) and address/data being sent on four I/Os (IO[3:0]).

2: XIP allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. A special mode byte must be entered after the address bits to enable/disable XIP – Axh / Fxh.

3: Read instruction must include Latency cycles to meet higher frequency. They are configurable (Configuration Register 2 – CR2[3:0]) and frequency dependent.

4: The augmented storage array is 256-Bytes in size. The address bits ADDR[23:8] must be Logic '0' for this instruction.

5: Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

6: WREN prerequisite for array writing is configurable (Configuration Register 4 – CR4[1:0]).

7: For the Exit Deep Power Down command, the maximum frequency is 54MHz for 1-1-1 operation and 36MHz for 2-2-2 and 4-4-4 operations.

Instruction Description and Structures

All communication between a host and ASx016A04 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from ASx016A04. All command, address and data information is transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic'1').
- CLK marks the transfer of each bit.
- Each instructions starts out with an 8-bit command. The command selects the type of operation ASx016A04 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location or register. The address is always 24-bits wide.
- The address bits are followed by data bits.
- In normal operational mode, Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction. ASx016A04 offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array or the augmented storage array. These modes are set in Configuration Register 4.
- ASx016A04 is a high performance serial memory and at higher frequencies, read instructions require latency cycles to compensate for the memory array access time. The number of latency cycles required depends on the operational frequency and is configurable – Configuration Register 2. The latency cycles are inserted after the address bits before the data comes out of ASx016A04.
- For Read and Write instructions, ASx016A04 offers XIP mode. XIP allows similar instructions to be executed sequentially without incurring the command cycles overhead. XIP is enabled by entering byte Axh and disabled by entering byte Fxh. These respective bytes must be entered following the address bits.
- For Read instructions, ASx016A04 offers wrap mode. Wrap bursts are confined to address aligned 16/32/64/128/256 byte boundary. The read address can start anywhere within the wrap boundary. 16/32/64/128/256 wrap configuration is set in Configuration Register 3.
- The entire memory array can be read from or written to using a single read or write instruction. After the staring address is entered, subsequent address are internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.

Figure 8 to **Figure 24** show the description of SDR instruction types supported.

Figure 8: Description of (1-0-0) Instruction Type

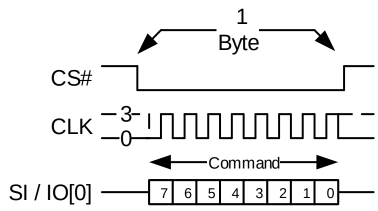


Figure 9: Description of (1-0-1) Instruction Type

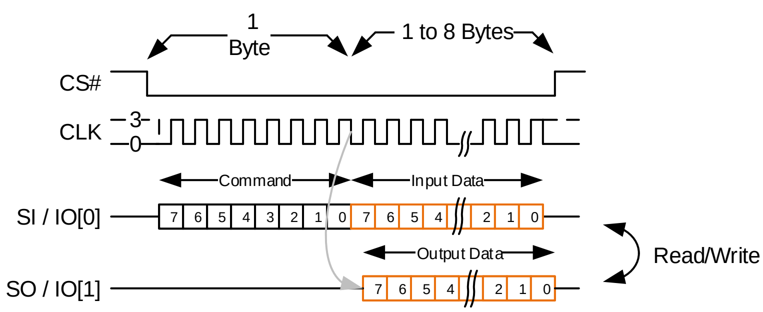


Figure 10: Description of (1-1-1) Instruction Type (Without XIP)

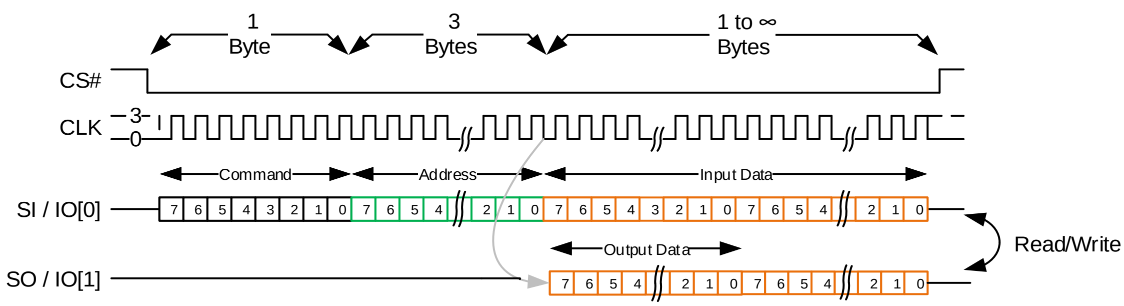


Figure 11: Description of (1-1-1) Augmented Storage Instruction Type

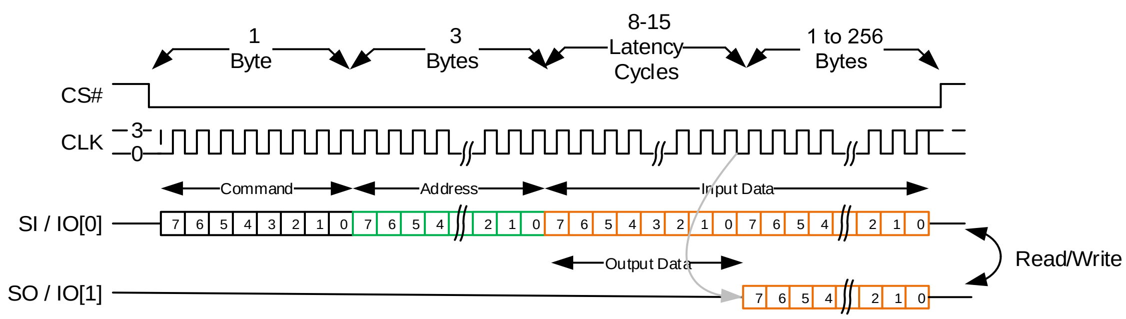


Figure 12: Description of (1-1-1) Instruction Type (With XIP)

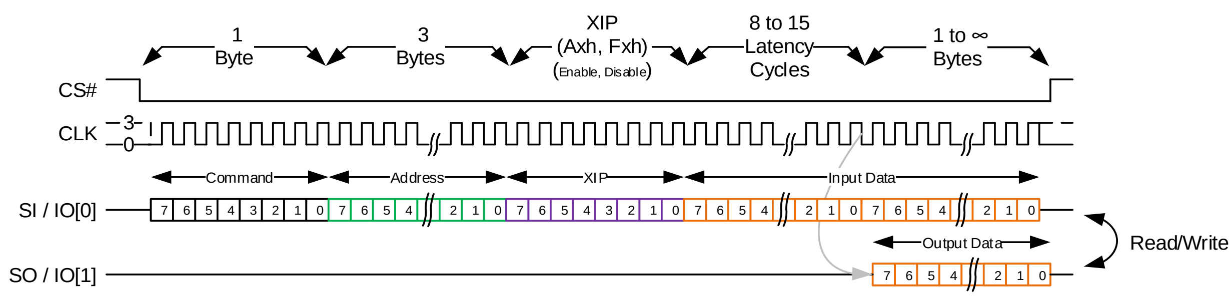


Figure 13: Description of (1-1-2) Instruction Type (With XIP)

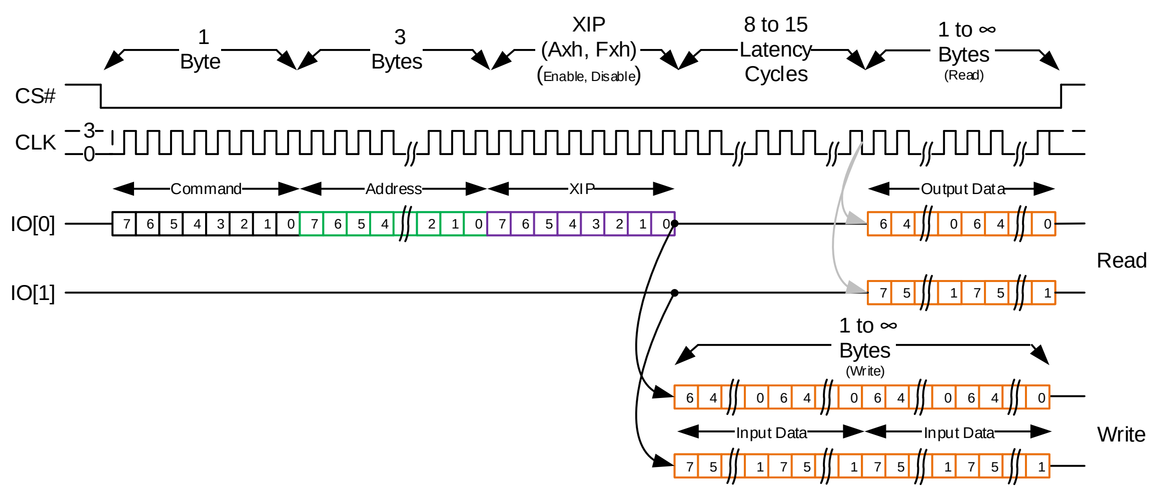


Figure 14: Description of (1-2-2) Instruction Type (With XIP)

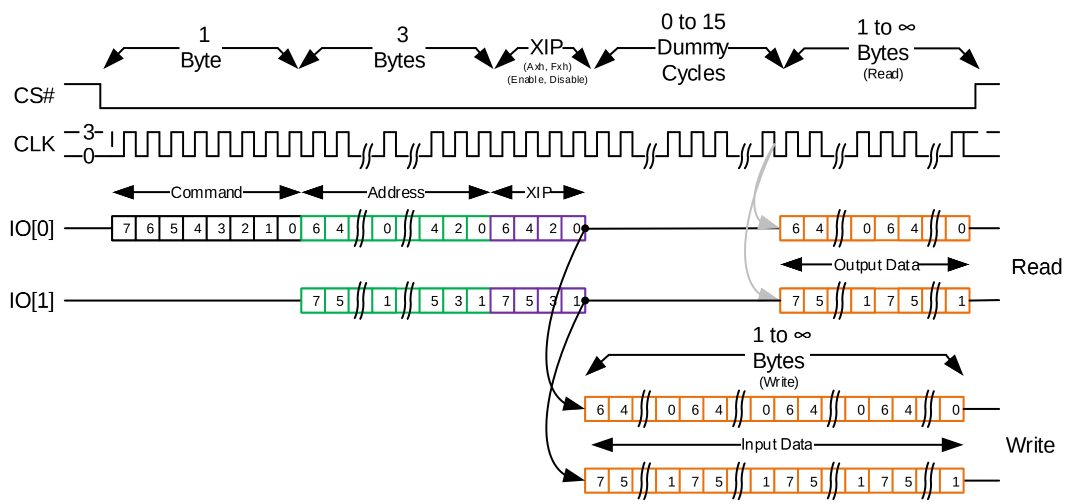


Figure 15: Description of (2-0-0) Instruction Type

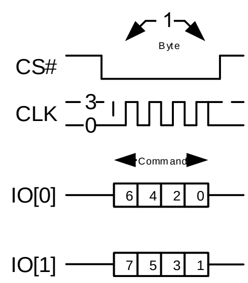


Figure 16: Description of (2-0-2) Instruction Type

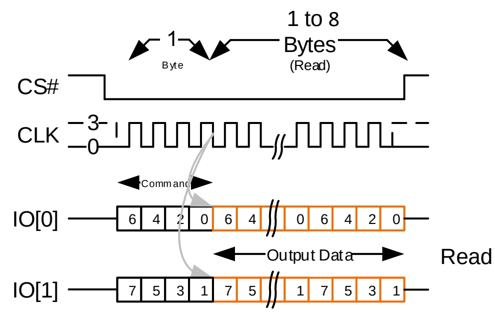


Figure 17: Description of (2-2-2) Any Register Instruction Type

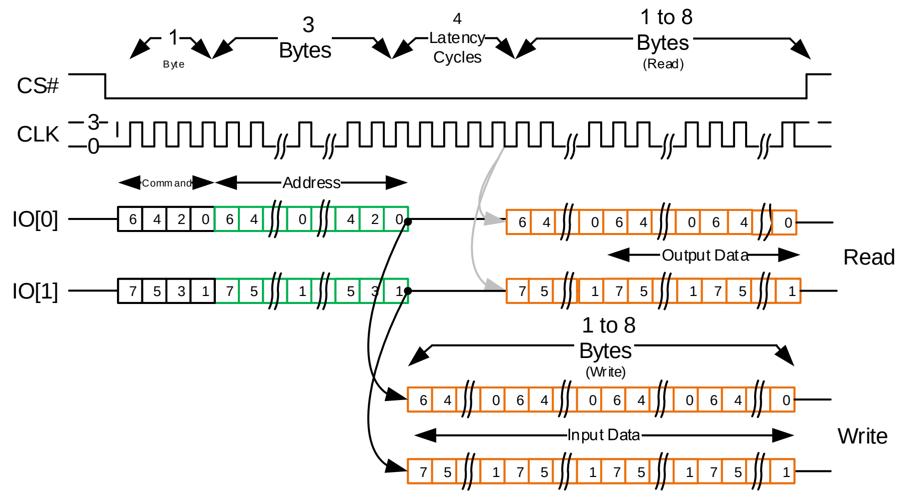


Figure 18: Description of (2-2-2) Instruction Type (With XIP)

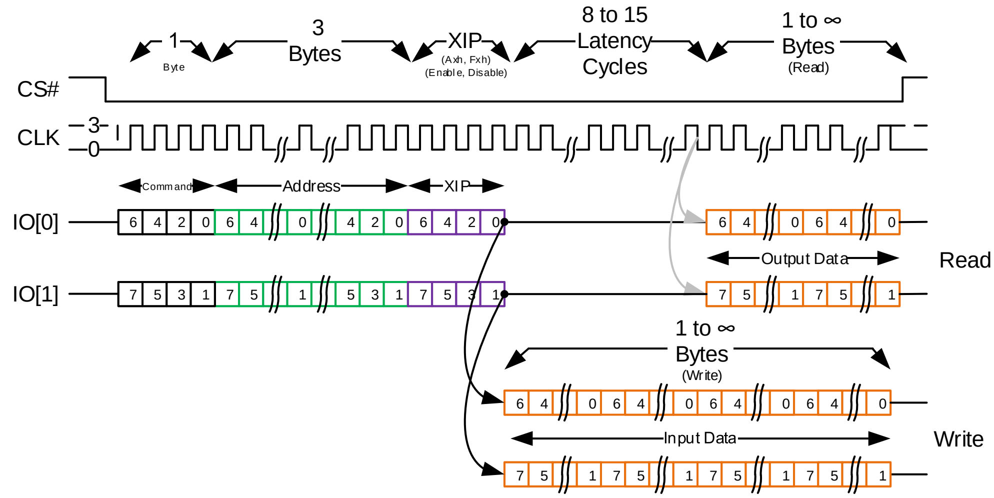


Figure 19: Description of (1-1-4) Instruction Type (With XIP)

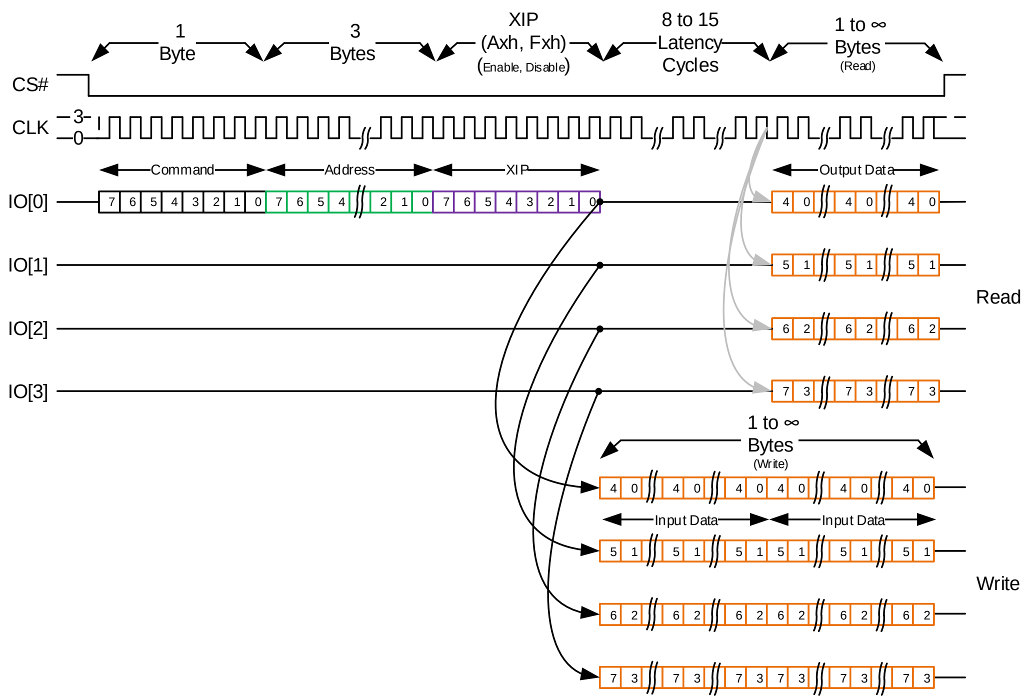


Figure 20: Description of (1-4-4) Instruction Type (With XIP)

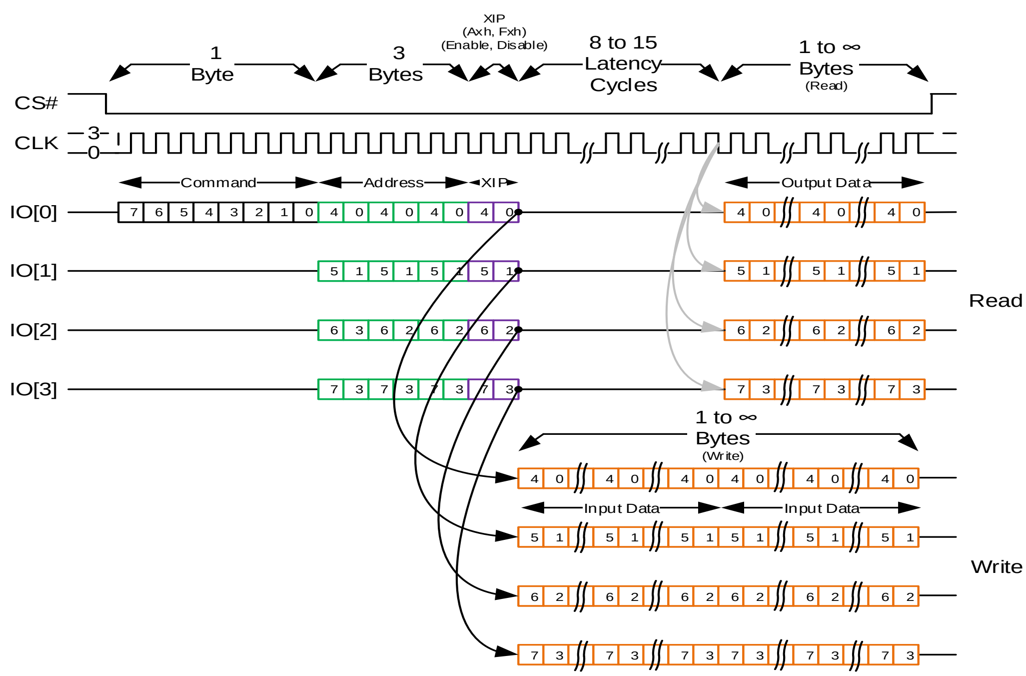


Figure 21: Description of (4-0-0) Instruction Type

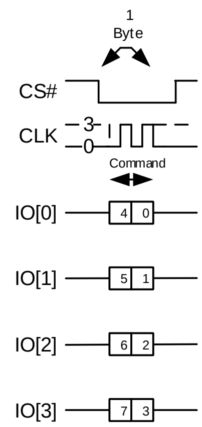


Figure 22: Description of (4-0-4) Instruction Type

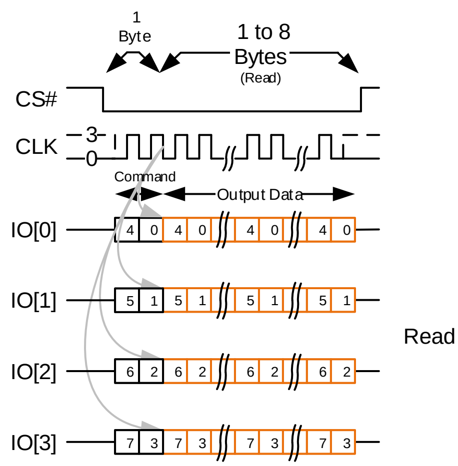


Figure 23: Description of (4-4-4) Any Register Instruction Type

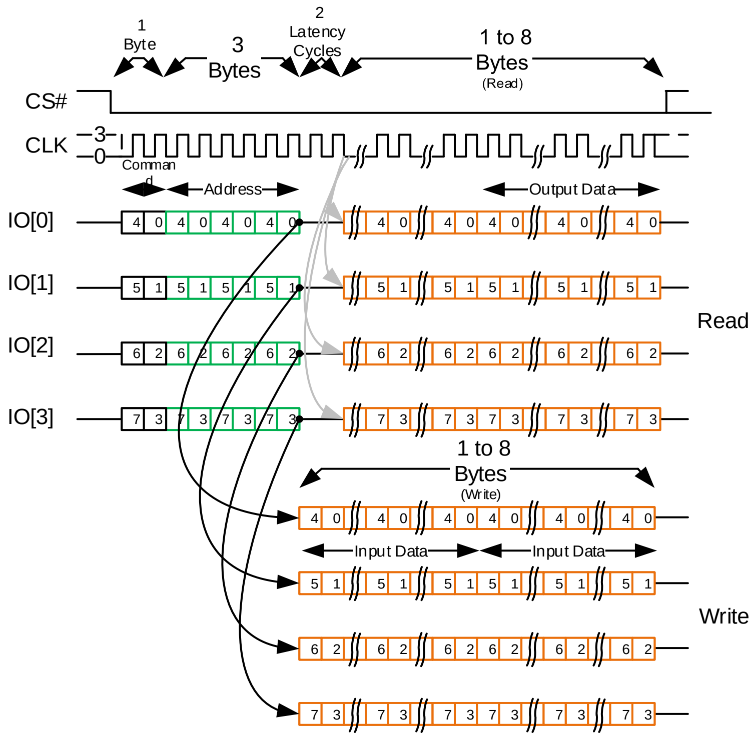
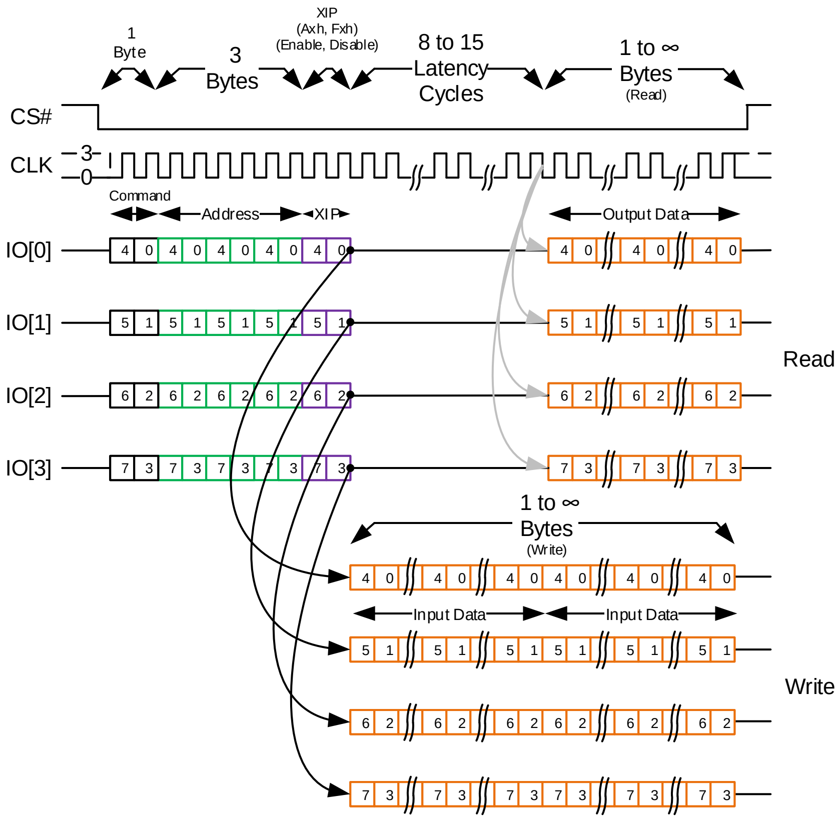


Figure 24: Description of (4-4-4) Instruction Type (With XIP)



Electrical Specifications

Table 29: Tested Operating Conditions

Parameter / Condition		Minimum	Typical	Maximum	Units
Operating Temperature	Industrial Extended	-40.0	-	125.0	°C
V_{CC} Supply Voltage (3.0V)	3.0V	2.7	3.0	3.6	V
V_{CC} Supply Voltage (1.8V)	1.8V	1.71	1.8	2.0	V
V_{SS} Supply Voltage		0.0	0.0	0.0	V

Table 30: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{IN}	5.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{INOUT}	6.0	pF

Table 31: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	125°C	10	years
		105°C	10	
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Table 32: 3.0V DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			
				Minimum	Typical	Maximum	Units
Read Current (1-1-1) SDR	I_{READ1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	8	9	mA
Read Current (2-2-2) SDR	I_{READ2}			-	9	10	mA
Read Current (4-4-4) SDR	I_{READ3}			-	10	12	mA
Write Current (1-1-1) SDR	I_{WRITE1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	14	16	mA
Write Current (2-2-2) SDR	I_{WRITE2}			-	17	20	mA
Write Current (4-4-4) SDR	I_{WRITE3}			-	22	25	mA
Standby Current	I_{SB}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	160	-	µA
			Ta = 85ºC	-	-	400	µA
			Ta =105ºC	-	-	600	µA
Deep Power Down Current	I_{DPD}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	5	25	µA
Hibernate Current	I_{HBN}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	0.1	-	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA		V_{CC}-0.2	-	-	V
		I_{OH} = -1mA		2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA		-	-	0.2	V
		I_{OL} = 2mA		-	-	0.4	V

Table 33: 1.8V DC Characteristics

Parameter	Symbol	Test Conditions		1.8V Device (1.71V-2.0V)			
				Minimum	Typical	Maximum	Units
Read Current (1-1-1) SDR	I_{READ1}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	5	8	mA
Read Current (2-2-2) SDR	I_{READ2}			-	6	9	mA
Read Current (4-4-4) SDR	I_{READ3}			-	7	11	mA
Write Current (1-1-1) SDR	I_{WRITE1}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	13	15	mA
Write Current (2-2-2) SDR	I_{WRITE2}			-	16	19	mA
Write Current (4-4-4) SDR	I_{WRITE3}			-	20	23	mA
Standby Current	I_{SB}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	140	-	µA
			Ta = 85ºC	-	-	350	µA
			Ta=105ºC	-	-	500	µA

Parameter	Symbol	Test Conditions	1.8V Device (1.71V-2.0V)			
			Minimum	Typical	Maximum	Units
Deep Power Down Current	I_{DPD}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	-	4	20	µA
Hibernate Current	I_{HBN}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	-	0.1	-	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±1.0	µA
WP# Leakage Current	$I_{WP\#LI}$	V_{IN}=0 to V_{CC} (max)	-100.0	-	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±1.0	µA
Input High Voltage	V_{IH}		0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA	V_{CC}-0.2	-	-	V
		I_{OH} = -1mA	1.5	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA	-	-	0.2	V
		I_{OL} = 2mA	-	-	0.4	V

Absolute Maximum Ratings

Stresses greater that those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 34: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Junction Temperature	---	125	°C
Storage Temperature	-55 to 150		°C
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test) JESD78	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Table 35: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	3.0ns
Input and output measurement timing levels	$V_{CC}/2$
Output Load	CL = 30.0pF

CS# Operation & Timing

Figure 25: CS# Operation & Timing

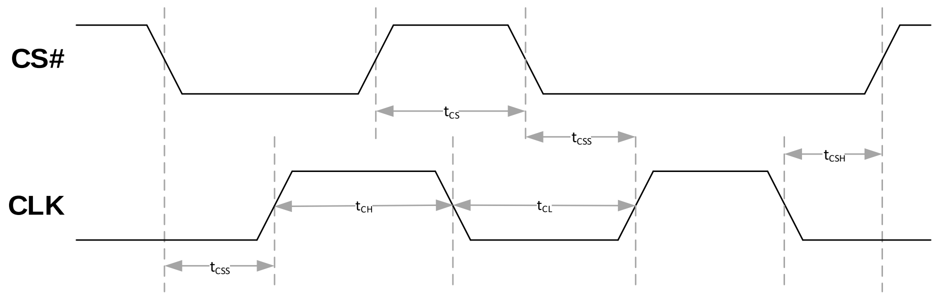


Table 36: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	54	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Register Write Cycle[1]	t_{CS2}	5	-	µs
Chip Deselect Time after Write Cycle (SPI)	t_{CS3}	280	-	ns
Chip Deselect Time after Write Cycle (DPI)	t_{CS4}	350	-	ns
Chip Deselect Time after Write Cycle (QPI)	t_{CS5}	490[2]	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:
Power supplies must be stable
1:SDR operation only
2:For single byte operations, t_{CS5} is 280ns

Command, Address, XIP and Data Input Operation & Timing

Figure 26: SDR Command, Address and Data Input Operation & Timing

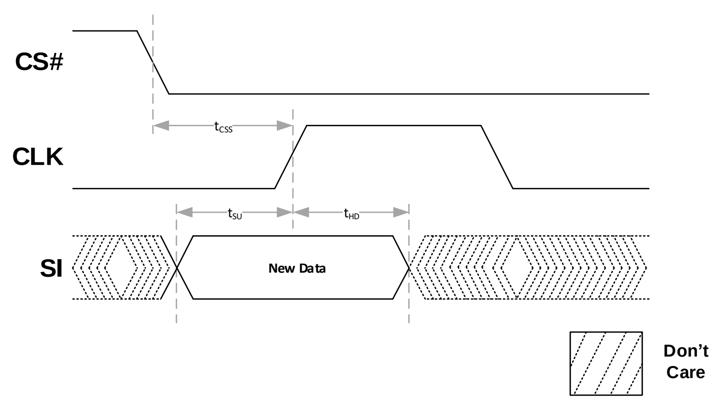


Table 37: SDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	2.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	3.0	-	ns

Notes:
Power supplies must be stable

Figure 27: DDR Command, Address and Data Input Operation & Timing

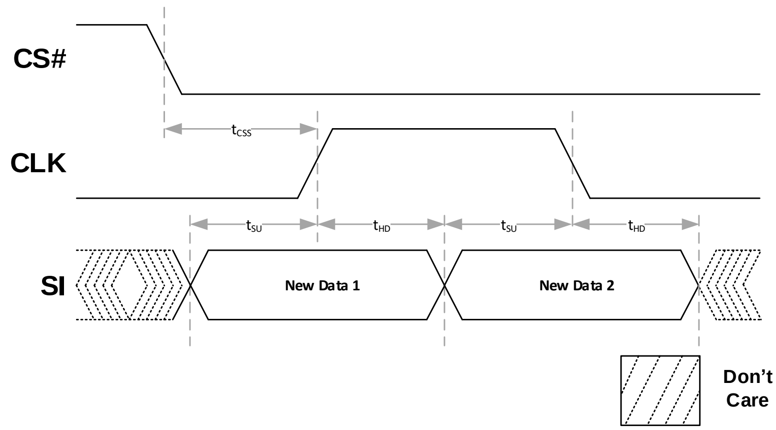


Table 38: DDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	4.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	4.0	-	ns

Notes:
Power supplies must be stable

Data Output Operation & Timing

Figure 28: SDR Data Output Operation & Timing

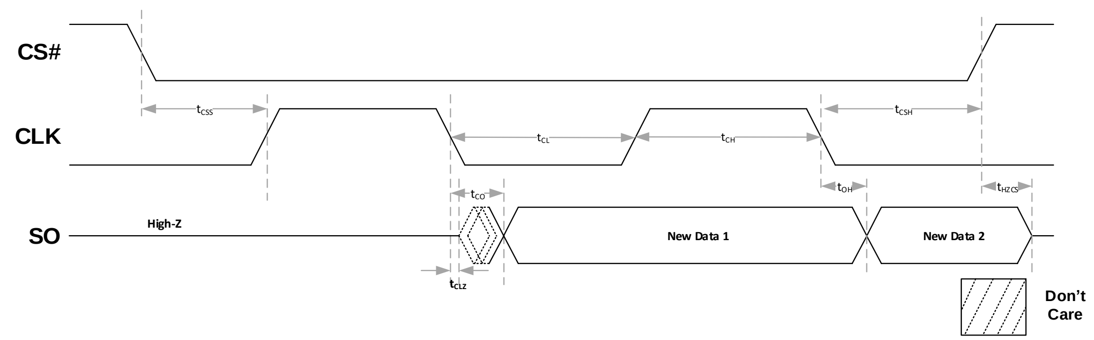


Table 39: SDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	7.0	ns

Notes:
Power supplies must be stable

Figure 29: DDR Data Output Operation & Timing

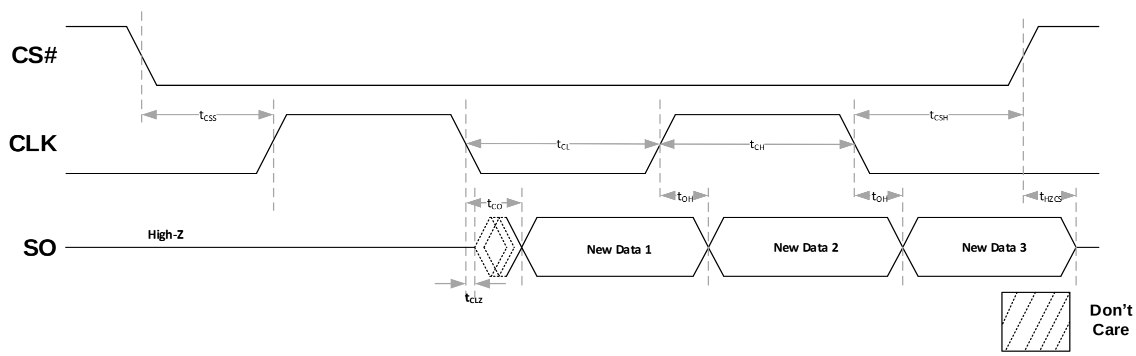


Table 40: DDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	6.0	ns

Notes:
Power supplies must be stable

WP# Operation & Timing

Figure 30: WP# Operation & Timing

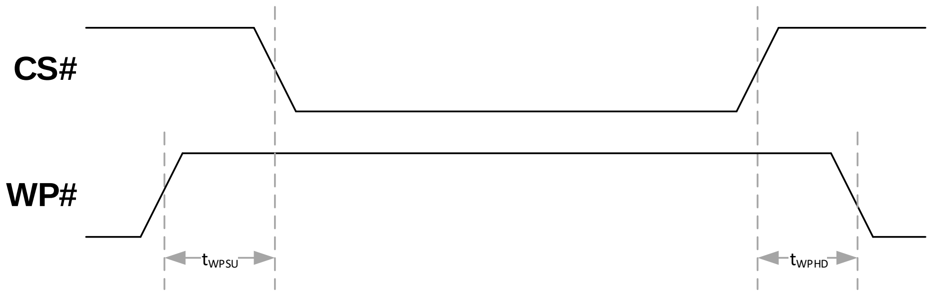


Table 41: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:
Power supplies must be stable

JEDEC Reset Operation & Timing

Figure 31: JEDEC Reset Operation & Timing

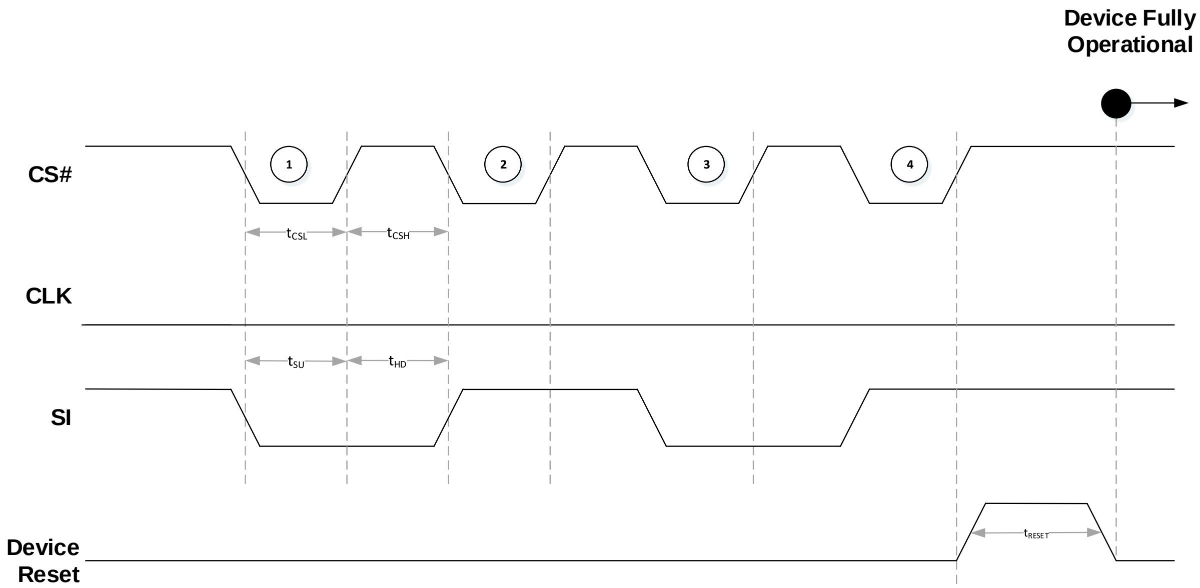


Table 42: JEDEC Reset Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CS# Low Time	t_{CL}	1.0	-	µs
CS# High Time	t_{CH}	1.0	-	µs
SI Setup Time (w.r.t CS#)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t CS#)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	450.0	µs
Software Reset[1]	t_{SRST}	-	50.0	µs

Notes:
Power supplies must be stable
1: Software Reset timing is for Instruction based Reset (SRST)

Enter Deep Power Down Command (EDP – B9h)

The command sequences are shown below. Executing the Enter Deep Power down (EDP) command is the only way to put the device in the deep power down mode. The device consumption drops to I_{DP}.

The deep power down mode subsequently reduces the standby current from I_{SB} to I_{DP}. No other command must be issued while the device is in deep power down mode.

To enter the deep power down mode, CS# is driven low, following the enter deep power down (EDPD) command, CS# must be driven high after the eighth bit of the command code has been latched in or the EDP command will not be executed. After CS# is driven high, it requires a delay of t_{EDPD} (Table 6 and 7) before the supply current is reduced to I_{DP} and the Deep Power Down mode is entered. The command can be issued in SPI or QPI modes.

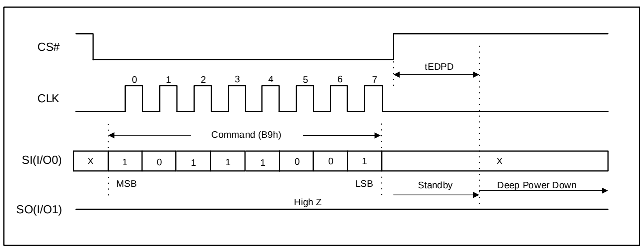


Figure 32: Enter Deep Power Down in SPI Command Sequence

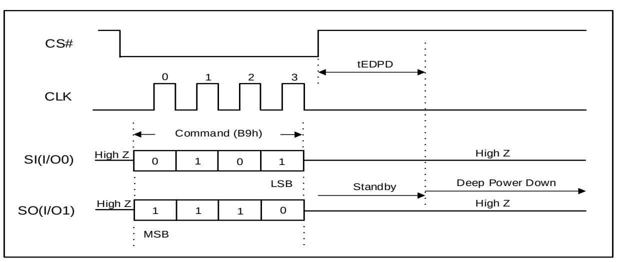


Figure 39: Enter Deep Power Down in DPI Command Sequence

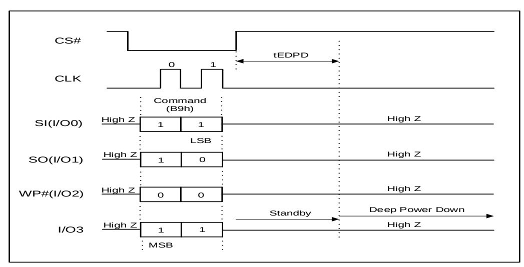


Figure 40: Enter Deep Power Down in QPI Command Sequence

Exit Deep Power Down Command (EXDPD - ABh)

The command sequences are shown below. There are two ways to exit deep power down mode:

1. Toggling CS# with a CS# pulse width of tCSDPD while CLK and I/Os are Don't Care. During waking up from deep power down, I/Os remain to be in high Z.

2. Driving CS# low follows with the Exit Deep Power Down (EXDPD) command. CS# must be driven high after the eight bit of the command code has been latched in or the EXDPD command will not executed.

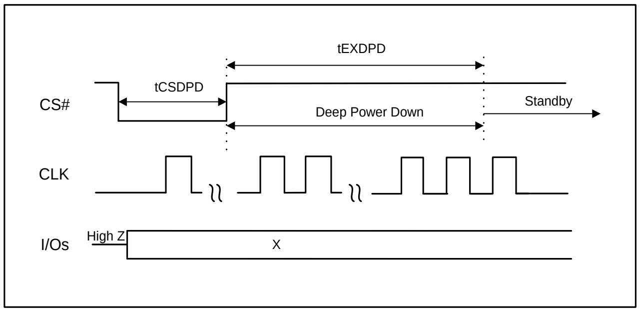


Figure 41: Exit Deep Power Down by Toggling CS#

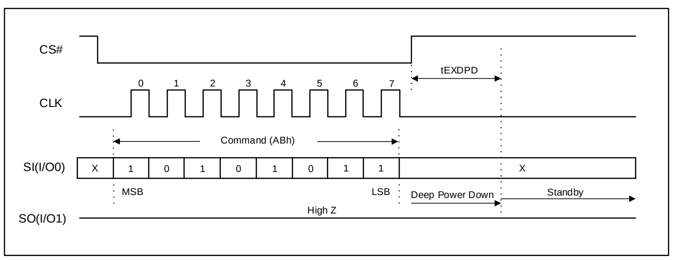


Figure 42: Exit Deep Power Down in SPI Command Sequence

It requires a delay of t_{EXDPD} (Table 6 and 7) before the device can fully exit the deep power down mode and enter standby mode. The command can be issued in SPI, DPI, and QPI mode. Status of all non-volatile bits in registers remains unchanged when the device enters or exits the deep power down mode.

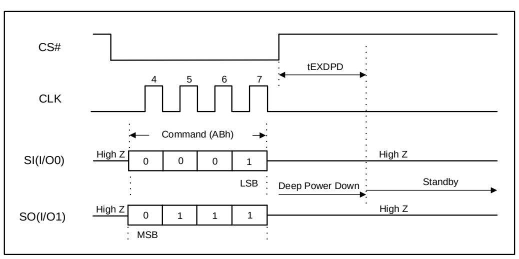


Figure 43: Exit Deep Power Down in DPI Command Sequence

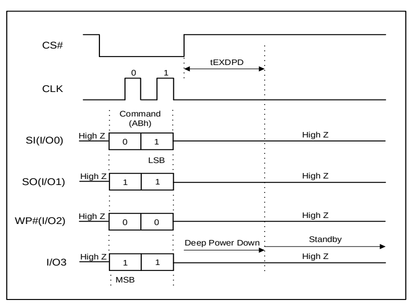


Figure 44: Exit Deep Power Down in QPI Command Sequence

Enter Hibernate Command (EHBN – BAh)

The command sequences are shown below. Executing the Enter Hibernate command is the only way to put the device in the hibernate mode. The device drops down to the lowest power consumption mode: I_{HBN}. When in hibernate mode, the CLK and SI pins are ignored and SO will be high-Z.

To enter the hibernate mode, CS# is driven low, following the Enter Hibernate (EHBN) command. After CS# is driven high, it requires a delay of t_{ENTHIB} time (Table 6 and 7) before the supply current is reduced to I_{HBN} and hibernate mode is entered.

Toggling CS# (low to high) will return the device to standby mode. The command can be issued in SPI, DPI, and QPI modes.

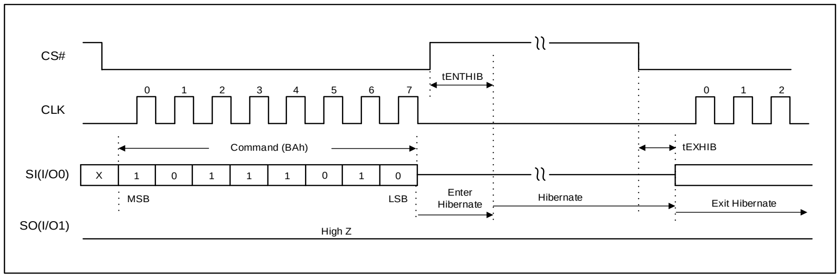


Figure 45: Enter Hibernate in SPI Command Sequence

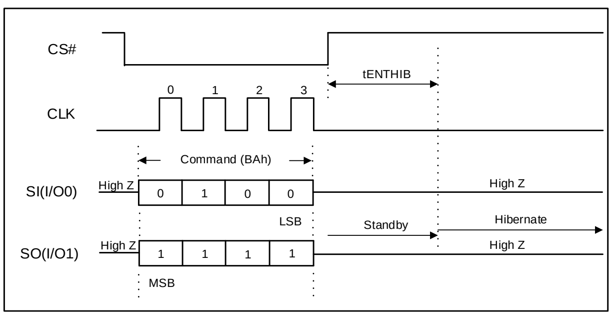


Figure 46: Enter Hibernate in DPI Command Sequence

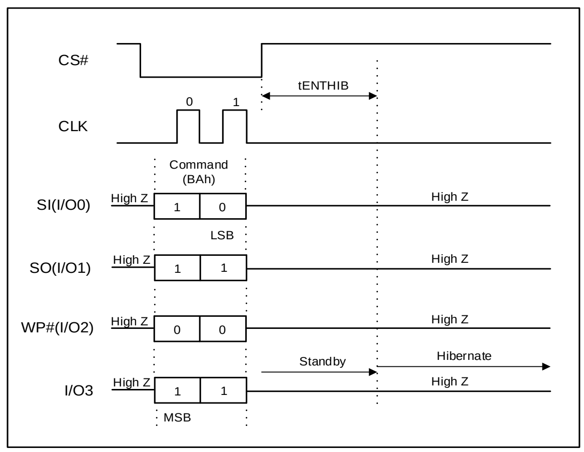


Figure 47: Enter Hibernate in QPI Command Sequence

Thermal Resistance

Table 43: Thermal Resistance

Parameter	Description	Test Conditions	8-pad WSON	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	43.67	53.59	°C/W
θ_{JC}	Thermal resistance (junction to case)		18.54	4.29	

Notes:
1: These parameters are guaranteed by characterization; not tested in production.

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Revision History

Revision	Date	Change Summary
REV J	03/04/2020	Added ESD and Latch-up specifications (Table 36). Corrected table numbering. Removed 3 rows on Table 23 with latency and changed to 50MHz for 108. Table 28: Instructions Set Read 03h: Removed 2-2-2, 4-4-4 and latency cycles dots, freq=50MHz Write 02h: Removed 2-2-2 and 4-4-4 dots. RDAS 4Bh: Added latency cycles dot, removed 2-2-2 and 4-4-4 dots, freq=50MHz WRAS 42h: Removed 2-2-2 and 4-4-4 dots. Added Table 24 for Augment Storage Array Read Latency vs Max Frequency. Removed Augmented Storage Protection Register from Table 11. Added Augmented Storage (1-1-1) Figure 12. Changed 2-2-2 and 4-4-4 (Figure 18 and 24) to Any Register Instruction diagrams. Changed all XIP diagrams from 0-15 dummy cycles to 8-15 latency cycles. Removed 0-15 dummy cycles from 1-1-1 without XIP (Figure 11). Changed tCSDPD to 50ns in Table 6 and Table 7. Removed Advanced from the footer.
REV K	06/03/2020	Swapped Standby and Deep Power Down in Figure 38. Removed mode in Figures 39, 45 and 46. Added junction and storage temperature specifications. Combined magnetic immunity and ESD tables. Updated burn-in specification and part numbers. Removed Serial Number Register from Table 11. Updated latency values in Table 22. Updated Icc and Isb values in Tables 32 and 33. Updated chip deselect values in Table 36 and Note 1. Added note 7 for Table 28.
REV L	07/17/2020	Updated ICC values in Tables 32 and 33. Corrected Figures 38 and 42.
REV M	09/11/2020	Removed 1Mb, 4Mb, 8Mb densities and BGA package options. Changed the burn in temperature to 125^{O}C. Changed Endurance to 10^{14} write cycles. Added thermal resistance specifications.
REV N	10/08/2020	Removed 108MHz operation, DDR mode Changed Endurance back to 10^{16} Updated Ordering Part Number decoder and valid product OPN table
REV O	07/16/2021	Added REACH Compliance Updated Product Use Limitations
REV P	03/15/2022	Corrected Manufacturer ID Temp field from 0002 to 0010