High Rel Parallel Persistent SRAM Memory

(AS3016B16, AS3032B16, AS3064B16)

Features

- Interface
  - Parallel Asynchronous x16
- Technology
  - 40nm pMTJ STT-MRAM
    - Virtually unlimited Endurance and Data Retention (see Endurance and Data Retention: Table 16)
- Density
  - 16Mb, 32Mb, 64Mb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
- Operating Temperature Range
  - Industrial Extended -40°C to 125°C
- Packages
  - 48-ball FBGA (10mm x 10mm)
- Memory Array Organization
  - 16Mbit
    - 1,048,576 x 16
  - 32Mbit
    - 2,097,152 x 16
  - 64Mbit
    - 4,194,304x 16
- 48-Hour Burn In
- RoHS & REACH Compliant

Performance

Device Operation	Typical Values	Units
Read Cycle Time	45.0 (minimum)	ns
Write Cycle Time	45.0 (minimum)	ns
Standby Current	3.5 (typical)*	mA
Read Current	20.0 (typical)	mA
Write Current	20.0 (typical)	mA

*Number shown is for 16Mb device

Table of Contents

Features 1
Performance 1
Table of Contents 2
General Description 3
Ordering Options 4
  Valid Combinations — Standard 5
Signal Description and Assignment 6
Package Options 7
  AS3016B16-045n in 48-Ball FBGA (Balls Down, Top View) 7
  AS3032B16-045n in 48-Ball FBGA (Balls Down, Top View) 7
  AS3064B16-045n in 48-Ball FBGA (Balls Down, Top View) 8
Package Drawings 9
  48-Ball FBGA 9
Architecture 9
Device Initialization 11
Electrical Specifications 13
Write Operation 15
Bus Turnaround Operation – Read to Write 17
Read Operation 18
Endurance and Data Retention 19
Product Use Limitations 21
  Limited Warranty 21

General Description

AS30xxB16 is a High Rel grade magneto-resistive random-access memory (MRAM). It is offered in 16Mb, 32Mb and 64Mb density options. MRAM technology is analogous to Flash technology with SRAM compatible 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with 10^{16} write cycles endurance and 10-year retention at 125°C. This makes MRAM a very reliable and fast non-volatile memory solution.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance, high-performance and scalable memory technology.

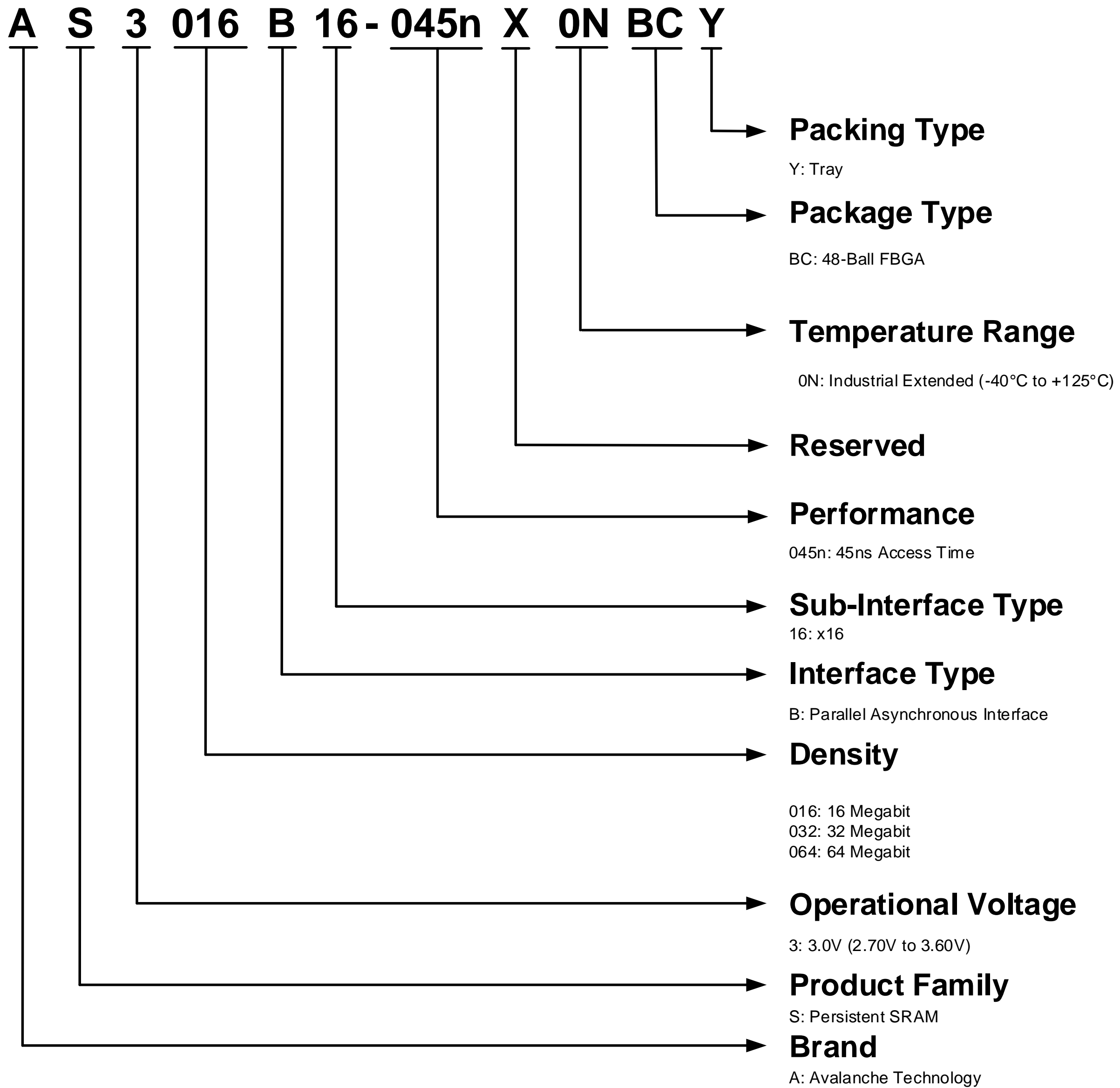
AS30xxB16 is available in small footprint 48-Ball FBGA (10mm x 10mm) packages supporting 16Mb, 32Mb and 32Mb densities. This package is compatible with similar low-power volatile and non-volatile products.

AS30xxB16 is offered in industrial extended (-40°C to 125°C) operating temperature ranges. Every unit goes through a 48-hour burn-in before it is shipped to customers.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Part Number Ordering System



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2: Valid Combinations List

Valid Combinations – 45ns				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS3016B16-045nX	0N	BC	R, Y	AS3016B16-045nX0NBCY
AS3032B16-045nX	0N	BC	R, Y	AS3032B16-045nX0NBCY
AS3064B16-045nX	0N	BC	R, Y	AS3064B16-045nX0NBCY

Signal Description and Assignment

Figure 2: Device Pinout

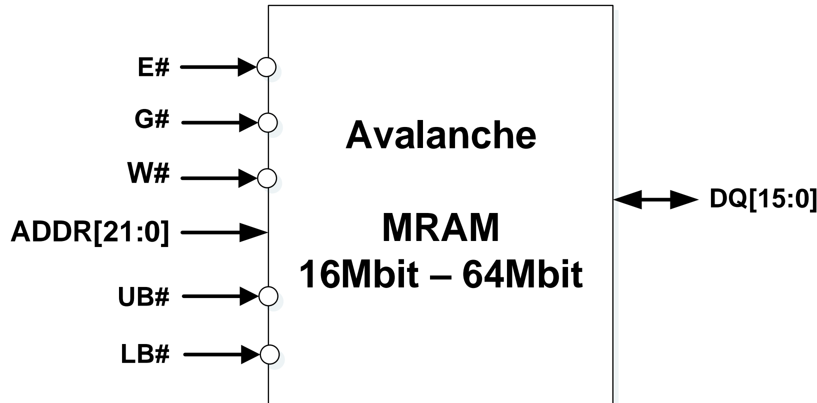
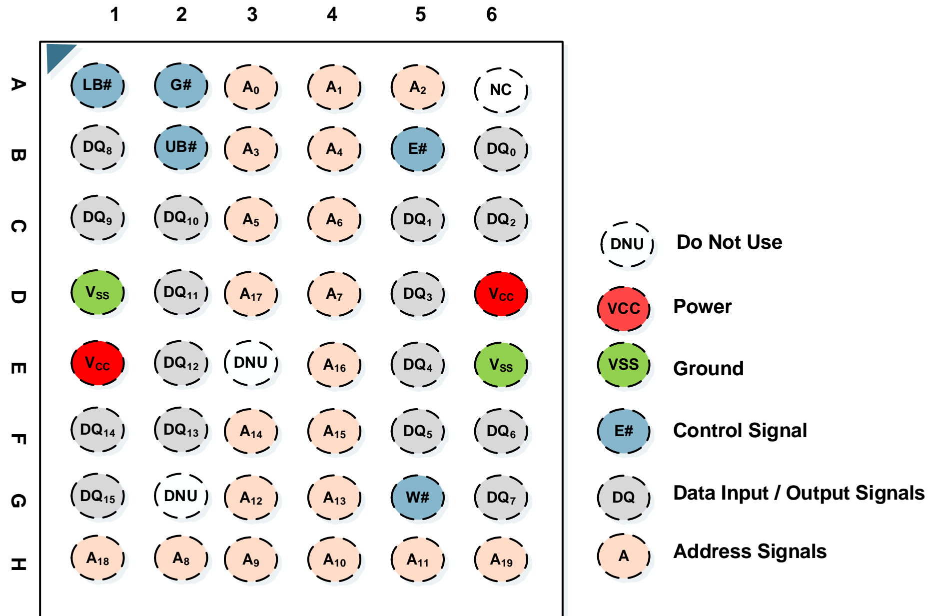


Table 3: Signal Description

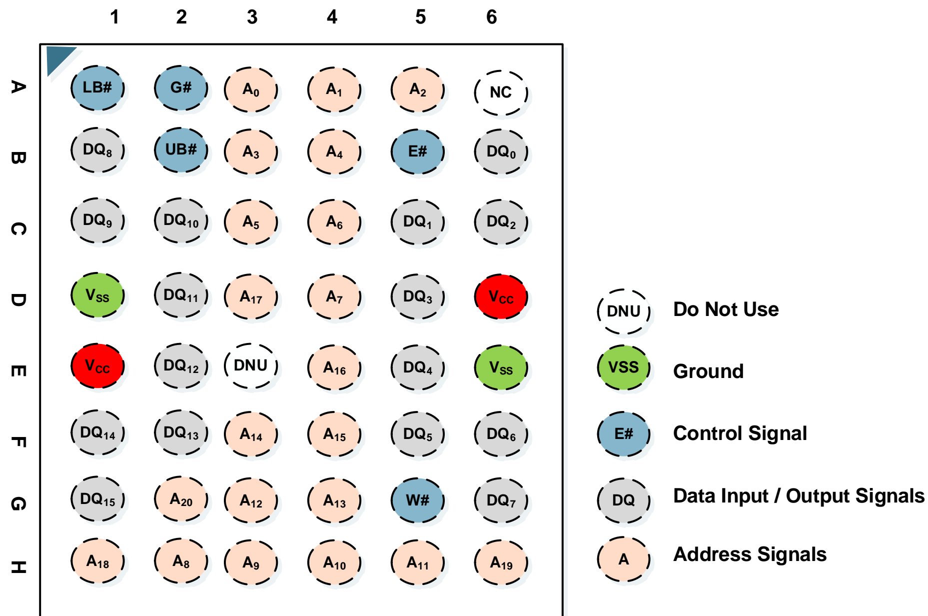
Signal	Type	Description
E#	Input	**Chip enable:** Enables or disables the MRAM.
G#	Input	**Output enable:** Enables the output drivers in bidirectional data transfer I/Os.
W#	Input	**Write enable:** Transfers serial data from the host system to the MRAM when Low (Logic ‘0’).Transfers serial data from the MRAM to the host system when High (Logic ‘1’).
UB#	Input	**Upper Byte Enable:** Enables or disables DQ[15:8]. Not available in 64Mb device.
LB#	Input	**Lower Byte Enable:** Enables or disables DQ[7:0]. Not available in 64Mb device.
ADDR[21:0]	Input	**Address:** I/Os for address transfer. 16M: ADDR[19:0] – 20 Address pins for 16M devices. 32M: ADDR[20:0] – 21 Address pins for 32M devices. 64M: ADDR[21:0] – 22 Address pins for 64M devices.
DQ[15:0]	Input / Output	**Data inputs/outputs:** The bidirectional I/Os transfer data.
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.
NC		**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU		**Do not use:** DNUs must be left unconnected.

Package Options

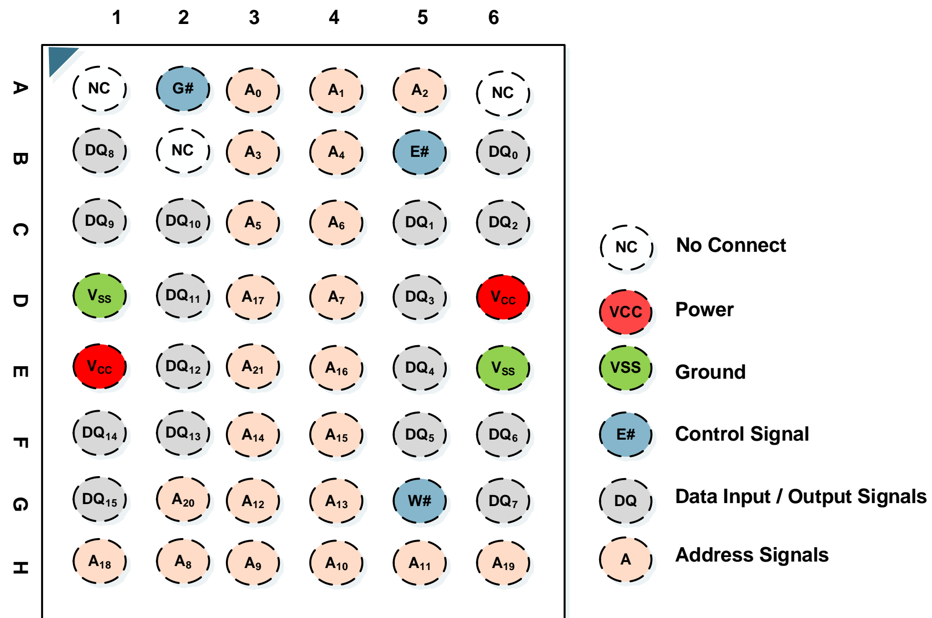
AS3016B16-045n in 48-Ball FBGA (Balls Down, Top View)



AS3032B16-045n in 48-Ball FBGA (Balls Down, Top View)

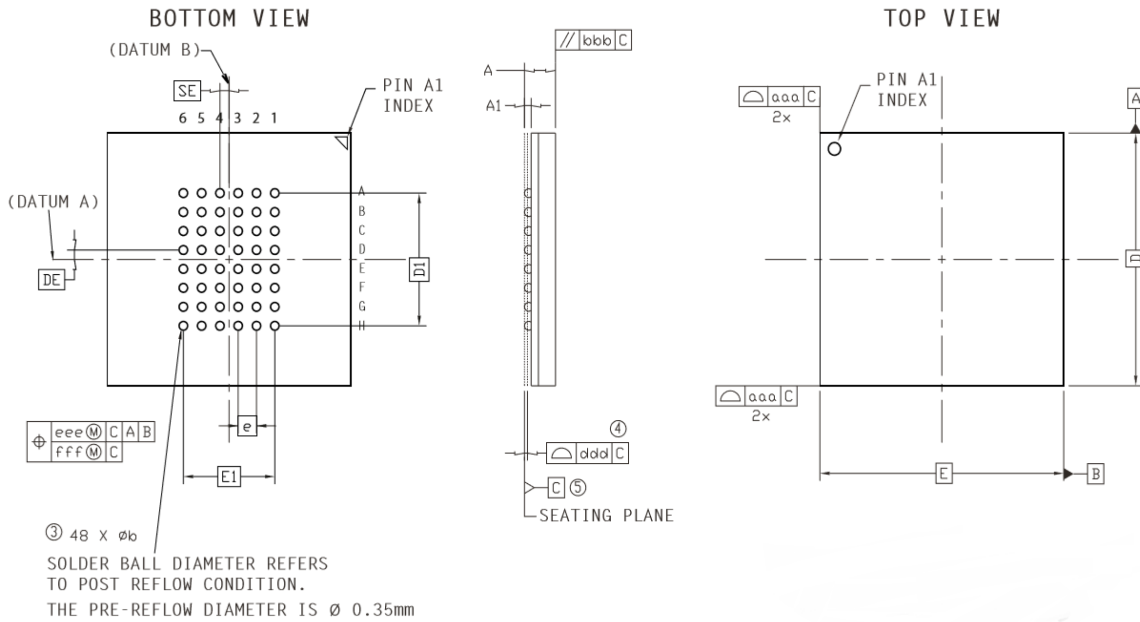


AS3064B16-045n in 48-Ball FBGA (Balls Down, Top View)



Package Drawings

48-Ball FBGA



Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D		10.00 BSC	
E		10.00 BSC	
D1		5.25 BSC	
E1		3.75 BSC	
DE		0.375 BSC	
SE		0.375 BSC	
e		0.75 BSC	

Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.10
eee	0.15
fff	0.08

1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
③ 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
④ Dimension 'ddd' is measured parallel to primary datum C.
⑤ Primary datum C (seating plane) is defined by the crowns of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.

Architecture

AS30xxB16 is a high performance MRAM device. Writing to and reading from the device as follows:

To write to the device, bring Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[15]) to be written into the memory location specified by the address pins ADDR[0] through ADDR[20] (54-pin TSOP and 48-ball FBGA) and ADDR[0] through ADDR[17] (44-pin TSOP).

To read from the device, bring Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins ADDR[0] through ADDR[20] (54-pin TSOP and 48-ball FBGA) and ADDR[0] through ADDR[17] (44-pin TSOP) to appear on I/O pins (DQ[0] to DQ[15]).

Figure 3: Functional Block Diagram

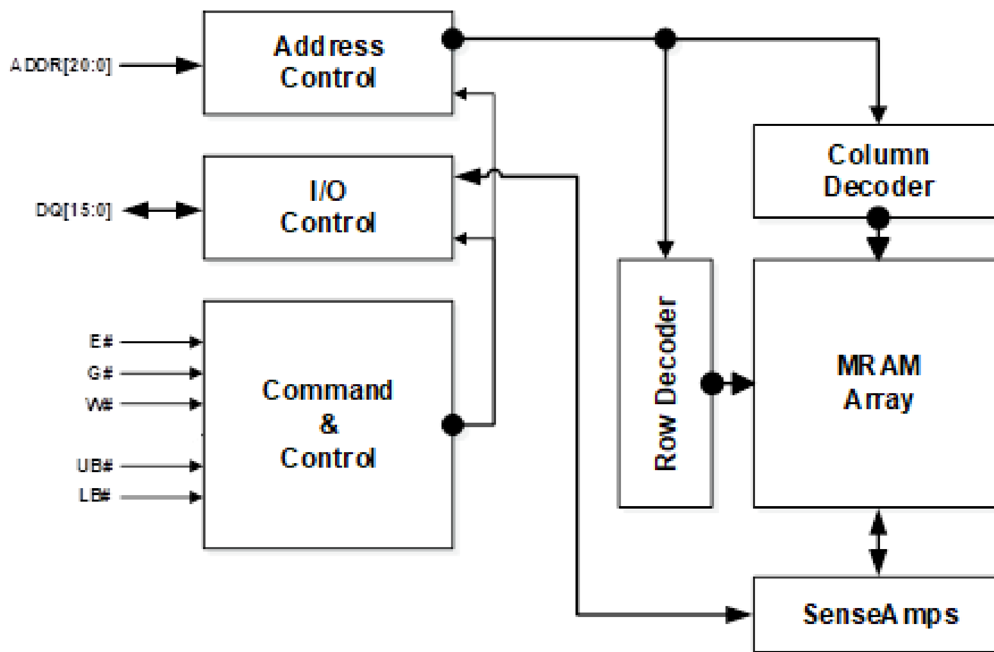


Table 4: Modes of Operation

Mode	E#	G#	W#	SE#	UB#[1]	LB#[1]	Current	DQ[15:8]	DQ[7:0]
Not Selected	H	X	X	H	X	X	I_{SB}	Hi-Z	Hi-Z
Output Disabled	L	H	H	H	X	X	I_{READ}	Hi-Z	Hi-Z
Output Disabled	L	X	X	H	H	H	I_{READ}	Hi-Z	Hi-Z
Read Upper Byte	L	L	H	H	L	H	I_{READ}	Dataout	Hi-Z
Read Lower Byte	L	L	H	H	H	L	I_{READ}	Hi-Z	Dataout
Read Word	L	L	H	H	L	L	I_{READ}	Dataout	Dataout
Write Upper Byte	L	X	L	H	L	H	I_{WRITE}	Datain	Hi-Z
Write Lower Byte	L	X	L	H	H	L	I_{WRITE}	Hi-Z	Datain
Write Word	L	X	L	H	L	L	I_{WRITE}	Datain	Datain

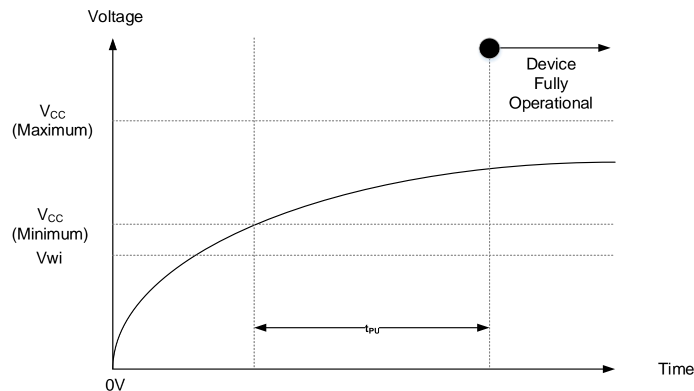
Notes:
H: High (Logic '1') X: Don't Care
L: Low (Logic '0') Hi-Z: High Impedance
1: UB# and LB# functionality is not available in 64Mb device.

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- E#, W#, G#, SE# must follow V_{CC} during power-up

Figure 4: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G#, SE# must follow V_{CC} during power-down
- During power loss or brownout, where Vcc goes below Vwi, read/write operations are prohibited. The power-up timing needs to be observed after Vcc goes above Vcc (minimum)

Figure 5: Power-Down Behavior

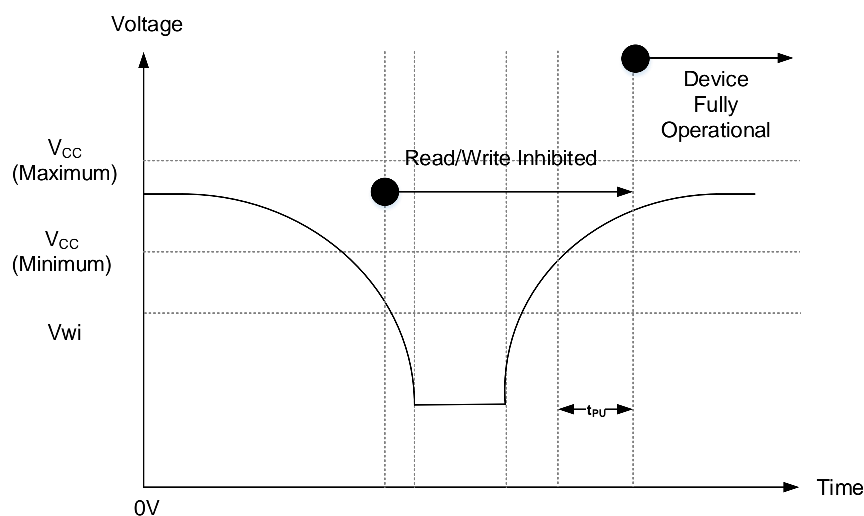


Table 6: Device Initialization Timing – 3.0V

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Power Up to First Instruction	t_{PU}	All operating voltages and temperatures	1	-	-	ms

Electrical Specifications

Table 7: Recommended Operating Conditions

Parameter / Condition		Minimum	Typical	Maximum	Units
	Industrial Extended	-40.0	-	125.0	°C
V_{CC} Supply Voltage	3.0V	2.7	3.0	3.6	V
V_{SS} Supply Voltage		0.0	0.0	0.0	V
Vwi Write Inhibit Voltage		2.1	2.3	2.5	V

Table 8: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V; Density = 16Mb	C_{IN}	10.0	pF
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V; Density = 32Mb		20.0	
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V; Density = 64Mb		40.0	
Input / Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V; Density = 16Mb	C_{INOUT}	10.0	pF
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V; Density = 32Mb		20.0	
	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V; Density = 64Mb		20.0	

Table 9: DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			Units
				Minimum	Typical	Maximum	
Read Current	I_{READ}	V_{CC} (max), I_{OUT}=0mA	16Mb	-	20.0	30.0	mA
			32Mb	-	20.0	30.0	
			64Mb	-	40.0	60.0	
Write Current	I_{WRITE}	V_{CC} (max)	16Mb	-	20.0	30.0	mA
			32Mb	-	20.0	30.0	
			64Mb	-	40.0	60.0	
Standby Current Industrial Extended (-40°C to 125°C)	I_{SB}	E#=V_{IH}, V_{CC} (max)	16Mb	-	3.5	4.5	mA
			32Mb		7.0	9.0	
			64Mb		14.0	18.0	
Sleep Mode Current	I_{SLP}	V_{CC} (max), 125°C	16Mb	-	50	70	uA
			32Mb		100	140	
			64Mb		200	280	
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.5	-	0.2xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -1.6mA		V_{CC}-0.5	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1.6mA		-	-	0.4	V

Table 10: Magnetic Immunity Characteristics

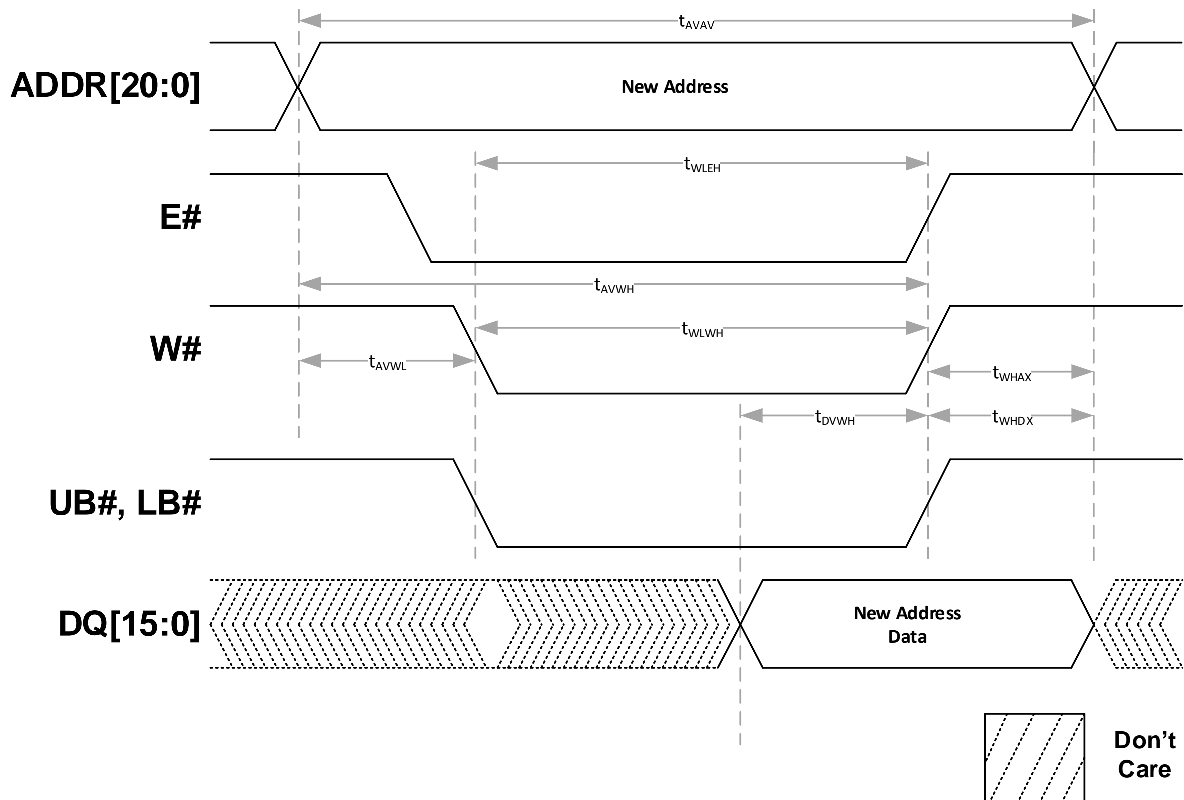
Parameter	Symbol	Maximum	Units
Magnetic Field During Write	H_{max_write}	24000	A/m
Magnetic Field During Read	H_{max_read}	24000	A/m

Table 11: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	5ns
Input and output measurement timing levels	V_{CC}/2
Output Load	CL = 30pF

Write Operation

Figure 7: Write Operation (W# Controlled)



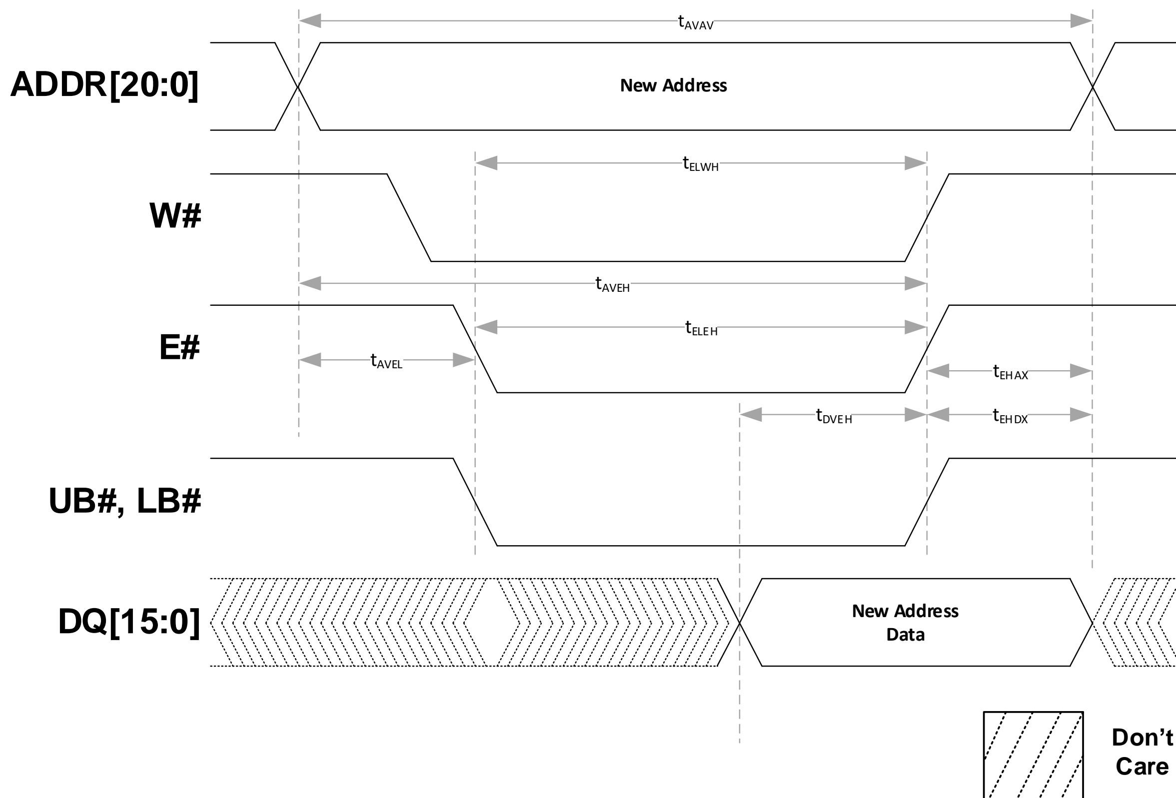
Note: UB#, LB# not available in 64Mb device.

Table 12: Write Operation (W# Controlled)

Parameter	Symbol	Minimum 45ns	Maximum	Units
Write Cycle Time	t_{AVAV}	45	-	ns
Address Set-Up Time	t_{AVWL}	0	-	ns
Address Valid to end of Write (G# High)	t_{AVWH}	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVWH}	30	-	ns
Write Pulse Width (G# High)	t_{WLWH}, t_{WLEH}	25	-	ns
Write Pulse Width (G# Low)	t_{WLWH}, t_{WLEH}	25	-	ns
Data Valid to end of Write	t_{DVWH}	15	-	ns
Data Hold Time	t_{WHDX}	0	-	ns
Write recovery Time	t_{WHAX}	12	-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

Figure 8: Write Operation (E# Controlled)



Note: UB#, LB# not available in 64Mb device.

Table 13: Write Operation (E# Controlled)

Parameter	Symbol	Minimum 45ns	Maximum	Units
Write Cycle Time	t_{AVAV}	45	-	ns
Address Set-Up Time	t_{AVEL}	0	-	ns
Address Valid to end of Write (G# High)	t_{AVEH}	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVEH}	30	-	ns
Write Pulse Width (G# High)	t_{ELWH}, t_{ELEH}	25	-	ns
Write Pulse Width (G# Low)	t_{ELWH}, t_{ELEH}	25	-	ns
Data Valid to end of Write	t_{DVEH}	15	-	ns
Data Hold Time	t_{EHDX}	0	-	ns
Write recovery Time	t_{EHAX}	12	-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as W# goes low

Bus Turnaround Operation – Read to Write

Figure 9: Bus Turnaround Operation

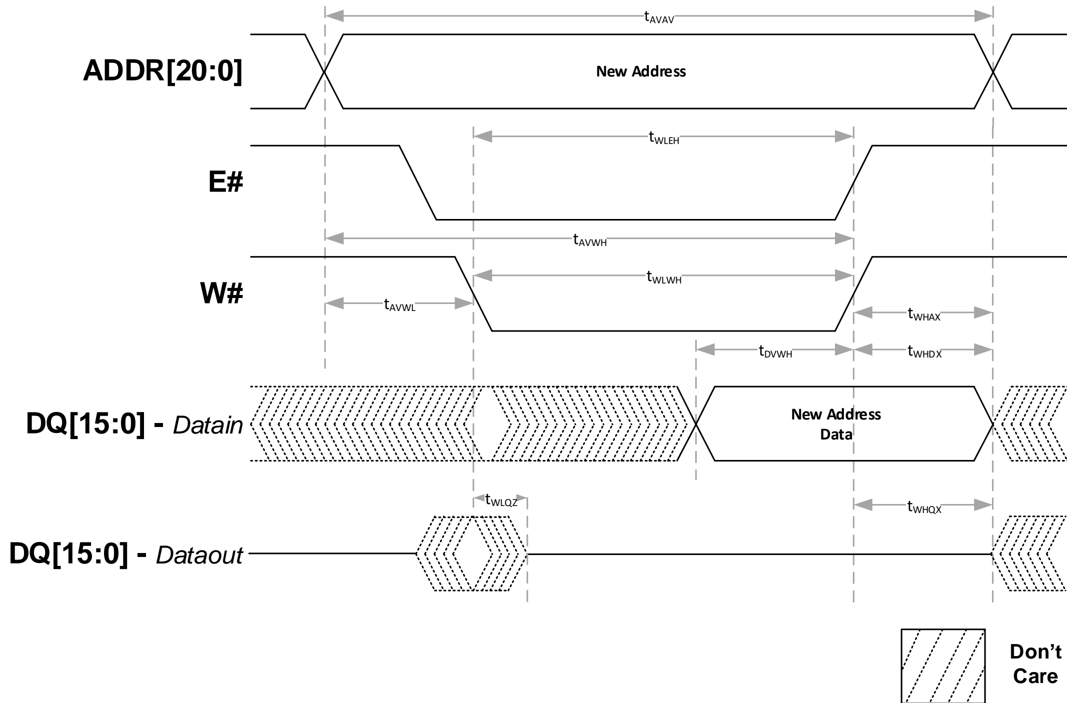


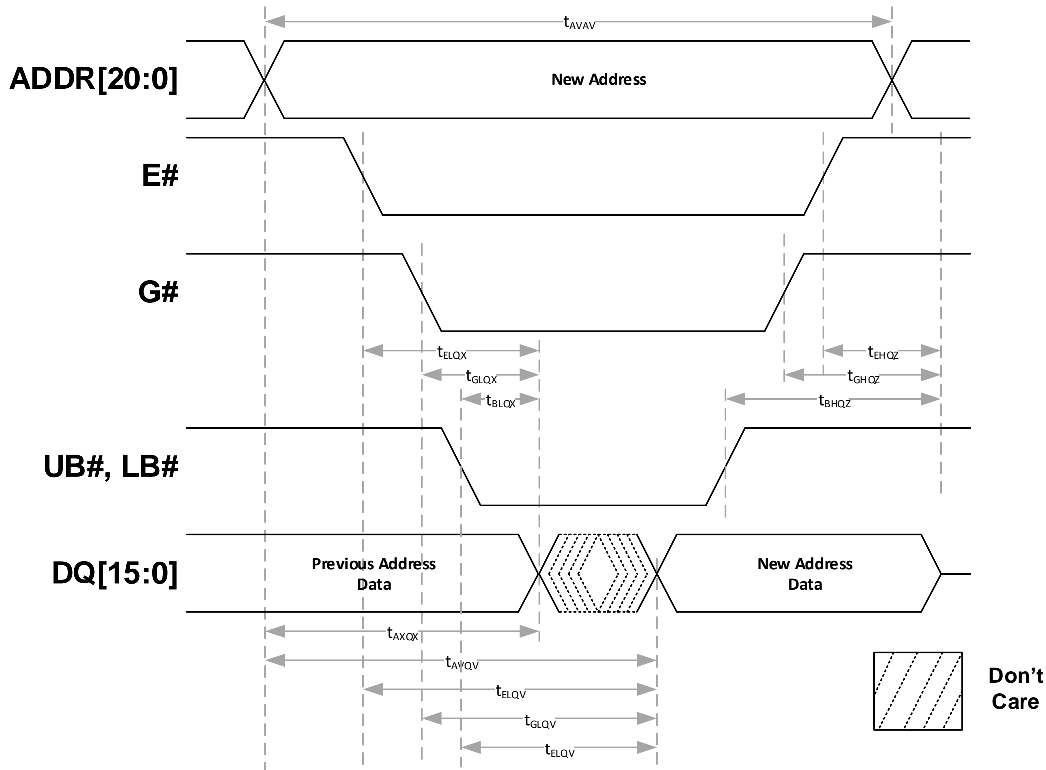
Table 14: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
			45ns	
W# Low to Data Hi-Z	t_{WLQZ}	0	15	ns
W# High to Output Active	t_{WHQX}	3	-	ns

Notes:
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

Read Operation

Figure 10: Read Operation



Note: UB#, LB# not available in 64Mb device.

Table 15: Read Operation

Parameter	Symbol	Minimum	Maximum	Units
		45ns	45ns	
Read Cycle Time	t_{AVAV}	45	-	ns
Address Cycle Time	t_{AVQV}	-	45	ns
Chip Enable Access Time	t_{ELQV}	-	45	ns
Output Enable Access Time	t_{GLQV}	-	25	ns
Byte Enable Access Time	t_{BLQV}	-	25	ns
Output Hold From Address Change	t_{AXQX}	3	-	ns
Chip Enable Low to Output Active	t_{ELQX}	3	-	ns
Output Enable Low to Output Active	t_{GLQX}	0	-	ns
Byte Enable Low to Output Active	t_{BLQX}	0	-	ns
Chip Enable High to Output Hi-Z	t_{EHQZ}	0	15	ns
Output Enable High to Output Hi-Z	t_{GHQZ}	0	15	ns
Byte Enable High to Output Hi-Z	t_{BHQZ}	0	10	ns

Notes:

W# is High (Logic '1') for Read operation

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

Endurance and Data Retention

Table 16: Endurance and Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	125°C	10	years
		105°C	10	
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Thermal Resistance

Table 17: Thermal Resistance Specifications

Parameter	Description	Test Conditions	48 Ball FBGA (16Mb)	48 Ball FBGA (32Mb)	48 Ball FBGA (64Mb)	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	42.67	45.45	45.45	°C/W
θ_{JC}	Thermal resistance (junction to case)		9.81	9.81	9.81	

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

2: Ambient temperature, T_A 25 ℃

3: Worst case Junction temp specified for Top die (θ_{JA}) and Bottom die (θ_{JC})

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Revision History

Revision	Date	Change Summary
REV U	4/01/2022	Updated Thermal Resistance Specification by removing TSOP package Removed Preliminary.
	5/09/2022	Corrected Table 6 : V_{CC} Power Up to First Instruction = 1ms
	5/18/2022	Fixed Spelling Mistake