Space-Grade High Performance Dual-Quad Serial Persistent SRAM Memory

(AS301G208, AS302G208, AS304G208, AS308G208)

Features

- Interface
  - Dual Quad SPI – support 8-bit wide transfer
    - Dual QPI (4-4-4) – up to 54MHz SDR
    - Dual QPI (4-4-4) – up to 40MHz DDR
- Technology
  - 22nm pMTJ STT-MRAM
    - Data Endurance: 10^{16} write cycles
    - Data Retention: 20 years @ 85°C
- Density
  - 1Gb, 2Gb, 4Gb, 8Gb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.0V, 3.3V ***
- Operating Temperature Range
  - Industrial Extended: -40°C to 125°C
- Packages
  - 96/224-ball FBGA (20mm x 20mm)
- Data Protection
  - Hardware Based
    - Dedicated Hardware Signals (HBP0, HBP1, HBP2) in conjunction with Top/Bottom Select Signal (HTBSEL)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- 48-hour burn-in at 125°C
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

* Leaded Balls available

** PEMS-INST-001 Flow available as custom option through partners

*** V_{CCIO} can be set to any voltage within the following range: 1.71V – 3.60V

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General Description

ASxxxx208 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in density ranging from 1Gbit to 8Gbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @85°C.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

ASxxxx208 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

ASxxxx208 connects two Quad SPI devices with dual-CS#, providing an eight bit I/O data path. Each device can be configured and operate independently with its own register sets, managing by a sperate CS#.

ASxxxx208 is available in an 96-ball FBGA package. The package has separate balls for CS1#, CLK1#, and INT1 (Dual-Quad SPI device 1) and CS2#, CLK2#, and INT2 (Dual-Quad SPI device 2). This package is compatible with similar low-power volatile and non-volatile products.

Table 2: Multi-Die Package Density

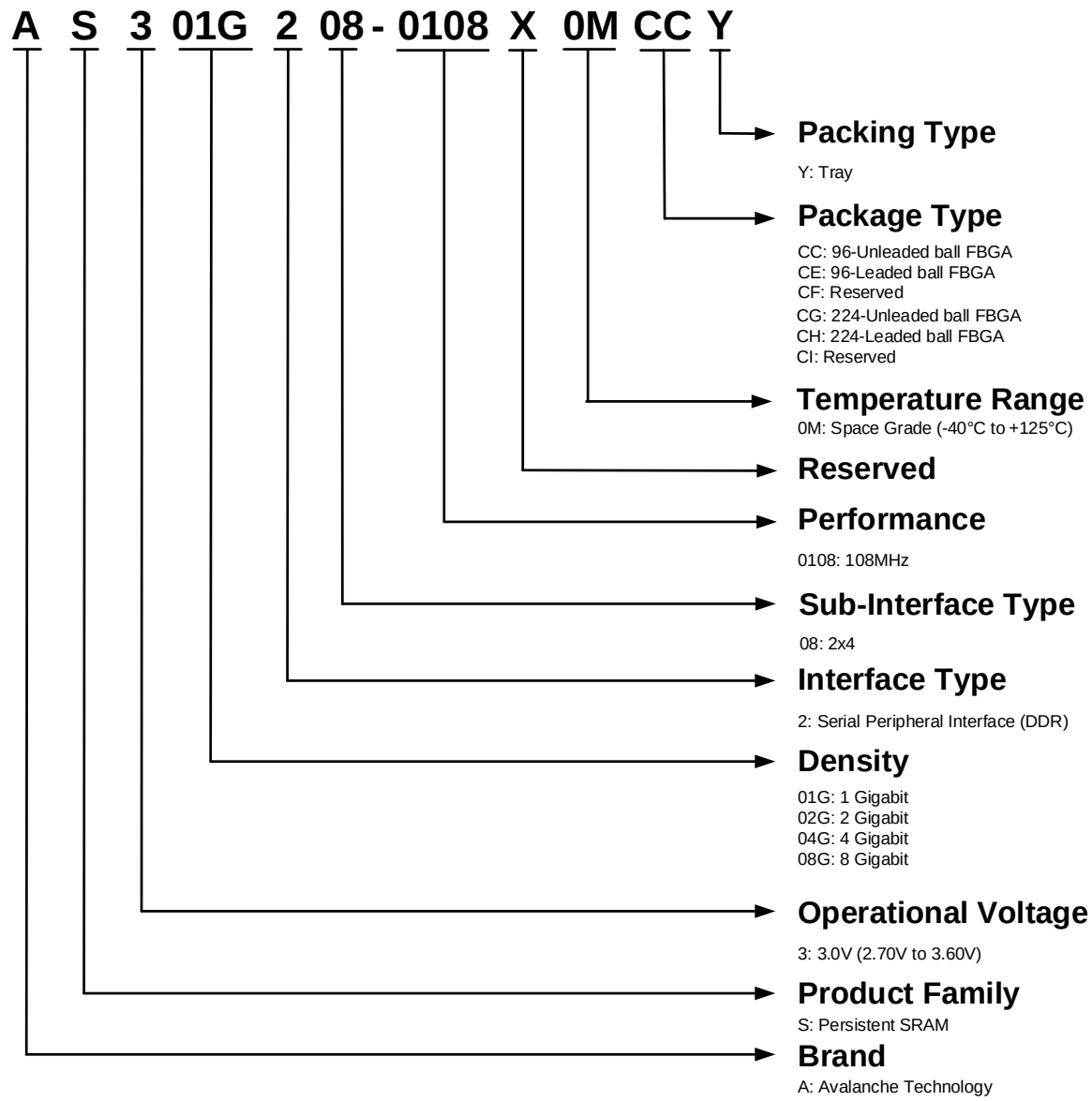
Density	512Mb Die	1Gb Die
1Gb	x2	-
2Gb	-	x2
4Gb	-	x4
8Gb	-	x8

ASxxxx208 is offered with industrial extended (-40°C to 125°C) operating temperature ranges: this is measured as the junction temperature.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Ordering Options



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 3: Valid Combinations List

Valid Combinations – 108MHz				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS301G208-0108X	0M	CC	Y	AS301G208-0108X0MCCY
AS302G208-0108X	0M	CC	Y	AS302G208-0108X0MCCY
AS304G208-0108X	0M	CC	Y	AS304G208-0108X0MCCY
AS308G208-0108X	0M	CC	Y	AS308G208-0108X0MCCY
AS301G208-0108X	0M	CE	Y	AS301G208-0108X0MCEY
AS302G208-0108X	0M	CE	Y	AS302G208-0108X0MCEY
AS304G208-0108X	0M	CE	Y	AS304G208-0108X0MCEY
AS308G208-0108X	0M	CE	Y	AS308G208-0108X0MCEY
AS301G208-0108X	0M	CG	Y	AS301G208-0108X0MCGY
AS302G208-0108X	0M	CG	Y	AS302G208-0108X0MCGY
AS304G208-0108X	0M	CG	Y	AS304G208-0108X0MCGY
AS308G208-0108X	0M	CG	Y	AS308G208-0108X0MCGY
AS301G208-0108X	0M	CH	Y	AS301G208-0108X0MCHY
AS302G208-0108X	0M	CH	Y	AS302G208-0108X0MCHY
AS304G208-0108X	0M	CH	Y	AS304G208-0108X0MCHY
AS308G208-0108X	0M	CH	Y	AS308G208-0108X0MCHY

Signal Description and Assignment

Figure 2: Device Pinout

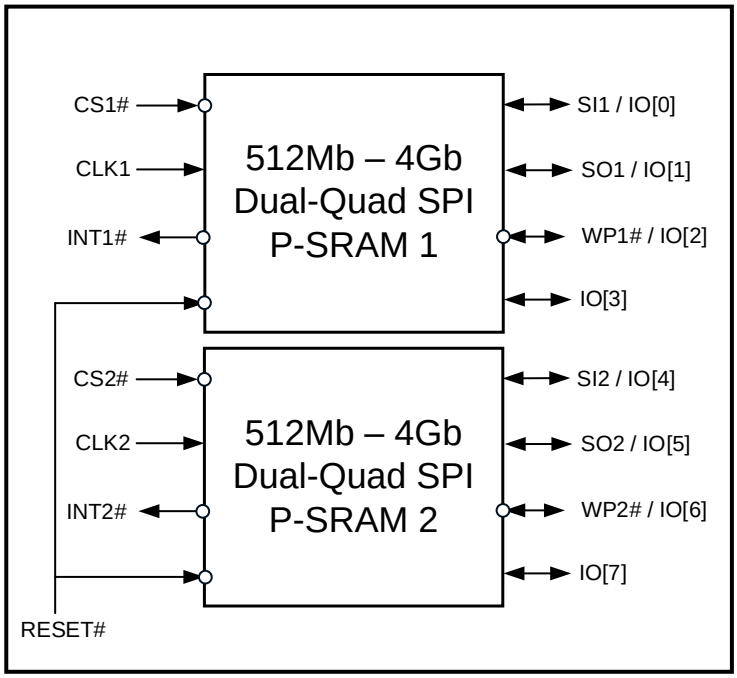


Figure 3: Single CS# System Block Diagram

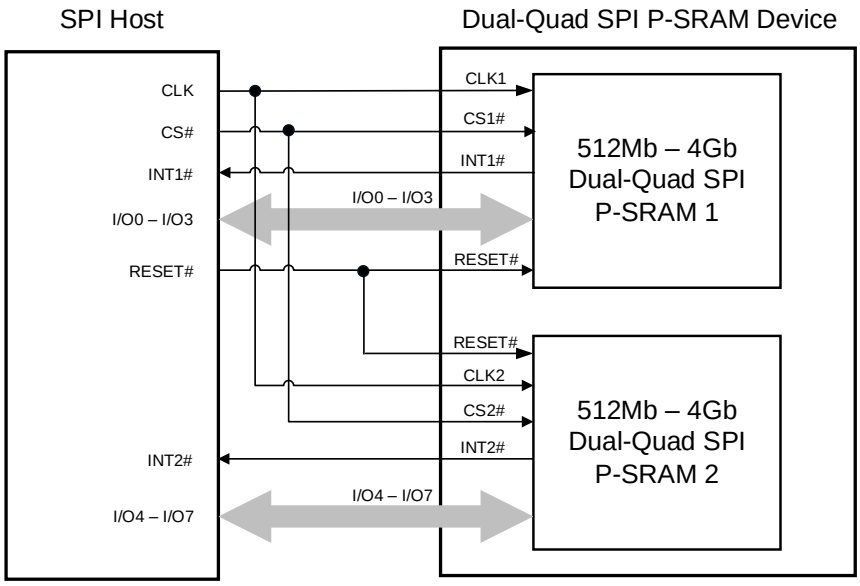


Figure 4: Dual-CS# System Block Diagram

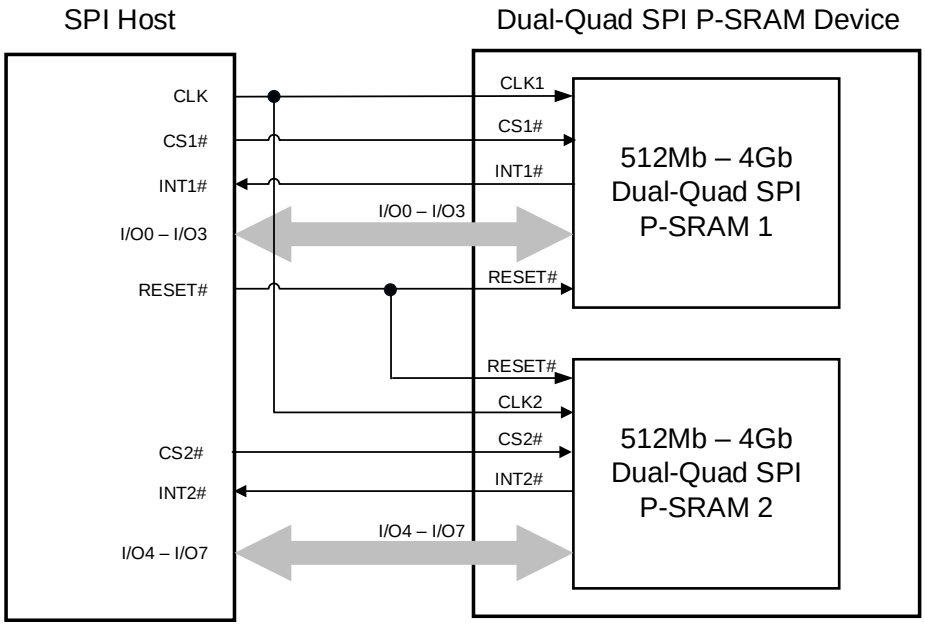


Table 4: Signal Description for 96-Ball FPGA Package

Signal	Ball Assignment	Type	Description
CS1#	L7	Input	**Chip Select 1:** When CS1# is driven High, the Quad SPI device 1 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
CLK1	K7	Input	**Clock 1:** Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT1#	J10	Output	**Interrupt 1:** Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI1	M8	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode.
IO[0]		Bidirectional	**Bidirectional Data 0 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
SO1	M7	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 1 on the falling edge of the clock in Single SPI mode.

Signal	Ball Assignment	Type	Description
IO[1]		Bidirectional	**Bidirectional Data 1 (QPI):** The bidirectional I/O that transfers data into and out of device 1 in Quad SPI mode.
WP1#	L9	Input	**Write Protect 1 (SPI):** Write protects the status register of device 1 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[2]		Bidirectional	**Bidirectional Data 2 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
IO[3]	M9	Bidirectional	**Bidirectional Data 3 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode. This pin can be tied to Vcc if not used.
CS2#	J8	Input	**Chip Select 2:** When CS2# is driven High, the Quad SPI device 2 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS2# Low enables device 2, placing it in the active mode. After power-up, a falling edge on CS2# is required prior to the start of any instructions.
CLK2	K6	Input	**Clock 2:** Provides the timing for device 2 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT2#	K8	Output	**Interrupt 2:** Output generated by device 2 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI2	M10	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode.
IO[4]		Bidirectional	**Bidirectional Data 4 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
SO2	N8	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 2 on the falling edge of the clock in Single SPI mode.
IO[5]		Bidirectional	**Bidirectional Data 5 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
WP2#	N7	Input	**Write Protect 2 (SPI):** Write protects the status register of device 2 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[6]		Bidirectional	**Bidirectional Data 6 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.

Signal	Ball Assignment	Type	Description
IO[7]	N6	Bidirectional	**Bidirectional Data 7 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
RESET#	J9	Input	**RESET:** This is a RESET# signal. When this signal is driven high, the device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z.
HBP[0:2]	G10, G11, H12	Input	**HPB0, HBP1, HBP2:** these Hardware Block Protect signals, when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions: These balls have a Pull down to Vss. If left disconnected they will be seen by device as “Low”.
HTBSEL	J12	Input	**HTBSEL:** this signal when driven High or Low, is used in conjunction with the Hardware Block Protect Pins (HBP0, HBP1, and HBP2) determines if the write-protected memory area defined by the state of the HBP pins, starts from the top or the bottom of the memory array: This ball have a Pull down to Vss. If left disconnected it will be seen by device as “Low”.
V_{CCIO}	G4, P4, G5, J5, P5, M6, H7, H9, N9, J11, M11, G12, P12	Supply	I/O power supply.
V_{SSIO}	M5, H6, L6, P8, H10, N10, P10, H11, N11	Supply	I/O ground supply.
V_{CC}	K4, M4, K5, G7, P7, G9, K9, P9, K11, K12, M12	Supply	Core power supply.
V_{SS}	A1, B1, W1, Y1, A2, Y2, F3, G3, P3, R3, F4, H4, J4, L4, N4, R4, L5, N5, G6, P6, G8, H8, L10, L11, P11, F12, L12, N12, R12, F13, G13, P13, R13, A14, Y14, A15, B15, W15, Y15	Supply	Core ground supply.
DNU	H5, J6, J7, L8, K10	-	**Do Not Use:** DNUs must be left unconnected, floating.

Table 5: Signal Description for 224-Ball FPGA Package

Signal	Ball Assignment	Type	Description
CS1#	L9	Input	**Chip Select 1:** When CS1# is driven High, the Quad SPI device 1 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
CLK1	K9	Input	**Clock 1:** Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT1#	J12	Output	**Interrupt 1:** Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI1	M10	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode.
IO[0]		Bidirectional	**Bidirectional Data 0 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
SO1	M9	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 1 on the falling edge of the clock in Single SPI mode.
IO[1]		Bidirectional	**Bidirectional Data 1 (QPI):** The bidirectional I/O that transfers data into and out of device 1 in Quad SPI mode.
WP1#	L11	Input	**Write Protect 1 (SPI):** Write protects the status register of device 1 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[2]		Bidirectional	**Bidirectional Data 2 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
IO[3]	M11	Bidirectional	**Bidirectional Data 3 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode. This pin can be tied to Vcc if not used.
CS2#	J10	Input	**Chip Select 2:** When CS2# is driven High, the Quad SPI device 2 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS2# Low enables device 2, placing it in the active mode. After power-up, a falling edge on CS2# is required prior to the start of any instructions.
CLK2	K8	Input	**Clock 2:** Provides the timing for device 2 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock.

Signal	Ball Assignment	Type	Description
			In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT2#	K10	Output	**Interrupt 2:** Output generated by device 2 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI2	M12	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode.
IO[4]		Bidirectional	**Bidirectional Data 4 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
SO2	N10	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 2 on the falling edge of the clock in Single SPI mode.
IO[5]		Bidirectional	**Bidirectional Data 5 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
WP2#	N9	Input	**Write Protect 2 (SPI):** Write protects the status register of device 2 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[6]		Bidirectional	**Bidirectional Data 6 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
IO[7]	N8	Bidirectional	**Bidirectional Data 7 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
RESET#	J11	Input	**RESET:** This is a RESET# signal. When this signal is driven high, the device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z.
HBP[0:2]	G12, G13, H14	Input	**HPB0, HBP1, HBP2:** these Hardware Block Protect signals, when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions: These balls have a Pull down to Vss. If left disconnected they will be seen by device as “Low”.
HTBSEL	J14	Input	**HTBSEL:** this signal when driven High or Low, is used in conjunction with the Hardware Block Protect Pins (HBP0, HBP1, and HBP2) determines if the write-protected memory area defined by the state of the HBP pins, starts from the top or the bottom of the memory array: This ball have a Pull down to Vss. If left disconnected it will be seen by device as “Low”.
V_{CCIO}	G6, P6, G7, J7, P7, M8, H9, H11, N11, J13, M13, G14, P14	Supply	I/O power supply.
V_{SSIO}	M7, H8, L8, P10, H12, N12, P12, H13, N13	Supply	I/O ground supply.
V_{CC}	K6, M6, K7, G9, P9, G11, K11,	Supply	Core power supply.

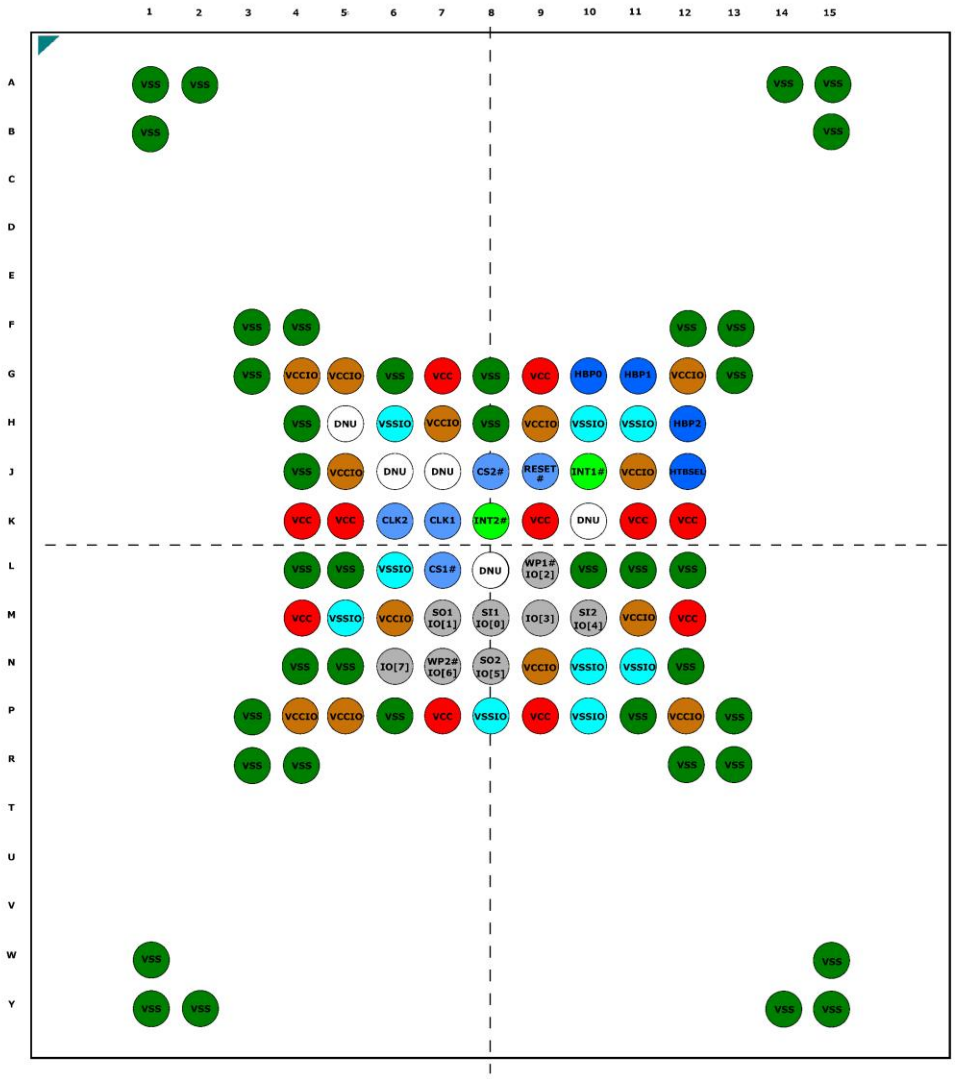
Signal	Ball Assignment	Type	Description
	P11, K13, K14, M14		
V_{SS}	A3, B3, W3, Y3, A4, Y4, F5, G5, P5, R5, F6, H6, J6, L6, N6, R6, L7, N7, G8, P8, G10, H10, L12, L13, P13, F14, L14, N14, R14, F15, G15, P15, R15, A16, Y16, A17, B17, W17, Y17	Supply	Core ground supply.
DNU	H7, J8, J9, L10, K12	-	**Do Not Use:** DNUs must be left unconnected, floating.
Dummy	A1,A2,A5,A6, A7,A8,A9,A10,A 11,A12,A13,A14 ,15,A18,A19 , B1,B2,B4,B5,B6 ,B7,B8,B9,B10, B11,B12,B13,B1 4,B15,B16,B18, B19 C1,C2,C18,C19, D1,D2,D18,D19, E1,E2,E18,E19, F1,F2,F18,F19, G1,G2,G18,G19 ,H1,H2,H18,H19 ,J1,J2,J18,J19,K 1,K2,K18,K19,L 1,L2,L18,L19,M 1,M2,M18,M19, N1,N2,N18,N19, P1,P2,P18,P19, R1,R2,R18,R19, T1,T2,T18,T19, U1,U2,U18,U19, V1,V2,V18,V19, W1,W2,W4,W5, W6,W7,W8,W9, W10,W11,W12, W13,W14,W15, W16,W18,W19, Y1,Y2,Y5,Y6,Y7 ,Y8,Y9,Y10,Y11,	Mechanical	**Dummy balls are electrically not connected. ***

Signal	Ball Assignment	Type	Description
	Y12,Y13,Y14,Y15,Y18,Y19		

Package Options

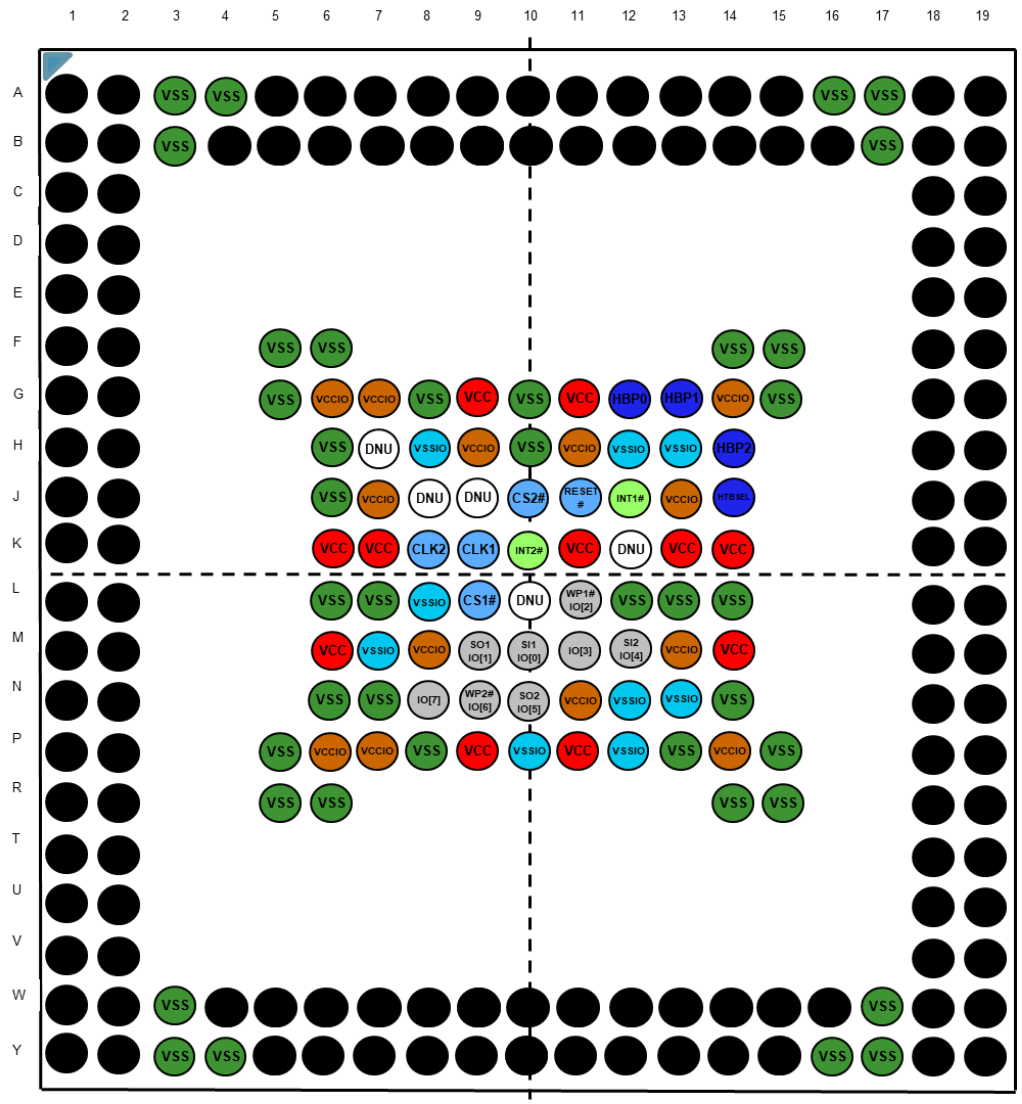
96-ball FBGA (Balls Down, Top View)

Figure 5: 96-ball FBGA



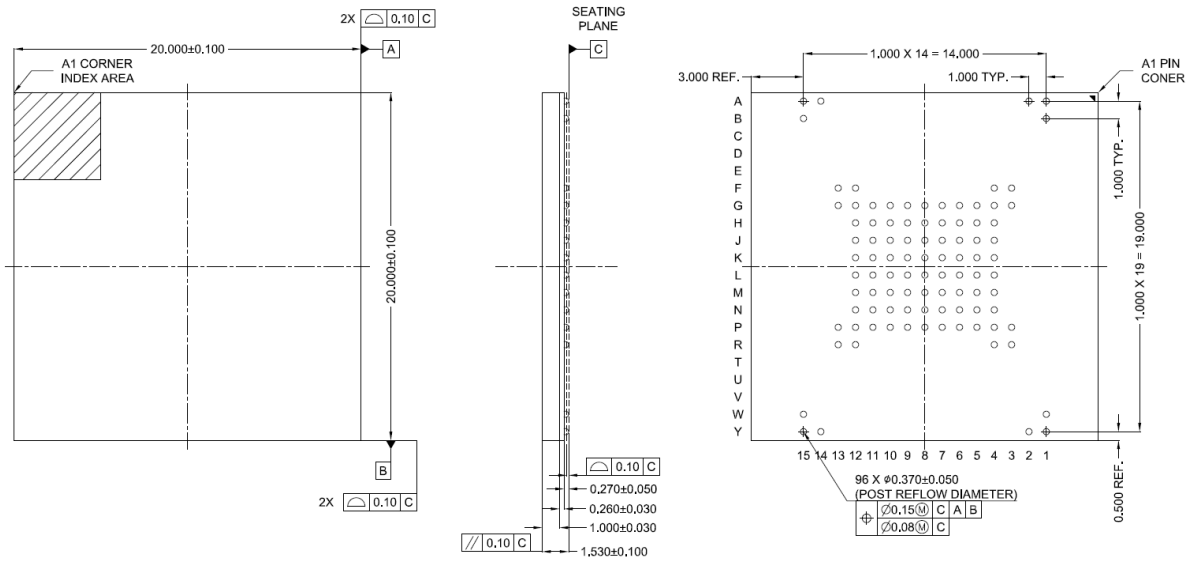
224-ball FBGA (Balls Down, Top View)

Figure 6: 224-ball FBGA



Package Drawings

Figure 7: 96-ball FBGA

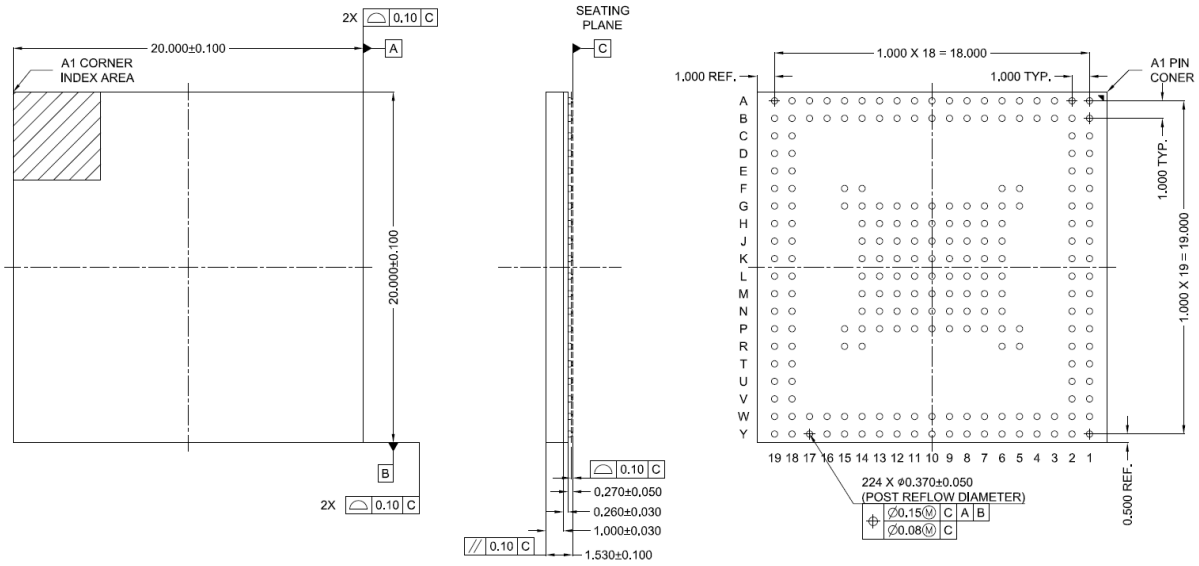


TOP VIEW SIDE VIEW BOTTOM VIEW

[NOTES]

1. RAW SOLDER BALL SIZE IS 0.350
2. SRO SIZE IS 0.300

Figure 8: 224-ball FBGA



TOP VIEW SIDE VIEW BOTTOM VIEW

[Notes]

1. RAW SOLDER BALL SIZE IS 0.350

2. SRO SIZE IS 0.300

Architecture

ASxxxx208 is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running up to 54MHz (QPI) DDR mode or 108MHz (QPI) SDR mode, eXecute-In-Place (XIP) functionality, and hardware/software-based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

ASxxxx208 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. In Single SPI mode, the device is accessed via the SI / IO[0] pin of a Dual-Quad SPI 1 and the SI / IO[4] pin of a Dual-Quad SPI 2. In Quad mode, the IO[0:3] of a Dual-Quad SPI 1 and the IO[4:7] of a Dual-Quad SPI 2 are used respectively to access the device (consult Figure 2 & Figure 3). Furthermore, Single Data Rate (SDR) and Double Data Rate (DDR) instructions utilize CLK edges differently to transfer information; SDR uses a single CLK edge whereas DDR uses both edges of CLK. ***Table 6 & Table 7*** summarizes all the different interface modes supported and their respective I/O usage. ***Table 8*** shows the clock edge used for each instruction component.

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0]] or SO / IO[1]) of a Dual-Quad SPI 1 and (SI / IO[4]] or SO / IO[5]) of a Dual-Quad SPI 2. On the other hand, 4-4-4 represents command, address and data being sent on eight I/Os: (IO[3:0]) of a Dual-Quad SPI 1 and (IO[7:4]) of a Dual-Quad SPI 2 (consult Figure 2 & Figure 3).

All AC timings and waveforms and DC specification are defined in the datasheet using single CS# (Chip Select) and CLK (Serial Clock) signals.

Table 6: Interface Modes of Operations – Device 1

Instruction Component	Single SPI (1-1-1)	Quad Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[0]	SI / IO[0]	SI / IO[0]	IO[3:0]
Address	SI / IO[0]	IO[0]	IO[3:0]	IO[3:0]
Data Input	SI / IO[0]	IO[3:0]	IO[3:0]	IO[3:0]
Data Output	SO / IO[1]	IO[3:0]	IO[3:0]	IO[3:0]

Table 7: Interface Modes of Operations – Device 2

Instruction Component	Single SPI (1-1-1)	Quad Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[4]	SI / IO[4]	SI / IO[4]	IO[7:4]
Address	SI / IO[4]	IO[4]	IO[7:4]	IO[7:4]
Data Input	SI / IO[4]	IO[7:4]	IO[7:4]	IO[7:4]
Data Output	SO / IO[5]	IO[7:4]	IO[7:4]	IO[7:4]

Table 8: Clock Edge Used for instructions in SDR and DDR modes

Instruction Type	Command	Address	Data Input	Data Output
(1-1-1) SDR	R	R	R	F 1
(1-1-1) DDR	R	R F	R F	F R 1
(1-4-4) SDR	R	R	R	F 1
(1-4-4) DDR	R	R F	R F	F R 1
(4-4-4) SDR	R	R	R	F 1
(4-4-4) DDR	R	R F	R F	F R 1

Notes:
R: Rising Clock Edge
F: Falling Clock Edge
1: Data output from ASxxxx208 always begins on the falling edge of the clock – SDR & DDR

ASxxxx208 supports eXecute-In-Place (XIP) which allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. Thus, XIP mode saves command overhead and reduces random read & write access time. A special XIP byte must be entered after the address bits to enable/disable (Axh/Fxh) XIP.

ASxxxx208 offers both hardware and software-based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

Figure 9: Functional Block Diagram – Dual QSPI Device 1

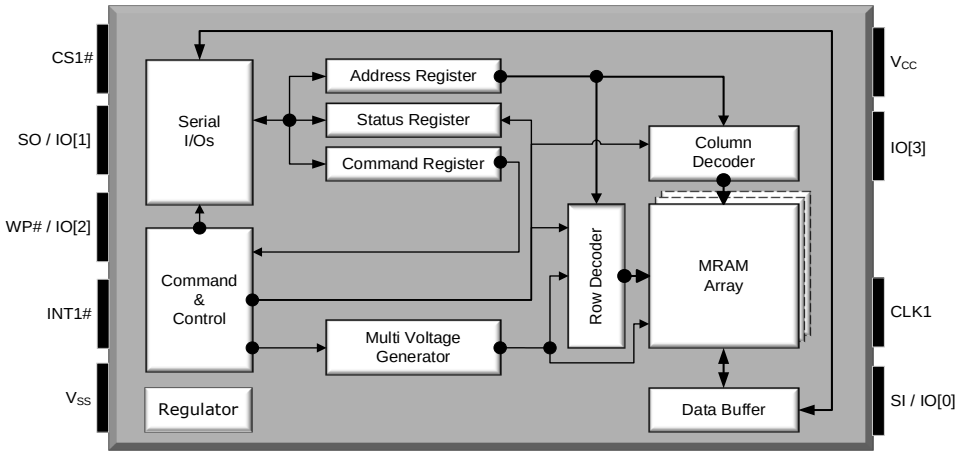


Figure 10: Functional Block Diagram – Dual QSPI Device 2

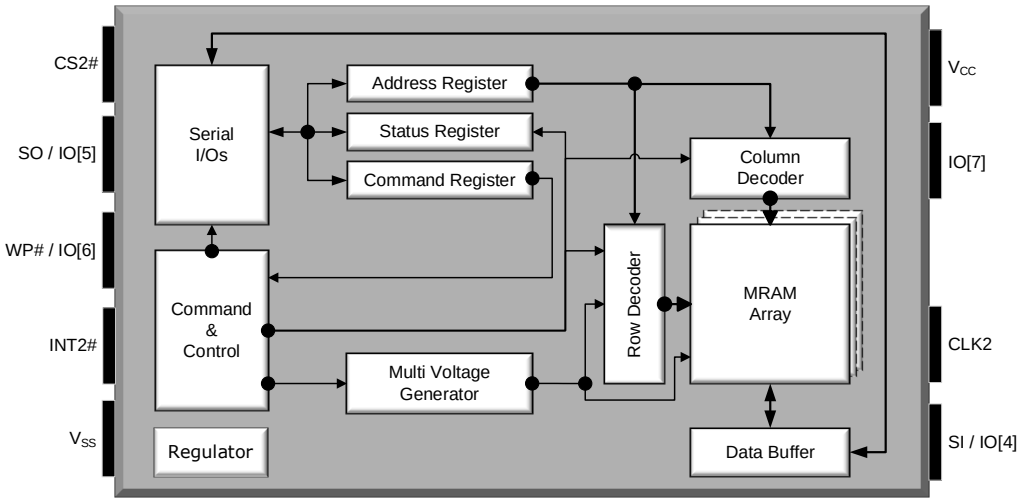


Table 9: Modes of Operation – Device 1

Mode	Current	CS#	CLK	SI / IO[3:0]	SO / IO[3:0]
Standby	I_{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I_{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I_{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z

Notes:
H: High (Logic '1')
L: Low (Logic '0')
Hi-Z: High Impedance

Table 10: Modes of Operation – Device 2

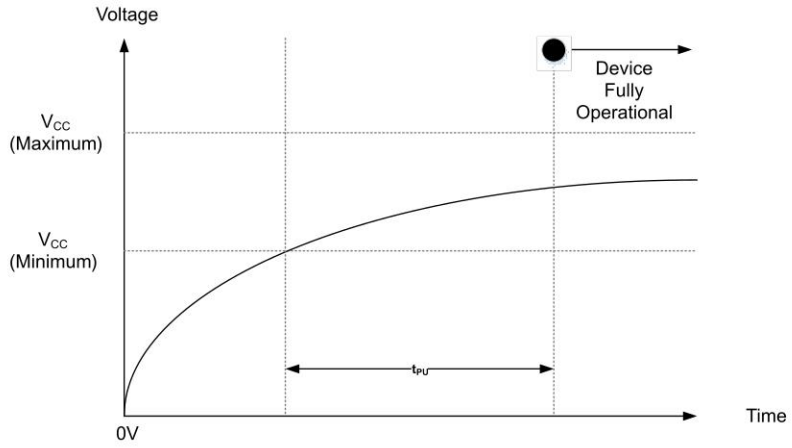
Mode	Current	CS#	CLK	SI / IO[7:4]	SO / IO[7:4]
Standby	I_{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I_{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I_{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- V_{CC} and V_{CCIO} can ramp up together (R_{VR}), if not possible then V_{CC} first followed by V_{CCIO}. The maximum difference between the two voltages should not exceed 0.7V before reaching the final value of V_{CCIO}.
- The device must not be selected at power-up (a 10KΩ pull-up Resistor to V_{CCIO} on CS# is recommended). Then a further delay of t_{PU} (Figure 11) until V_{CC} reaches V_{CC}(minimum) .
- During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences (Figure 11).

Figure 11: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- V_{CC} and V_{CCIO} can ramp down together (R_{VF}), if not possible then V_{CC} first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-down (a 10KΩ pull-up Resistor to V_{CCIO} on CS# is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, when V_{CC} goes below $V_{CC\text{-}CUTOFF}$. The voltage must be dropped below V_{CC}(Reset) for a period of t_{PD}. The power-up timing needs to be observed after V_{CC} goes above V_{CC} (minimum)

Figure 12: Power-Down Behavior

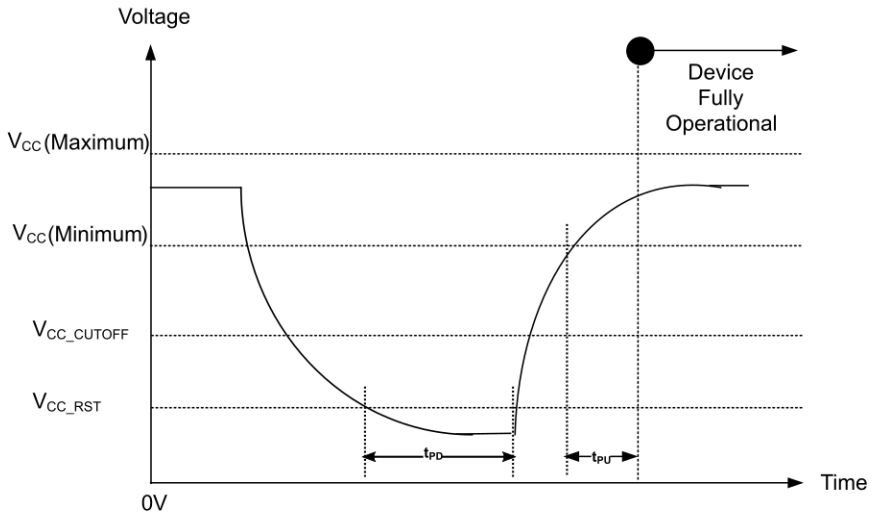


Table 11: Power Up/Down Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		25	-	-	ms
V_{CC} (low) time	t_{PD}		1			ms
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} (Reset)	V_{CC_RST}		0		0.3	V

The following procedure is required to power down the device correctly:

- It is recommended to power down all supplies together. If not possible then the following sequence must be followed 1-V_{CC}, 2-V_{CCIO}.
- Timing for Ramp down rate should follow ramp down time (R_{VF}).
- CS# cannot be active during power-down (a 10KΩ pull-up Resistor to V_{CCIO} is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, if V_{CC} goes below $V_{CC\text{-}CUTOFF}$. All supply voltages V_{CC} and V_{CCIO} must be dropped below their respective (RESET) values V_{CC_RST} for a period of t_{PD}. Figure-12 timing needs to be observed for the subsequence power-up.

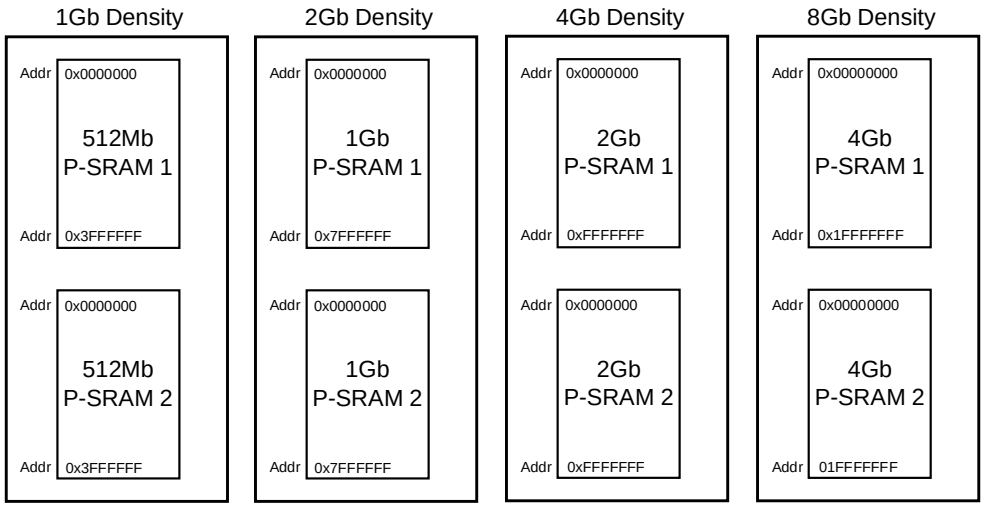
Memory Map

Table 12: Memory Map

Device Density	Address Range	32-bit Address [31:0]	
512Mb	0000000h – 3FFFFFFh	[31:26] - Logic '0'	[25:0] - Addressable
1Gb	0000000h – 7FFFFFFh	[31:27] - Logic '0'	[26:0] - Addressable
2Gb	0000000h – FFFFFFFh	[31:28] - Logic '0'	[27:0] - Addressable
4Gb	000000h – 1FFFFFFFh	[31:29] - Logic '0'	[28:0] - Addressable

Address Range

Figure 13: Address Range



Read any Register Addresses

Table 13: Register Addresses

Register Name	Address
Status Register	0x000000
Interrupt Status Register	0x000001
Configuration Register 1	0x000002
Configuration Register 2	0x000003
Interrupt Configuration Register	0x000004
ECC Test – Data Input Register	0x000005
ECC Test – Error Injection Register	0x000006
ECC Test – Data Output Register	0x000007
ECC Test – Error Count Register	0x000008
Extended Address Register	0x000009
Flag Status Register	0x00000Ah
Device Identification Register	0x000030

Hardware Block Protection

The Hardware Block Protect signals (HBP0, HBP1, and HBP2), when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions. When one or more HBP signals are driven High, the relevant memory area, as defined in Table 14 and Table 15 below, becomes protected against all Write memory array instructions. When all three signals, HBP0, HBP1, and HBP2 are driven Low, the memory array is in normal operation without being write-protected.

The Hardware Top/Bottom Select signal (HTBSEL), when driven High or Low, is used in conjunction with the Hardware Block Protect signals (HBP0, HBP1, and HBP2) to determine if the write-protected memory area defined by the state of the HBP signals, starts from the top or the bottom of the memory array:

- When the HTBSEL signal is driven Low, the memory area, protected by the HBP signals, starts from the top of the memory array.
- When the HTBSEL signal is driven High, the memory area, protected by the HBP signals, starts from the bottom of the memory array.

These pins have an internal pull down to Vss. If the pins are left unconnected, the device will have no hardware protection and all regions of the device can be written to (unless the Software Block Protection is activated through the Status Register).

Table 14: Hardware Top Block Protection Address Range Selection (HTBSEL Signal = L)

HBP [2]	HBP [1]	HBP [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
L	L	L	None	None	None	None	None
L	L	H	Upper 1/64	3F00000h – 3FFFFFFh	7E00000h – 7FFFFFFh	FC00000h – FFFFFFFh	1F800000h – 1FFFFFFFh
L	H	L	Upper 1/32	3E00000h – 3FFFFFFh	7C00000h – 7FFFFFFh	F800000h – FFFFFFFh	1F000000h – 1FFFFFFFh
L	H	H	Upper 1/16	3C00000h – 3FFFFFFh	7800000h – 7FFFFFFh	F000000h – FFFFFFFh	1E000000h – 1FFFFFFFh
H	L	L	Upper 1/8	3800000h – 3FFFFFFh	7000000h – 7FFFFFFh	E000000h – FFFFFFFh	1C000000h – 1FFFFFFFh
H	L	H	Upper 1/4	3000000h – 3FFFFFFh	6000000h – 7FFFFFFh	C000000h – FFFFFFFh	18000000h – 1FFFFFFFh
H	H	L	Upper 1/2	2000000h – 3FFFFFFh	4000000h – 7FFFFFFh	8000000h – FFFFFFFh	10000000h – 1FFFFFFFh
H	H	H	All	0000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Table 15: Hardware Bottom Block Protection Address Range Selection (HTBSEL Signal = H)

HBP [2]	HBP [1]	HBP [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
L	L	L	None	None	None	None	None
L	L	H	Lower 1/64	000000h – 0FFFFFh	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh
L	H	L	Lower 1/32	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh

HBP [2]	HBP [1]	HBP [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
L	**H**	**H**	Lower 1/16	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh
H	**L**	**L**	Lower 1/8	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh
H	**L**	**H**	Lower 1/4	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh
H	**H**	**L**	Lower 1/2	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh
H	**H**	**H**	All	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Notes:
High (H): Logic '1'
Low (L): Logic '0'

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

The WREN bit must be set to "1" to enable write operations. This bit can only be set by executing the Write Enable (WREN) instruction opcode.

The device supports Back-to-Back write operations: WREN is prerequisite to only the first Memory Array Write instruction. The WREN bit doesn't clear to "0" following subsequent memory write opcodes. WREN disable instruction must be executed to reset WREN.

Table 16 : Status Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – unprotected
SR[6]	RSVD	Reserved	R	0	Reserved for future use
SR[5]	TBPSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits (Table 17, Table 18)
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Protection Enable/Disable	R	0	1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Software Block Protection

These 4 bits are OR'ed with the Hardware Protection Bits and can be used to dynamically protect regions of memory.

Table 17: Software Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
0	**0**	**0**	None	None	None	None	None
0	**0**	**1**	Upper 1/64	3F00000h – 3FFFFFFh	7E00000h – 7FFFFFFh	FC00000h – FFFFFFFh	1F800000h – 1FFFFFFFh
0	**1**	**0**	Upper 1/32	3E00000h – 3FFFFFFh	7C00000h – 7FFFFFFh	F800000h – FFFFFFFh	1F000000h – 1FFFFFFFh
0	**1**	**1**	Upper 1/16	3C00000h – 3FFFFFFh	7800000h – 7FFFFFFh	F000000h – FFFFFFFh	1E000000h – 1FFFFFFFh
1	**0**	**0**	Upper 1/8	3800000h – 3FFFFFFh	7000000h – 7FFFFFFh	E000000h – FFFFFFFh	1C000000h – 1FFFFFFFh
1	**0**	**1**	Upper 1/4	3000000h – 3FFFFFFh	6000000h – 7FFFFFFh	C000000h – FFFFFFFh	18000000h – 1FFFFFFFh
1	**1**	**0**	Upper 1/2	2000000h – 3FFFFFFh	4000000h – 7FFFFFFh	8000000h – FFFFFFFh	10000000h – 1FFFFFFFh
1	**1**	**1**	All	0000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Table 18: Software Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	512Mb	1Gb	2Gb	4Gb
0	**0**	**0**	None	None	None	None	None
0	**0**	**1**	Lower 1/64	000000h – 0FFFFFh	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh
0	**1**	**0**	Lower 1/32	000000h – 01FFFFFh	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh
0	**1**	**1**	Lower 1/16	000000h – 03FFFFFh	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh
1	**0**	**0**	Lower 1/8	000000h – 07FFFFFh	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh
1	**0**	**1**	Lower 1/4	000000h – 0FFFFFFh	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh
1	**1**	**0**	Lower 1/2	000000h – 1FFFFFFh	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh
1	**1**	**1**	All	000000h – 3FFFFFFh	000000h – 7FFFFFFh	000000h – FFFFFFFh	0000000h – 1FFFFFFFh

Table 19: Software Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status & Configuration Registers	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	**X**	**X**	Protected	Protected	Protected
1	**0**	**X**	Unprotected	Protected	Unprotected
1	**1**	**Low**	Protected	Protected	Unprotected
1	**1**	**High**	Unprotected	Protected	Unprotected

Notes:
High: Logic '1'
Low: Logic '0'
X: Don't Care – Can be Logic '0' or '1'
Protected: Write protected
Unprotected: Writable
Note 1: Memory address range protection based on Block Protection Bits

Extended Address Register (Read/Write)

For the 3-byte addressing mode, the extended address register provides a fourth address byte A[31:24] to enable the host to access memory area beyond 128Mb. The extended address register bits [4:0] operate as memory address bit A[24:28] to select one of thirty two 128Mb segments of the memory array.

The value of the extended address register does not change when a 3-byte read operation crosses the selected 128Mb boundary.

Table 20: Extended Address Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
[7:5]	A[31:29]	Reserved	R/W	00000000	000
[4:0]	A[28:24]	Enables specified 128Mb memory segment Up to 4Gb			11111: 32rd Highest 128Mb segment (1F000000h – 1FFFFFFFh) 11110: 31th 128Mb segment (1E000000h – 1EFFFFFFh) 11101: 30th 128Mb segment (1D000000h – 1DFFFFFFh) 11100: 29th 128Mb segment (1C000000h – 1CFFFFFFh) 10111: 28th 128Mb segment (1B000000h – 1BFFFFFFh) 11010: 27th 128Mb segment (1A000000h – 1AFFFFFFh) 11001: 26th 128Mb segment (19000000h – 19FFFFFFh) 11000: 25th 128Mb segment (18000000h – 18FFFFFFh) 10111: 24th 128Mb segment (17000000h – 17FFFFFFh) 10110: 23th 128Mb segment (16000000h – 16FFFFFFh) 10101: 22th 128Mb segment (15000000h – 15FFFFFFh) 10100: 21th 128Mb segment (14000000h – 14FFFFFFh) 10011: 20th 128Mb segment (13000000h – 13FFFFFFh) 10010: 19th 128Mb segment (12000000h – 12FFFFFFh) 10001: 18th 128Mb segment (11000000h – 11FFFFFFh) 10000: 17th 128Mb segment (10000000h – 10FFFFFFFh) 01111: 16th 128Mb segment (0F000000h – 0FFFFFFFh) 01110: 15th 128Mb segment (0E000000h – 0EFFFFFFh) 01101: 14th 128Mb segment (0D000000h – 0DFFFFFFh) 01100: 13th 128Mb segment (0C000000h – 0CFFFFFFh) 01011: 12th 128Mb segment (0B000000h – 0BFFFFFFh) 01010: 11th 128 Mb segment (0A000000h – 0AFFFFFFh) 01001: 10th 128Mb segment (09000000h – 09FFFFFFh) 01000: 9th 128Mb segment (08000000h – 08FFFFFFh) 00111: 8th 128Mb segment (07000000h – 07FFFFFFh)

Bits	Name	Description	Read / Write	Default State	Selection Options
					00110: 7th 128Mb segment (06000000h – 06FFFFFFh) 00101: 6th 128Mb segment (05000000h – 05FFFFFFh) 00100: 5th 128Mb segment (04000000h - 04FFFFFFh) 00011: 4th 128Mb segment (030000000h – 03FFFFFFh) 00010: 3rd 128Mb segment (02000000h – 02FFFFFFh) 00001: 2nd 128Mb segment (01000000h – 01FFFFFFh) 00000: Lowest 128Mb segment (00000000h – 00FFFFFFh)

Flag Status Register (Read Only)

Flag status register contains device's access status and addressing information.

Table 21: Flag Status Register - Read Only

Bits	Name	Description	Read / Write	Default State	Selection Options
FSR1[7]	ST	Device Access Status	R	1	1: Ready 0: Busy
FSR1[6:1]	RSVD	Reserved	R	0	Reserved for future use
FSR1[0]	RSVD	Reserved	R	0	Reserved for future use

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 22: Device Identification Register – Read Only

Bits	Avalanche Manufacturer's ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temp	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0010-HP Dual-Quad SPI	0001 - 3V	0010 - -40ºC to 125ºC	0110 - Reserved	00000001 - 054MHz
				1000 - 1Gb	
				1001 – 2Gb	
				1010 – 4Gb	
				1100 – 8Gb	

Configuration Register 1 (Read/Write)

Configuration Register 1 (CR1) controls the output drive strength selection, locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register. In addition, CR1 controls the Write Enable protection (WREN – Status Register) reset functionality during memory array writing[1]. This functionality makes SPI MRAM compatible to other SPI devices.

Table 23: Configuration Register 1 (CR1) – Read and Write

Bits	Name	Description	Read / Write	Default	Selection Options
CR1[7]	ODSEL[2]	Output Driver Strength Selector	R/W	0	000: 35Ω 001: 75Ω 010: 60Ω 011: 45Ω 100: 35Ω 101: 40Ω 110: 20Ω 111: 15Ω
CR1[6]	ODSEL[1]			1	
CR1[5]	ODSEL[0]			1	
CR1[4]	RSVD	Reserved	R	0	Reserved for future use
CR1[3]	RSVD	Reserved	R	0	Reserved for future use
CR1[2]	MAPLK	Status Register Lock Enable/Disable (TBSEL, BPSEL[2:0]	R/W	0	1: Lock TBSEL and BPSEL[2:0] 0: Unlock TBSEL and BPSEL[2:0]
CR1[1]	WRENS[1]	WREN Reset Selector (Memory Array Write Functionality)	R/W	0	00: Normal: WREN is prerequisite to all Memory Array Write instruction. (WREN is reset after CS# goes High) 01: SRAM: WREN is not a prerequisite to Memory Array Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset once CS# goes High) 11: Illegal - Reserved for future use
CR1[0]	WRENS[0]			0	

Notes:
1: Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 1 settings. In other words, all register write instructions require WREN to be set and WREN resets once CS# goes High for the write instruction.

Configuration Register 2 (Read/Write)

Configuration Register 2 (CR2) controls the memory array access latency.

Table 24: Configuration Register 2 (CR2) – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR2[7]	RSVD	Reserved	R	0	Reserved for future use
CR2[6]	RSVD	Reserved	R	0	Reserved for future use
CR2[5]	RSVD	Reserved	R	0	Reserved for future use
CR2[4]	RSVD	Reserved	R	0	Reserved for future use
CR2[3]	MLATS[3]	Memory Array Read/Read Any Register Latency Selection [1]	R/W	1	0000: 0 Cycles 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles - Default 1001: 9 Cycle 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	MLATS[2]			0	
CR2[1]	MLATS[1]			0	
CR2[0]	MLATS[0]			0	

Notes:
1: Latency is frequency dependent. Please consult Table 30, 31 and 32

Interrupt Configuration Register (Read/Write)

The Interrupt Configuration Register controls different events that trigger INT# pin transitioning from High to Low state. INT# pin can be configured in the INT# configuration register to transition to the active Low state when either ECC error is detected and corrected or transitioning from the busy to the ready state.

This register also enables access to 1 of 4 die sitting on the internal bus. The ECC engine can be tested be enabling the Test Enable bit and selecting 1 of 4 die.

Table 25: Interrupt Configuration Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
INTCR[7]	INTRF	Shows status of ECC error detection	R	0	Selection Options: 1: Unrecoverable ECC error detected 0: No unrecoverable ECC error detected
INTCR[6]	INTR	Clear Interrupt Status	W	0	Selection Options: 1 = Resets Interrupt caused by unrecoverable ECC 0 = No Action
INTCR[5]	ECC_CR	Reset the ECC Error Count Register	W	0	Selection Options: 1 = Resets ECC count register to 0 0 = No Action
INTCR[4]	----	Reserved	-	-	-
INTCR[3:2]	ECCDS	Die Selection	W	0	Die Select Options: 11 = Die 4 selected 10 = Die 3 selected 01 = Die 2 selected 00 = Die 1 selected
INTCR[1]	ECCTE	ECC Test Enable	W	0	ECC Test Engine Test mode: 1 = Enable 0 = Disable
INTCR[0]	ECCDS	ECC Error Detection Selection	W	0	Selection Options: 1 = ECC detection will transition a High to Low state on the INT# pin 0 = ECC detection will not transition the INT# pin

Error Correction Code (ECC) Test – Data Input Register

The contents of this register are entered into the ECC engine data buffer i.e. used as data input to test the ECC engine.

Table 26: ECC Test Data Input Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_In	Data Input	R/W	32'b0	Any value from 0x00000000 to 0xFFFFFFFF

Error Correction Code (ECC) Test – Error Injection

The contents of this register are used as an error mask to inject error to test the ECC engine.

Table 27: ECC Test Error Injection Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Error_Injection	Error Mask	R/W	32'b0	1 in any position injects an error into ECC engine. For example, 0x00000003 will inject a two-bit error in two LSB bits i.e. the Data in the ECC engine buffer is Exclusive or'd with the error mask.

Error Correction Code (ECC) Test – Data Output Register

The contents of this register are the output of the ECC engine when testing the ECC engine.

Table 28: ECC Test Data Output Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_Out	Output of ECC engine	R	32'b0	None – read only.

Error Correction Code (ECC) – Error Count Register

The Error Count Register is incremented when uncorrectable ECC errors are detected during normal memory operations. An interrupt is generated on device pin INT# and the interrupt flag is set when an unrecoverable error is detected.

Table 29: ECC Count Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	Error_Count	Number of uncorrectable Errors detected	R	32'b0	None – read only

Table 30: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

Read Type	Latency	Max Frequency
(1-1-1) SDR	8-15	54MHz
(1-1-1) DDR	8-15	40MHz
(1-4-4) SDR	8-15	54MHz
(1-4-4) DDR	8-15	40MHz
(4-4-4) SDR	10-15	54MHz
(4-4-4) DDR	8-15	40MHz

Table 31: Memory Read Latency Cycles vs. Maximum Clock Frequency (without XIP)

Read Type	Latency	Max Frequency
(1-1-1) SDR	0	50MHz

Table 32 : Read Any Register Command Latency Cycles vs. Maximum Clock Frequency

Read Type	Latency Cycles	Max Frequency
(1-1-1) SDR	8-15	54MHz
(1-4-4) SDR	8-15	54MHz
(4-4-4) SDR	8-15	54MHz

Instruction Set

Table 33: Instruction Set

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Address Byte	Data Bytes	Max. Frequency	Prerequisite	Note
1	**No Operation**	NOOP 00h	•								•			0		108 MHz		
2	**Write Enable**	WREN 06h	•					•			•			0		108 MHz		
3	**Write Disable**	WRDI 04h	•					•			•			0		108 MHz		
4	**Enable QPI**	QPIE 38h	•		•						•			0		108 MHz		
5	**Enable SPI**	SPIE FFh	•						•		•			0		108 MHz		
6	**Read Status Register**	RDSR 05h		•							•			0	1	54 MHz		
7	**Read Flag Status Register**	RDFSR 70h		•					•			•			1	50 MHz		
8	**Read Device ID**	RDID 9Fh		•							•			0	4	54 MHz		
9	**Read Any Register - Address Based**	RDAR 65h			•				•		•		•	4	1	108 MHz		
10	**Write Status Register**	WRSR 01h		•							•			0	1	108 MHz	WREN	
11	**Write Any Register - Address Based**	WRAR 71h			•				•					4	1	108 MHz	WREN	

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Address Byte	Data Bytes	Max. Frequency	Prerequisite	Note
12	**Read Memory Array - SDR**	READ 03h			•						•			4	1 to ∞	50 MHz		1,2
13	**Read Memory Array - SDR**	READ 13h			•						•			4	1 to ∞	50 MHz		1,2,5
14	**Fast Read Memory Array - SDR**	RDFT 0Bh			•				•		•		•	3	1 to ∞	108 MHz		1,2,3,5
15	**Fast Read Memory Array - SDR**	RDFT 0Ch			•				•		•		•	4	1 to ∞	108 MHz		1,2,3,5
16	**Fast Read Memory Array - DDR**	DRFR 0Dh			•				•	•		•	•	4	1 to ∞	54 MHz		1,2,3
17	**Read Quad Output Memory Read - SDR**	RDQO 6Bh				•					•		•	3	1 to ∞	108 MHz		1,2,3,5
18	**Read Quad Output Memory Read - SDR**	RDQO 6Ch				•					•		•	4	1 to ∞	108 MHz		1,2,3,5
19	**Read Quad I/O Memory Read - SDR**	RDQI EBh					•			•	•		•	4	1 to ∞	108 MHz		1,2,3
20	**Read Quad I/O Memory Read - DDR**	DRQI EDh					•			•		•	•	4	1 to ∞	54 MHz		1,2,3
21	**Write Memory Array - SDR**	WRTE 02h			•				•		•			4	1 to ∞	108 MHz	WREN	1,4
22	**Fast Write Memory Array - SDR**	4WRFT DAh			•				•	•	•			4	1 to ∞	108 MHz	WREN	1,2,4
23	**Fast Write Memory Array - DDR**	4DRFW DEh			•					•		•		4	1 to ∞	54 MHz	WREN	1,2,4
24	**Write Quad I/O Memory Array - SDR**	4WQIO D2h					•			•	•			4	1 to ∞	108 MHz	WREN	1,2,4

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Address Byte	Data Bytes	Max. Frequency	Prerequisite	Note
25	**Write Quad I/O Memory Array - DDR**	4DWQO D1h					•			•		•		4	1 to ∞	54 MHz	WREN	1,2,4

Notes:
1: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O Dual-Quad SPI device 1 (SI / IO[0] or SO / IO[1]) and Dual-Quad SPI device 2 (SI / IO[04 or SO / IO[7]). On the other hand, 1-4-4 represents command being sent on a single I/O Dual-Quad SPI device 1 (SI / IO[0]) and Dual-Quad SPI device 2 (SI / IO[4]) - address/data being sent on four I/Os of Dual-Quad SPI device 1 (IO[3:0]) and Dual-Quad SPI device 2 (IO[7:4])
2: XIP allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. A special mode byte must be entered after the address bits to enable/disable XIP – Axh / Fxh.
3: Fast Read instruction must include Latency cycles to meet higher frequency. They are configurable (Configuration Register 2 – CR2[3:0]) and frequency dependent.
4: WREN prerequisite for array writing is configurable (Configuration Register 1– CR1[1:0])
5. Support legacy device boot on Xilinx platforms

Instruction Description and Structures

All communication between a host and ASxxxx208 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from ASxxxx208. All command, address and data information are transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic'1').
- CLK marks the transfer of each bit.
- Each instruction starts out with an 8-bit command. The command selects the type of operation ASxxxx208 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location or register. The address is 4-byte (32-bit).
    - SDR: The address is transferred on the rising edges of CLK.
    - DDR: The address is transferred on both edges of the CLK in DDR.
- The address bits are followed by data bits. For Write instructions:
    - SDR: Write data bits to ASxxxx208 are transferred on the rising edges of CLK.
    - DDR: Write data bits to ASxxxx208 are transferred on both edges of CLK.
- In normal operational mode, Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction. ASxxxx208 offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array. These modes are set in Configuration Register 1.
- Similar to write instructions, the address bits are followed by data bits for read instructions:
    - SDR: Read data bits from ASxxxx208 are transferred on the falling edges of CLK.
    - DDR: Read data bits from ASxxxx208 are transferred on both edges of CLK. The start of read data transfer is always on the falling edge of the CLK.
- ASxxxx208 is a high-performance serial memory and at higher frequencies, read instructions require latency cycles to compensate for the memory array access time. The number of latency cycles required depends on the operational frequency and is configurable – Configuration Register 2. The latency cycles are inserted after the address bits before the data comes out of ASxxxx208.
- For Read and Write instructions, ASxxxx208 offers XIP mode. XIP allows similar instructions to be executed sequentially without incurring the command cycles overhead. XIP is enabled by entering byte Axh and disabled by entering byte Fxh. These respective bytes must be entered following the address bits.

- The entire memory array can be read from or written to using a single read or write instruction. After the staring address is entered, subsequent address is internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.
- Read Data Strobe (DS) is used as an additional output signal, driven by the MRAM, to synchronize with other data outputs to validate data transition. DS is edge-aligned with output data and is always enabled in the DDR read operation.

Figure 14 to **Figure 22** show the description of SDR instruction types supported.

Figure 14: Description of (1-0-0) Instruction Type

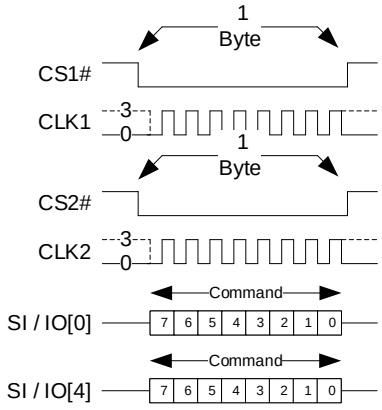


Figure 15: Description of (1-0-1) Instruction Type

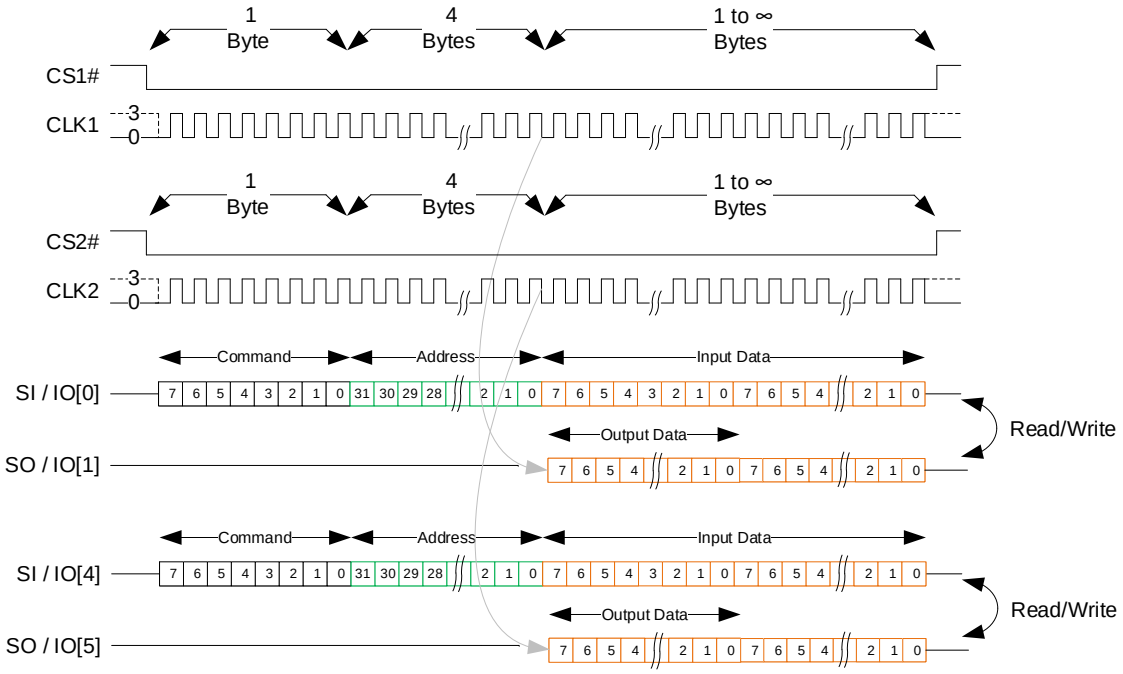


Figure 16: Description of (1-1-1) Instruction Type (Without XIP)

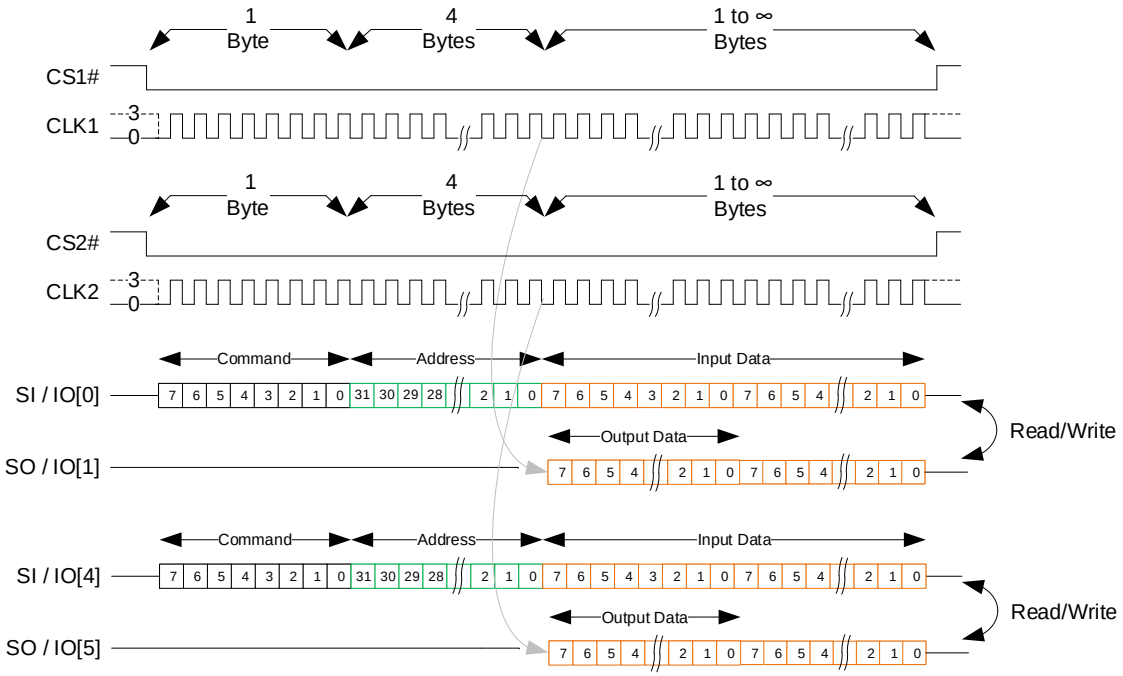


Figure 17: Description of (1-1-1) Instruction Type (With XIP)

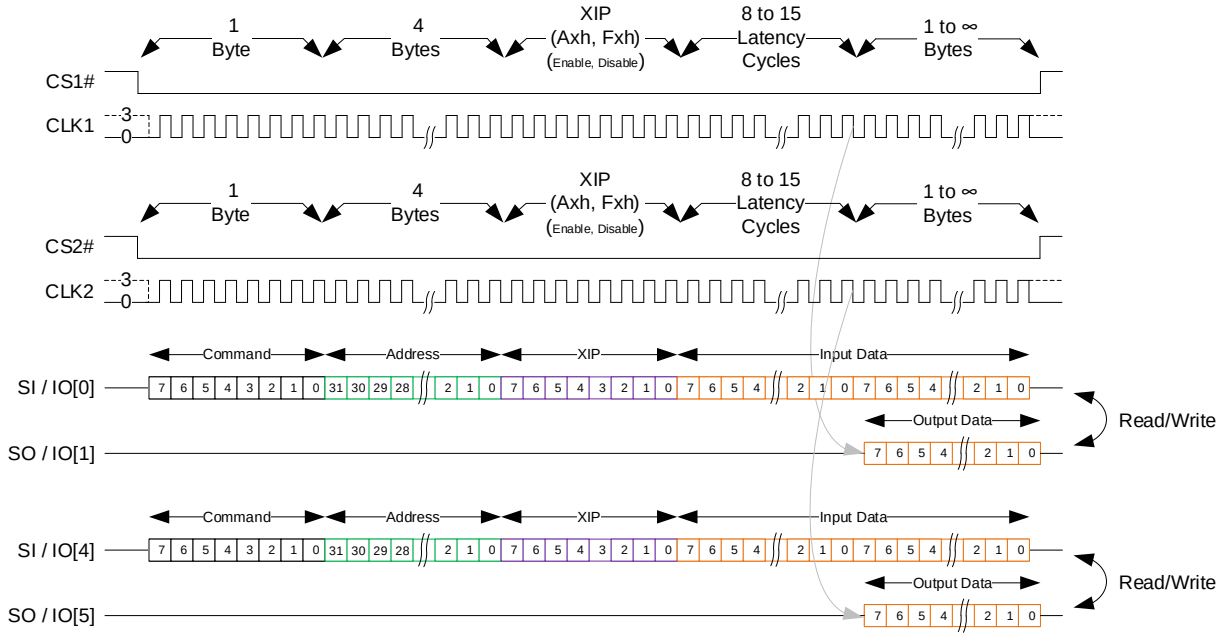


Figure 18: Description of (1-1-1) Instruction Type (Without XIP)

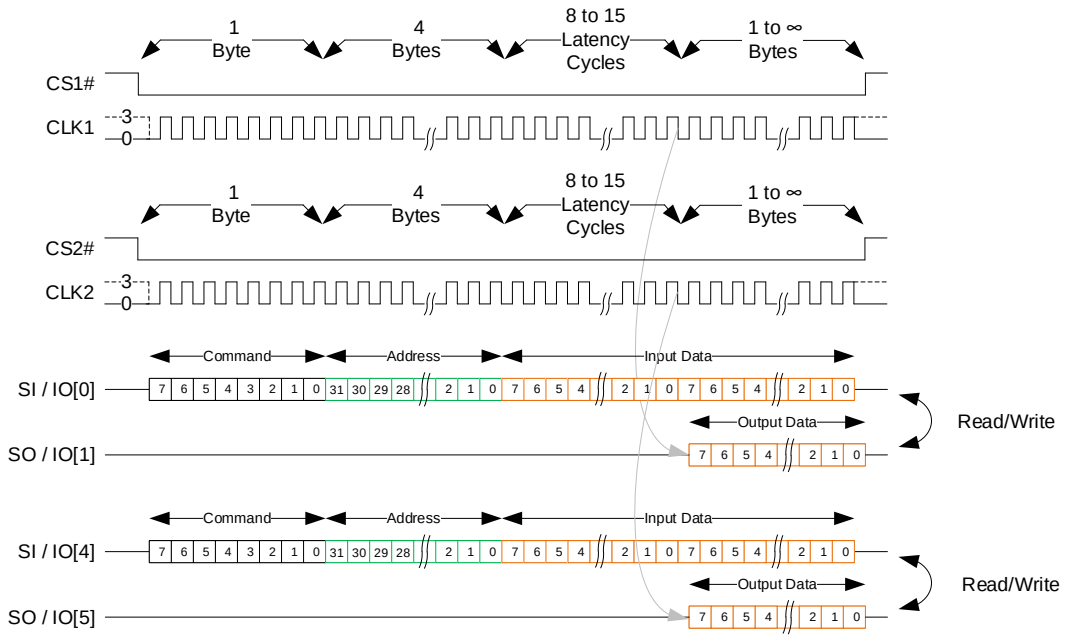


Figure 19: Description of (1-1-4) Instruction Type (Without XIP)

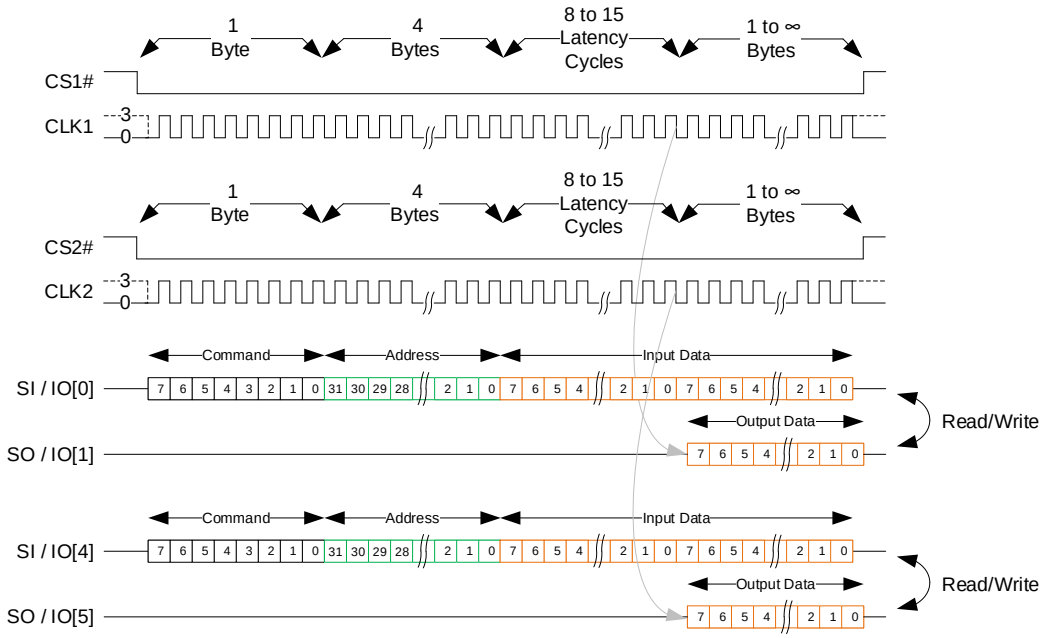


Figure 20: Description of (1-4-4) Instruction Type with XIP

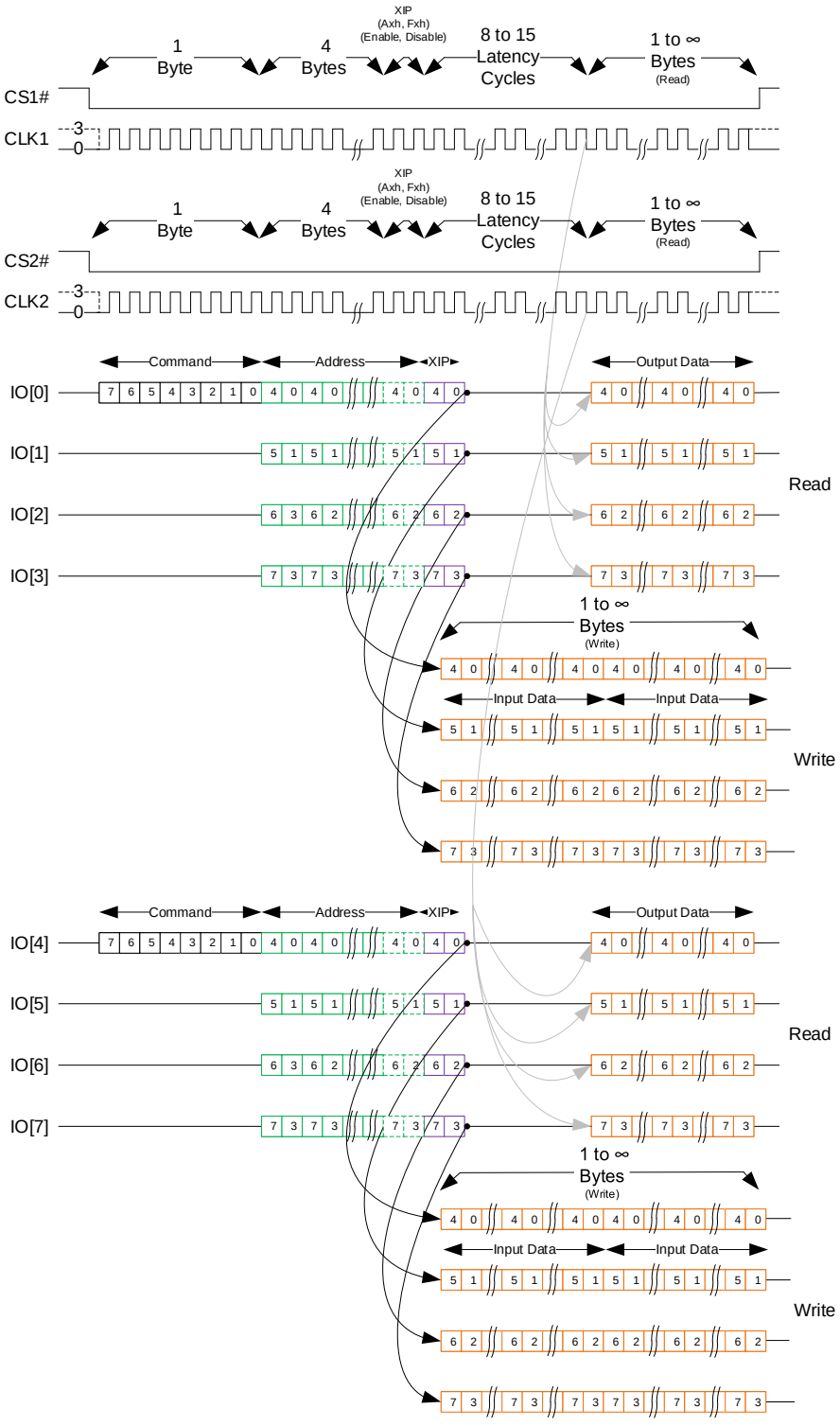


Figure 21: Description of (4-4-4) Instruction Type (Without XIP)

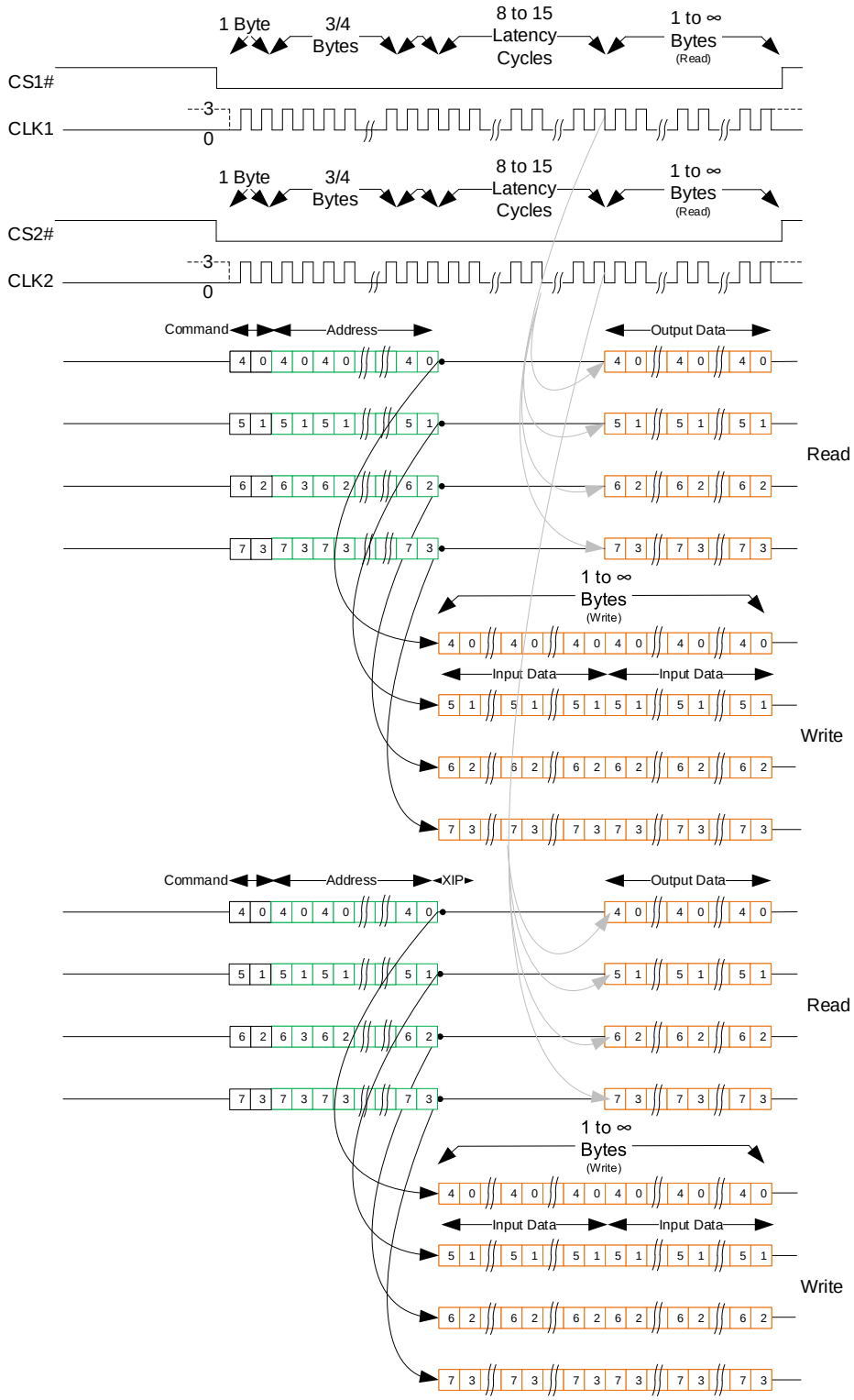


Figure 22: Description of (4-4-4) Instruction Type with XIP

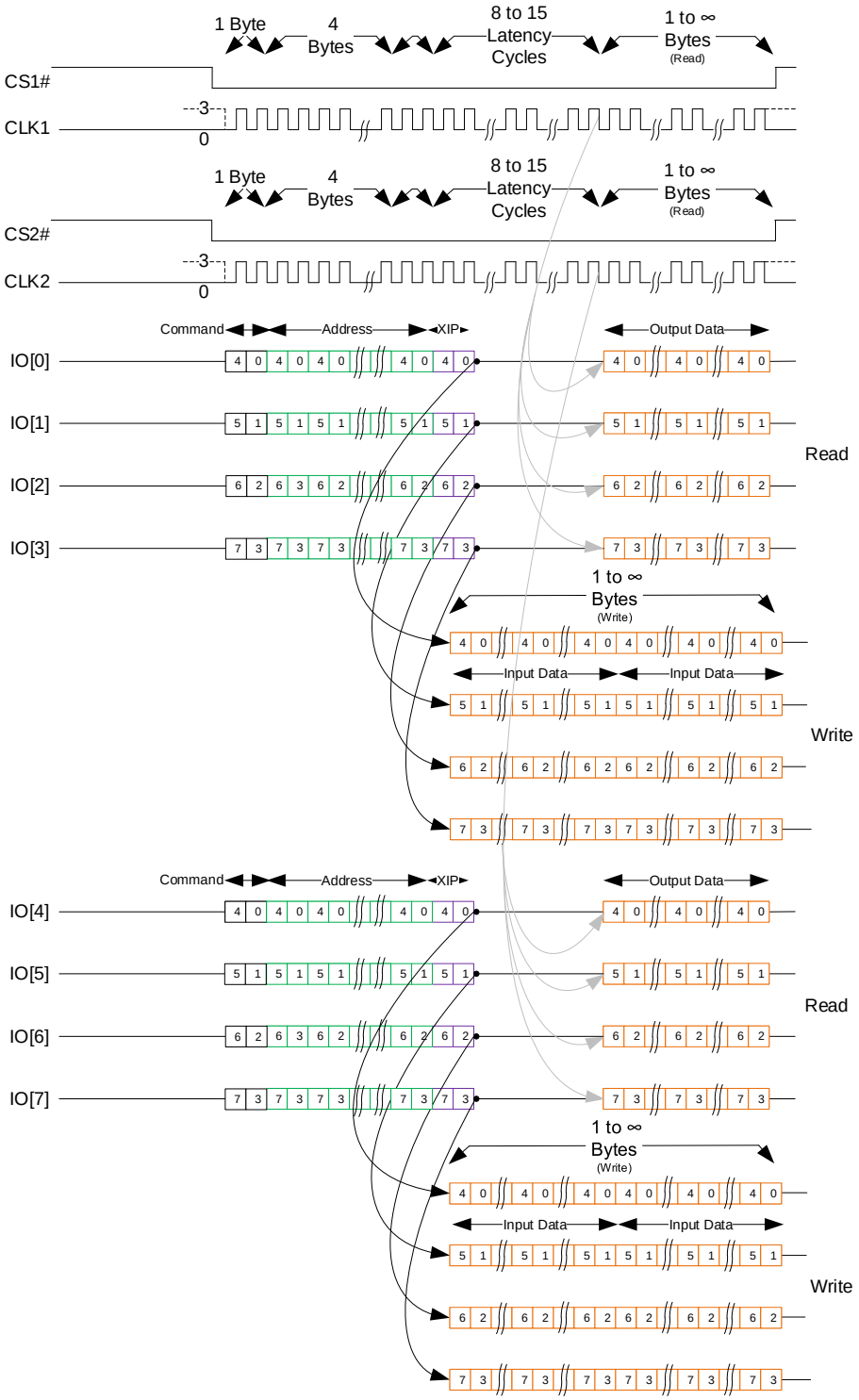


Figure 23 to **Figure 24 show the description of DDR instruction types supported.**

Figure 23: Description of (1-1-1) DDR Instruction Type (With XIP)

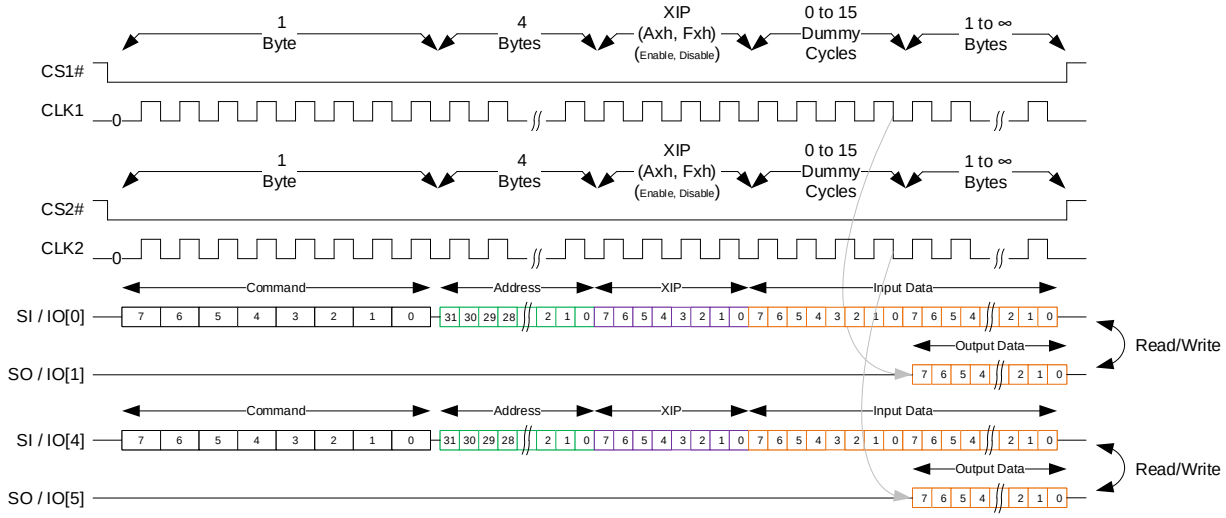
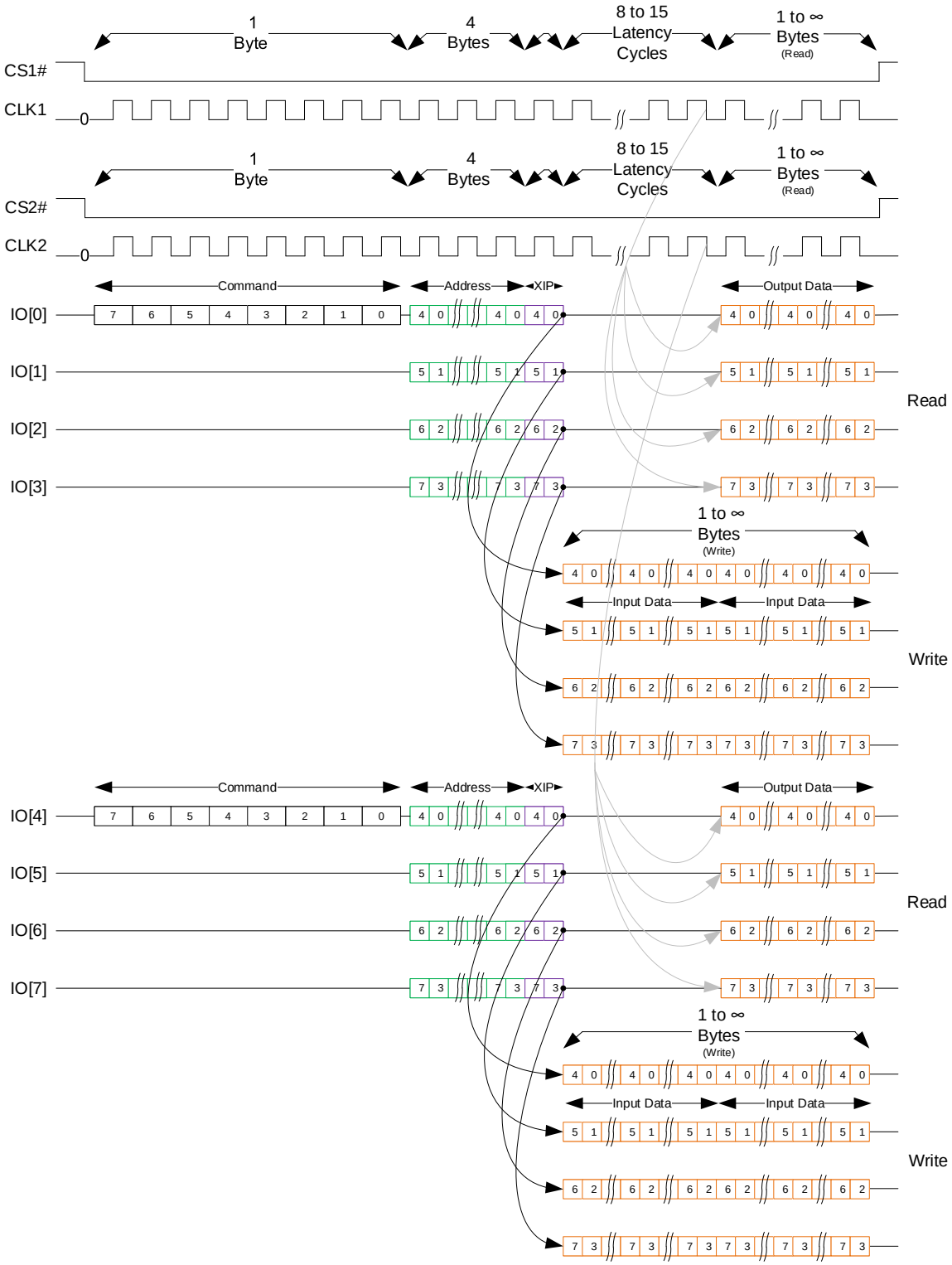


Figure 24: Description of (1-4-4) DDR Instruction Type (With XIP)



Electrical Specifications

Table 34: Recommended Operating Conditions

Parameter / Condition	Minimum	Typical	Maximum	Units
Operating Temperature (T_A)	-40.0	-	125.0	°C
V_{CC} Supply Voltage	2.7	3.0	3.6	V
V_{CCIO} Supply Voltage	1.71	1.8 - 3.0	3.6	V
V_{SS} Supply Voltage	0.0	0.0	0.0	V
V_{SSIO} Supply Voltage	0.0	0.0	0.0	V

Table 35: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{IN}	5.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{INOUT}	6.0	pF

Table 36: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	85°C	20	years

Table 37: DC Characteristics

Parameter	Symbol	Test Conditions	Density	3.0V Device (2.7V-3.6V)				
				Min	Typical[1]	85°C[2]	Max[3]	Units
Active Read Current	I_{READ}	V_{CC} = 3.6V, CLK=108MHz	1Gb		90	180	300	mA
			2Gb		90	180	300	mA
			4GB		120	250	450	mA
			8Gb		200	400	750	mA
Active Write Current	I_{WRITE}	V_{CC} = 3.6V, CLK=108MHz	1Gb		90	180	300	mA
			2Gb		90	180	300	mA
			4GB		120	250	450	mA
			8Gb		180	400	750	mA
Standby Current	I_{SB}	V_{CC} = 3.6V, CLK=V_{CCIO}, CS#=V_{CCIO}, SI=WP#=V_{CCIO}	1Gb		70	135	260	mA
			2Gb		70	135	260	mA
			4GB		100	200	400	mA
			8Gb		200	350	700	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CCIO} (max)		-	-		±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CCIO} (max)		-	-		±1.0	µA
Input High Voltage (V_{CCIO}=1.71-2.2)	V_{IH}			0.65* V_{CCIO}	-		V_{CCIO}+0.2	V
Input High Voltage (V_{CCIO}=2.2-2.7)				1.8				
Input High Voltage (V_{CCIO}=2.7-3.6)				2.2				
Input Low Voltage (V_{CCIO}=1.71-2.2)	V_{IL}			-0.2	-		0.35* V_{CCIO}	V
Input Low Voltage (V_{CCIO}=2.2-2.7)							0.7	
Input Low Voltage (V_{CCIO}=2.7-3.6)							0.8	
Output Low Voltage (V_{CCIO}=1.71-2.2)	V_{OL}	I_{OL} = 0.1mA		-			0.2	V
Output Low Voltage (V_{CCIO}=2.2-2.7)		I_{OL} = 0.1mA					0.4	
Output Low Voltage (V_{CCIO}=2.7-3.6)		I_{OL} = 2.0mA					0.4	
Output High Voltage (V_{CCIO}=1.71-2.2)	V_{OH}	I_{OH} = -0.1mA		1.4			-	V
Output High Voltage (V_{CCIO}=2.2-2.7)		I_{OH} = -0.1mA		2.0				
Output High Voltage (V_{CCIO}=2.7-3.6)		I_{OH} = -1.0mA		2.4				

Notes: *[1] Typical values are measured at 25°C*

[2] 85°C values are guaranteed by characterization; not tested in production

[3] Max values are measured at 125°C

Table 38: Magnetic Immunity Characteristics

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	H_{max_write}	24000	A/m
Magnetic Field During Read	H_{max_read}	24000	A/m

Table 39: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CCIO}
Input rise and fall times	3.0ns
Input and output measurement timing levels	$V_{CCIO}/2$
Output Load	CL = 30.0pF

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 40: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Temperature Under Bias	-45	130	°C
Storage Temperature	-55 to 150		°C
Supply Voltage Vcc	-0.5	4.0	V
Supply Voltage Vccio	-0.5	3.8	V
Voltage on any pin	-0.5	Vccio + 0.2	V
DC output current Iout	± 20		mA
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test) JESD78	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

CS# Operation & Timing

Figure 25: CS# Operation & Timing

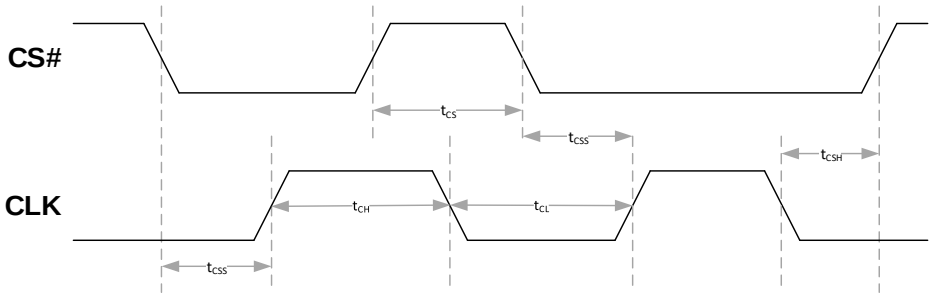


Table 41: SDR CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	108 (SDR)	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Write Cycle (SPI)	t_{CS3}	600	-	ns
Chip Deselect Time after Write Cycle (QPI)	t_{CS5}	600	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:
Power supplies must be stable

Table 42: DDR CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1.0	54 (DDR)	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
CS# High Time (End of Read)	t_{CS1}	20.0	-	ns
CS# High Time (End of Memory Array Write) SPI	t_{CS3}	120.0	-	ns
CS# High Time (End of Memory Array Write) QPI	t_{CS5}	120.0	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5.0	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4.0	-	ns

Notes:
Power supplies must be stable

Command, Address, XIP and Data Input Operation & Timing

Figure 26: SDR Command, Address and Data Input Operation & Timing

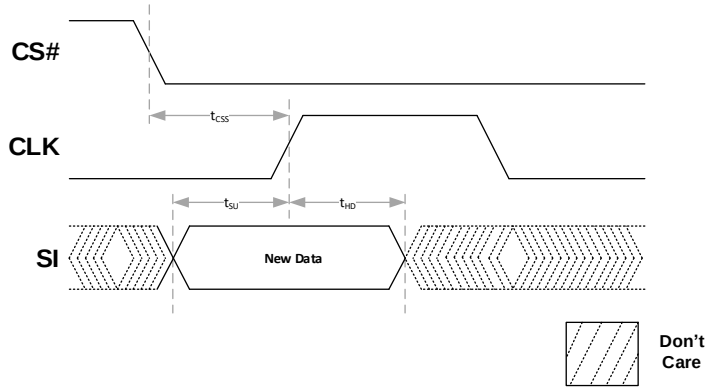


Table 43: SDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	2.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	3.0	-	ns

Notes: Power supplies must be stable

Figure 27: DDR Command, Address and Data Input Operation & Timing

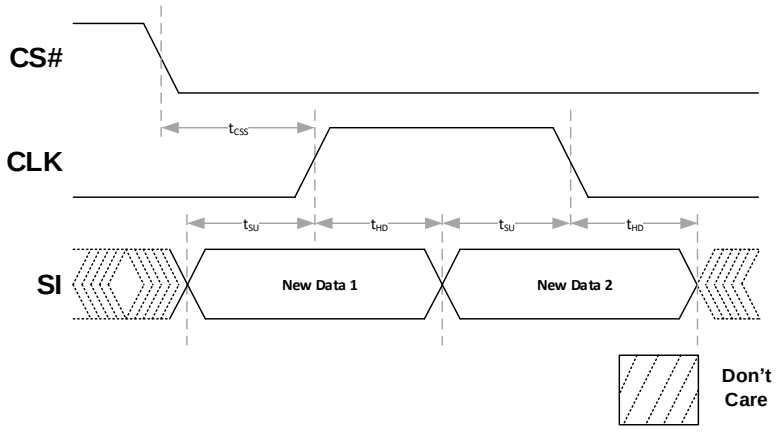


Table 44: DDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	4.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	4.0	-	ns

Notes: Power supplies must be stable

Data Output Operation & Timing

Figure 28: SDR Data Output Operation & Timing

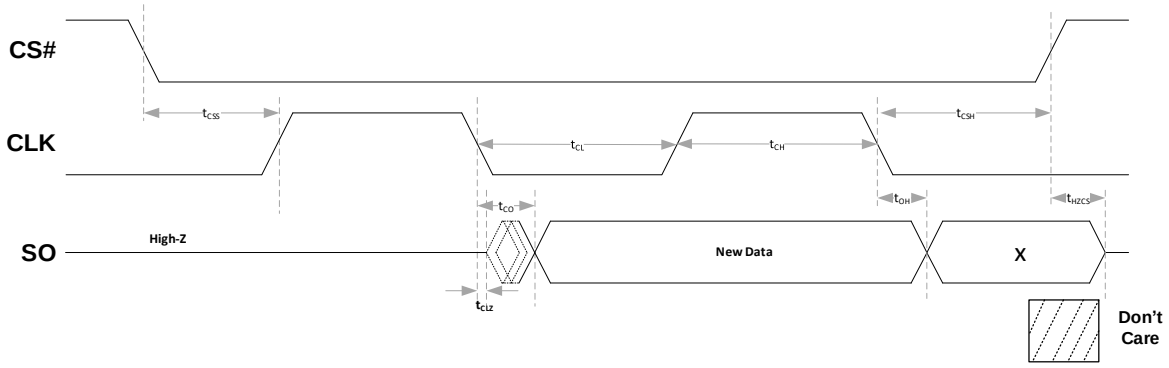


Table 45: SDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	7.0	ns

Notes:
Power supplies must be stable

Figure 29: DDR Data Output Operation & Timing

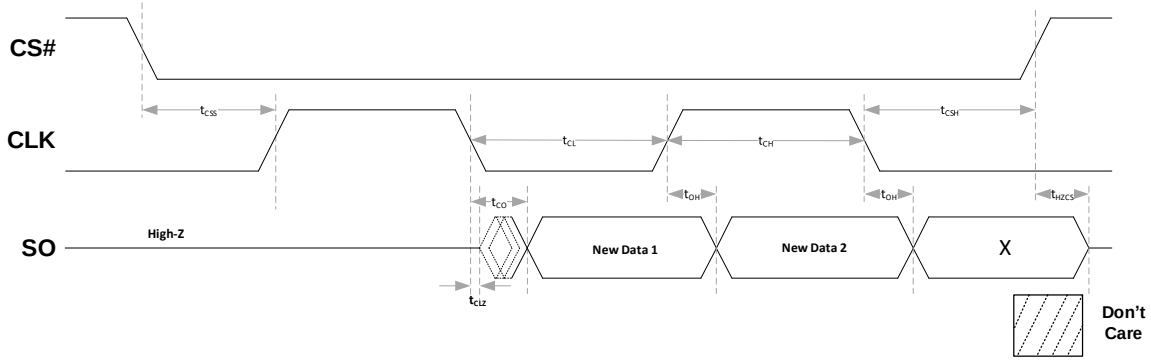


Table 46: DDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	6.0	ns

Notes:
Power supplies must be stable

Figure 30: DDR Data Strobe (DS) Output Timing

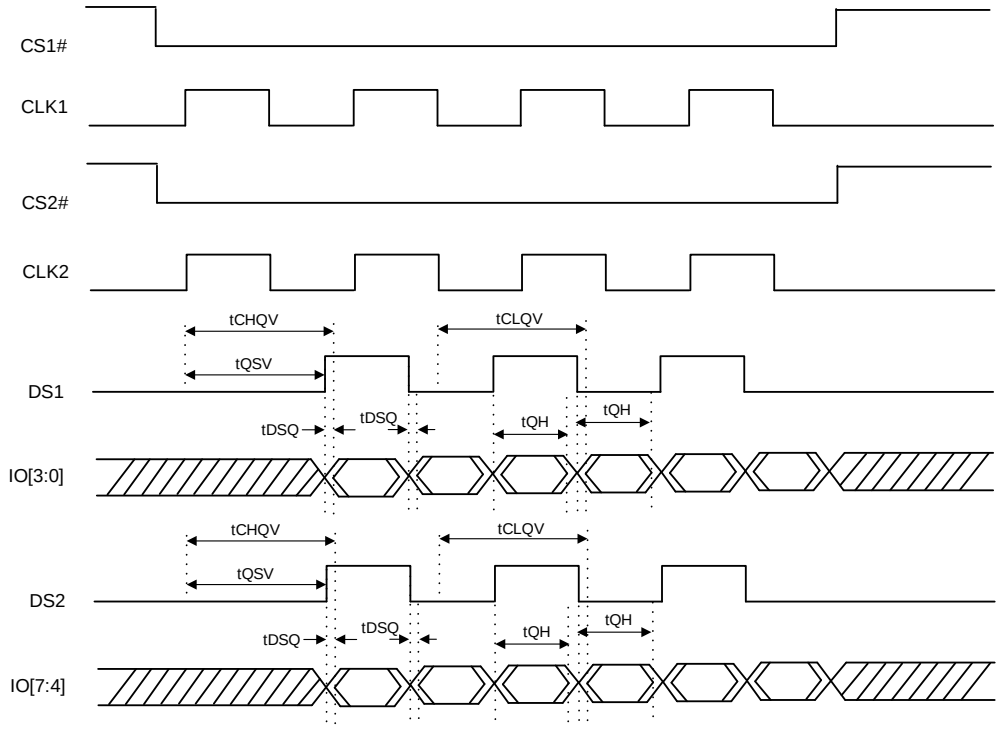


Table 47: DDR Data Strobe (DS) Output Timing

Parameter	Symbol	Minimum	Maximum	Units
Clock Transient to Output Valid (30pF Loading)	t_{CLQV}/ t_{CHQV}	-	5.0	ns
I/O Valid Skew Related to DS (30pF Loading)	t_{DSQ}	-	1.0	ns
I/O Hold Time Related to DS	t_{QH}	(t_{CL}/ t_{CH}) - t_{QHS}	-	ns
I/O Hold Skew Factor (30pF Loading)	t_{QHS}	-	1.0	ns
DS Clock Transient to DS Valid Time	t_{QSV}	-	5.0	ns

WP# Operation & Timing

Figure 31: WP# Operation & Timing

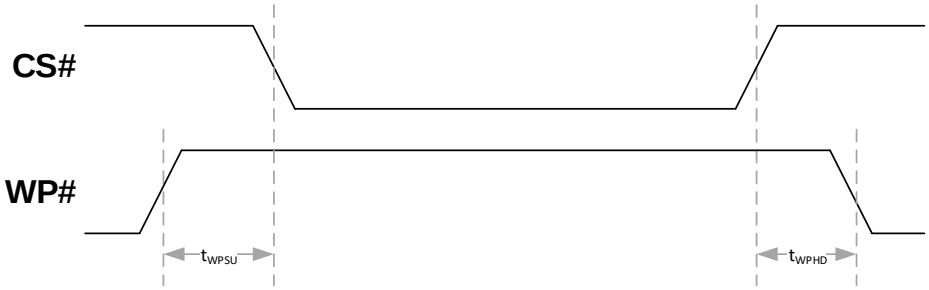


Table 48: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:
Power supplies must be stable

JEDEC Reset Operation & Timing

Figure 32: JEDEC Reset Operation & Timing

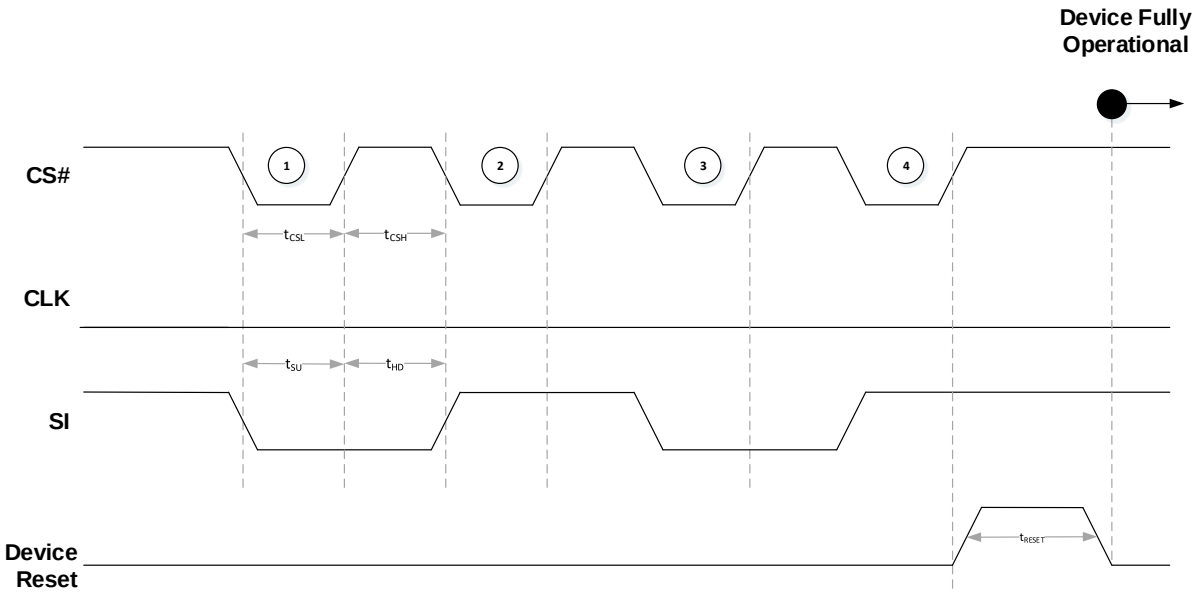


Table 49: JEDEC Reset Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CS# Low Time	t_{CL}	1.0	-	µs
CS# High Time	t_{CH}	1.0	-	µs
SI Setup Time (w.r.t CS#)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t CS#)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	450.0	µs

Notes:
Power supplies must be stable

Thermal Resistance

Table 50: Thermal Resistance Specifications

Parameter	Description	Test Conditions	96/224 Ball FBGA				Unit
			1Gb	2Gb	4Gb	8Gb	
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	17.89	17.89	17.90	TBD	°C/W
θ_{JC}	Thermal resistance (junction to case)		2.10	2.10	2.19	TBD	

Notes:
1: These parameters are guaranteed by characterization; not tested in production.
2: Ambient temperature, T_A 25 ℃
3: Worst case Junction temp specified for Top die (θ_{JA}) and Bottom die (θ_{JC})

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Revision History

Revision	Date	Change Summary
REV A	01/10/2022	Initial release Package pinout updated to reflect Dual QSPI Removed DS1 & DS2 (Will not require a data strobe at these frequencies) Added 2 interrupt pins to the package Added 2Gb to the densities supported
REV B	3/30/2022	Changed signal description of Vccio. It wasn't clear that it is referring to I/O supply. Removed option of 1.8V Vcc supply Updated package pin definition: Changed Vccq to Vccio Added Pin assignment table Removed Deep Power down Enter and Exit commands Changed DDR max freq. from 80MHz to 54MHz Defined V_{DD2} for 8Gb devices as Ball J6. This is a NC ball on the 1, 2 &4Gb devices. Changed density field from 4 digits to 3 digits in part number. Added V_{DD} Currents to DC Characteristics
B.1	05/16/2022	Updated DC Characteristics Table: Current numbers are based on UMC's analysis of their current 22nm process. Added V_{DD} to supply line on Front page
B.2	05/23/2012	Updated Ball assignment table: N12 was not shown as Vss Updated Power sequencing description under DEVICE INITIALIZATION Added Absolute Maximum Ratings Table Called out specific voltages are allowed for V_{CCIO} on front page.
B.3	05/25/2022	Added Thermal Resistance table Added Absolute Maximum Rating on V_{DD} and V_{DD2} Changed the height of the package to allow for stacking of 8 rather than 4 devices. This increases nominal height "A" from 1.39 to 1.85
REV C	06/01/2022	Changes the outer limit of package dimension to allow compatibility between 1-4 and 8Gb densities. See Figure 5. See Changes to E and E2. Changed the nominal height "A" to be compatible with Gen 3 parallel devices: Nominal Height/Thickness in Figure 5 changed to 1.43 Leaded ball options added to Order Option table
C.1	07/20/2022	Removed Performance Table Added Figures to ToC Added Tables to ToC Updated SDR Data Output Operation & Timing Updated DDR Data Output Operation & Timing Renamed from 88Ball to 96Ball (Included mechanical support balls) Added Extended Safe Operating Area as well as Normal Operating Conditions Updated Memory Map Table
REV D	09/22/2022	Removed redundant Table under package drawing Updated Package Ball H12: This is DNU and not GRD Updated Power consumption in DC Characteristics Table Fixed wording on use for V_{BYP} in pin definition table
	11/21/2022	Added Op Code 13h to support legacy device boot on Xilinx platforms
REV E	12/23/2022	Added Op code 06Ch to support legacy device boot on Xilinx platforms This device is now available for use in LEO. The Extended Safe Operating Area (ESOA) is no longer described here and is only available through our partner program: As such Ball K10, J6 (previously external Vdd & Vdd2) are now NC and L10 (previously VBYP) has to be connected to Vss. Added 85℃ power consumption to DC Characteristics Table.
E.1	01/10/2023	Added Hardware Block Protect function using HBP0, HBP1, HBP2, and HTBSEL signals Removed Serial Number Register Nominal Height/Thickness in Figure 6 changed from 1.43mm to 1.53mm Changed 0x6B command opcode to 3-Byte address from 4-Byte address

E.2	04/05/2023	Changed 0x0B command opcode to 3-Byte address from 4-Byte address Added 0x6C command opcode Changed latency cycles requirement to 10 from 8 for Fast Read in QPI (4-4-4)
E.3	05/26/2023	Input & Output Low & High Voltage levels have been redefined as references to V_{CCIO} rather than V_{CC} in the DC Characteristics. Specified Max temp to be junction rather than ambient.
E.4	05/27/2023	Added Extended Address Register
E.5	06/22/2023	Increased Deselect Time after Write Cycle to 600ns (Table 41).
E.6	06/23/2023	Increased tPU to 25ms (Table 10).
E.7	07/28/2023	Renamed Bit 6 in status register from SNPEN (Serial Number Protection Enable/Disable) to reserved. This is a R/W bit but has no function as There is no serial number.
REV F	08/30/2023	Added 224 Ball package option Clarification that PEMS-INST-001 flow version of product will be supplied through a partner. Input & Output Low & High Voltage levels have been redefined as references to VCCIO rather than VCC in the DC Characteristics Table 37. Guideline on device initialization corrected to say: pullup on CS# is to VCCIO.
F.1	09/25/2023	Fixed the table and figure numbering in Device Power up and Power down
F.2	10/03/2023	Cleaned up DC Characteristics table Hardware RESET is now supported instead of JEDEC RESET Updated Maximum rating table 40
	11/10/2023	Fixed Ball assignment for HTBSEL and HBP2 in Table-5 for 224-ball package. (The package drawing was correct).
F.3	11/21/2023	ECC Count register definition was incorrect. Only uncorrectable errors are counted and increment the count. Maximum frequency of operation at all corner cases defined Removed Unique ID Register. This read only register always returned a 64 bit Zero value.
F.4	01/02/2024	CR1 default for WREN was incorrectly stated as 10. It is 00. CR2 default for latency was incorrectly stated as 0000. It is 8 cycles: 1000