

Space-Grade High Performance Dual-Quad Serial Persistent SRAM Memory

(AS301G208, AS302G208, AS304G208, AS308G208)

Features

- Interface
 - Dual Quad SPI – support 8-bit wide transfer
 - Dual QPI (4-4-4) – up to 108MHz SDR
 - Dual QPI (4-4-4) – up to 54MHz DDR
- Technology
 - 22nm pMTJ STT-MRAM
 - Data Endurance: 10^{16} write cycles
 - Data Retention: 20 years @ 85°C
- Density
 - 1Gb, 2Gb, 4Gb, 8Gb
- Operating Voltage Range
 - V_{CC} : 2.70V – 3.60V
 - V_{CCIO} : 1.8V, 2.5V, 3.0V, 3.3V ***
 - V_{DD} : 1.00V ****
- Operating Temperature Range
 - Industrial Extended: -40°C to 125°C
- Packages
 - 96-ball FBGA (20mm x 20mm)
- Data Protection
 - Hardware Based
 - Write Protect Pin (WP#)
 - Software Based
 - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Identification
 - 64-bit Unique ID
 - 64-bit User Programmable Serial Number
- Supports JEDEC Reset
- 48-hour burn-in at 125°C
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

* Leaded Balls available

** PEMS-INST-001 Flow available as custom option

*** V_{CCIO} can be set to any voltage within the following range: 1.71V – 3.60V

**** V_{DD} is an optional reference supply that extends the safe operating area of the device

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General Description

ASxxxx208 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in density ranging from 1Gbit to 8Gbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @85°C.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

ASxxxx208 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

ASxxxx208 connects two Quad SPI devices with a single CS#, providing an eight bit I/O data path.

ASxxxx208 is available in an 88-ball FBGA package. The package has separate balls for CS1#, CLK1#, and INT1 (Dual-Quad SPI device 1) and CS2#, CLK2#, and INT2 (Dual-Quad SPI device 2). This package is compatible with similar low-power volatile and non-volatile products.

Table 2: Multi-Die Package Density

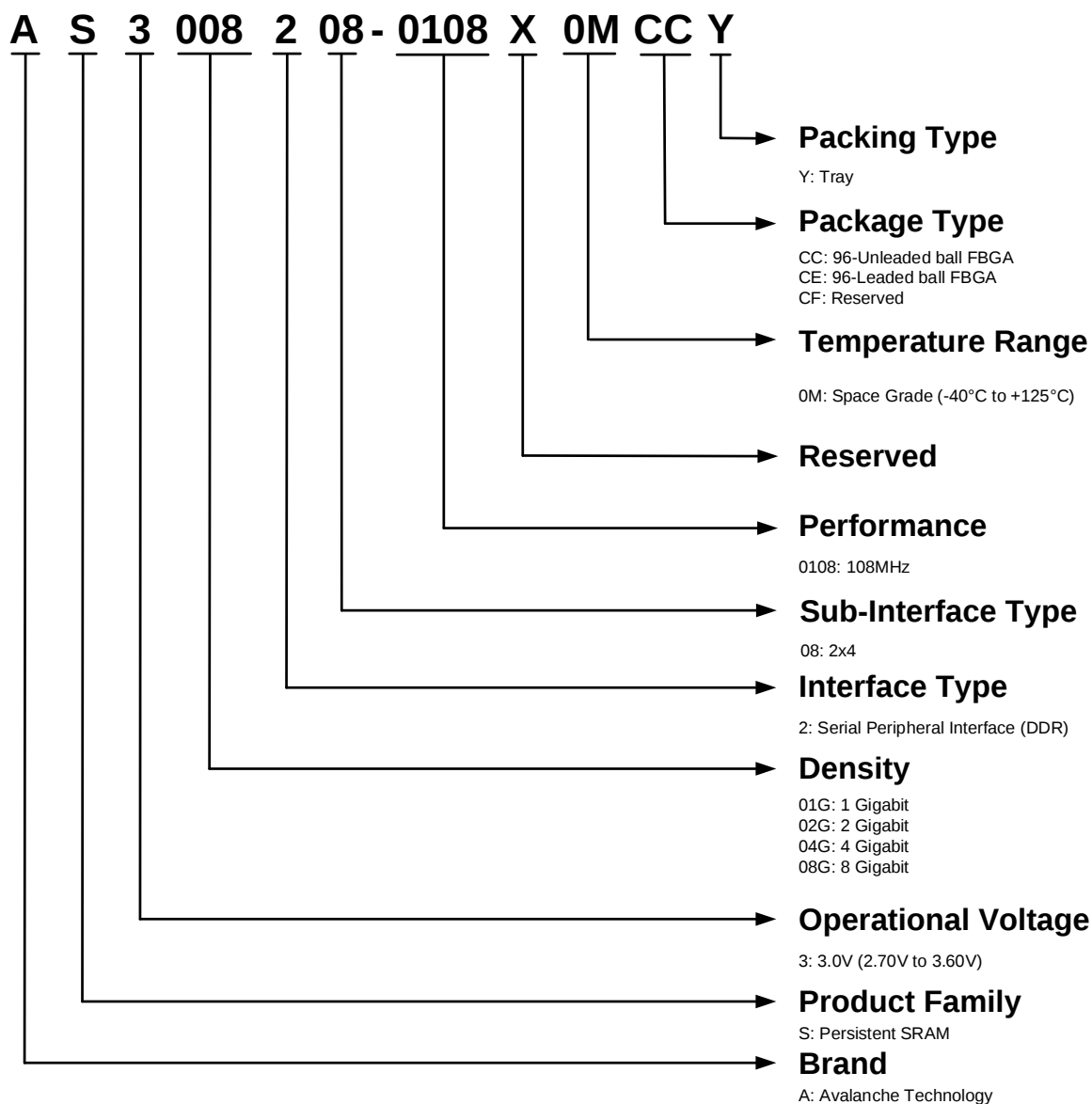
Density	512Mb Die	1Gb Die
1Gb	x2	–
2Gb	–	x2
4Gb	–	x4
8Gb	–	x8

ASxxxx208 is offered with industrial extended (-40°C to 125°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Ordering Options



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 3: Valid Combinations List

Valid Combinations – 108MHz				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
AS301G208-0108X	0M	CC	Y	AS301G208-0108X0MCCY
AS302G208-0108X	0M	CC	Y	AS302G208-0108X0MCCY
AS304G208-0108X	0M	CC	Y	AS304G208-0108X0MCCY
AS308G208-0108X	0M	CC	Y	AS308G208-0108X0MCCY
AS301G208-0108X	0M	CE	Y	AS301G208-0108X0MCEY
AS302G208-0108X	0M	CE	Y	AS302G208-0108X0MCEY
AS304G208-0108X	0M	CE	Y	AS304G208-0108X0MCEY
AS308G208-0108X	0M	CE	Y	AS308G208-0108X0MCEY

Signal Description and Assignment

Figure 2: Device Pinout

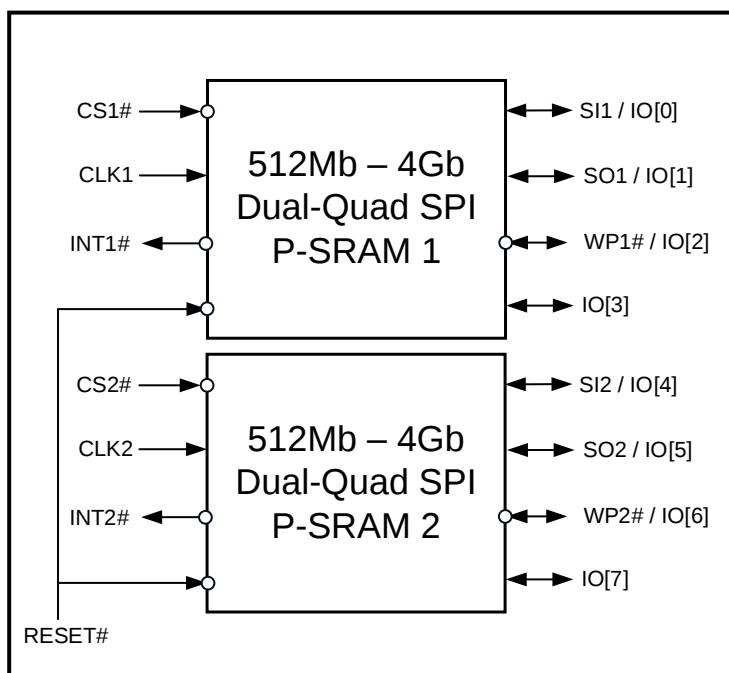


Figure 3: System Block Diagram

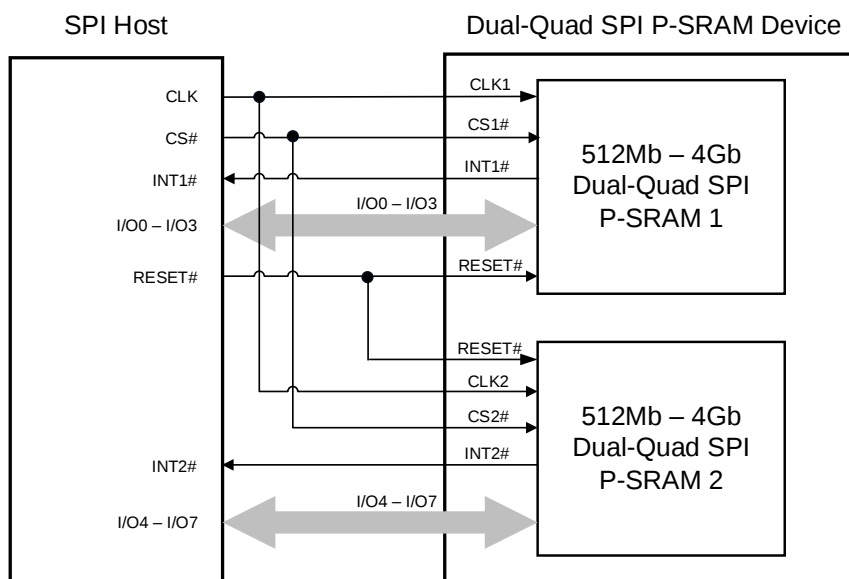


Table 4 : Signal Description

Signal	Ball Assignment	Type	Description
CS1#	L7	Input	Chip Select 1: When CS1# is driven High, the Quad SPI device 1 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
CLK1	K7	Input	Clock 1: Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. - SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR - SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT1#	J10	Output	Interrupt 1: Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI1	M8	Input	Serial Data Input (SPI): The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode.
IO[0]		Bidirectional	Bidirectional Data 0 (QPI): The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
SO1	M7	Input	Serial Data Output (SPI): The unidirectional I/O transfers data out of device 1 on the falling edge of the clock in Single SPI mode.
IO[1]		Bidirectional	Bidirectional Data 1 (QPI): The bidirectional I/O that transfers data into and out of device 1 in Quad SPI mode.
WP1#	L9	Input	Write Protect 1 (SPI): Write protects the status register of device 1 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[2]		Bidirectional	Bidirectional Data 2 (QPI): The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
IO[3]	M9	Bidirectional	Bidirectional Data 3 (QPI): The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode. This pin can be tied to Vcc if not used.
CS2#	J8	Input	Chip Select 2: When CS2# is driven High, the Quad SPI device 2 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS2# Low enables device 2, placing it in the active mode. After power-up, a falling edge on CS2# is required prior to the start of any instructions.
CLK2	K6	Input	Clock 2: Provides the timing for device 2 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock.

Signal	Ball Assignment	Type	Description
			In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. - SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR - SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT2#	K8	Output	Interrupt 2: Output generated by device 2 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI2	M10	Input	Serial Data Input (SPI): The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode.
IO[4]		Bidirectional	Bidirectional Data 4 (QPI): The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
SO2	N8	Input	Serial Data Output (SPI): The unidirectional I/O transfers data out of device 2 on the falling edge of the clock in Single SPI mode.
IO[5]		Bidirectional	Bidirectional Data 5 (QPI): The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
WP2#	N7	Input	Write Protect 2 (SPI): Write protects the status register of device 2 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[6]		Bidirectional	Bidirectional Data 6 (QPI): The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
IO[7]	N6	Bidirectional	Bidirectional Data 7 (QPI): The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
RESET#	J9	Input	RESET: This is a RESET# signal. When this signal is driven high, the device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z.
V _{CCIO}	G4, P4, G5, J5, P5, M6, H7, H9, N9, J11, M11, G12, P12	Supply	I/O power supply.*
V _{SSIO}	M5, H6, L6, P8, H10, N10, P10, H11, N11	Supply	I/O ground supply.
V _{CC}	K4, M4, K5, G7, P7, G9, K9, P9, K11, K12, M12	Supply	Core power supply.*
V _{SS}	A1, B1, W1, Y1, A2, Y2, F3, G3, P3, R3, F4, H4, J4, L4, N4,	Supply	Core ground supply.

Signal	Ball Assignment	Type	Description
	R4, L5, N5, G6, P6, G8, H8, G10, G11, L11, P11, F12, H12, J12, L12, R12, N12, F13, G13, P13, R13, A14, Y14, A15, B15, W15, Y15		
V_{DD}	K10	Supply	Supply reference: This is an optional reference supply to allow the safe operating zone in harsh environments to be extended. If not necessary, this ball should be left as a NC.*
V_{DD2}	J6	Supply	Supply reference only on the 8Gb device * This ball is a NC in 2 cases a) In 1, 2 & 4Gb devices this ball is a NC (not internally connected. They can be driven or left unconnected). b) Same as V _{DD} (Ball K10). If the device is not expected to operate in the extended zone, it should be left as a NC
V_{BYP}	L10	Input	V _{DD} bypass. If the device is not operating in normal mode and not extended Safe Operating Area, this pin should be connected to V _{SS} . See Device initialization sequence extended safe zone for correct operation if this signal is used.
DNU	H5, J7, L8		Do not use: DNUs must be left unconnected.

* For normal operation an internal V_{DD} supplies all necessary reference voltages and Balls K10 & J6 should be left as a NC. Ball V_{BYP} should also be grounded (Connected to V_{SS}). See Device initialization on power sequencing.

For device operation in the Extended Safe Operating Area (See app note), V_{DD} (in the case of 1, 2 & 4Gb) and additionally V_{DD2} (in the case of 8Gb) need to be supplied. V_{BYP} should also be driven per spec in Device Initialization sequence for Extended Safe Operating Area (ESOA).

Package Options

96-ball FBGA (Balls Down, Top View)

Figure 4: 96-ball FBGA

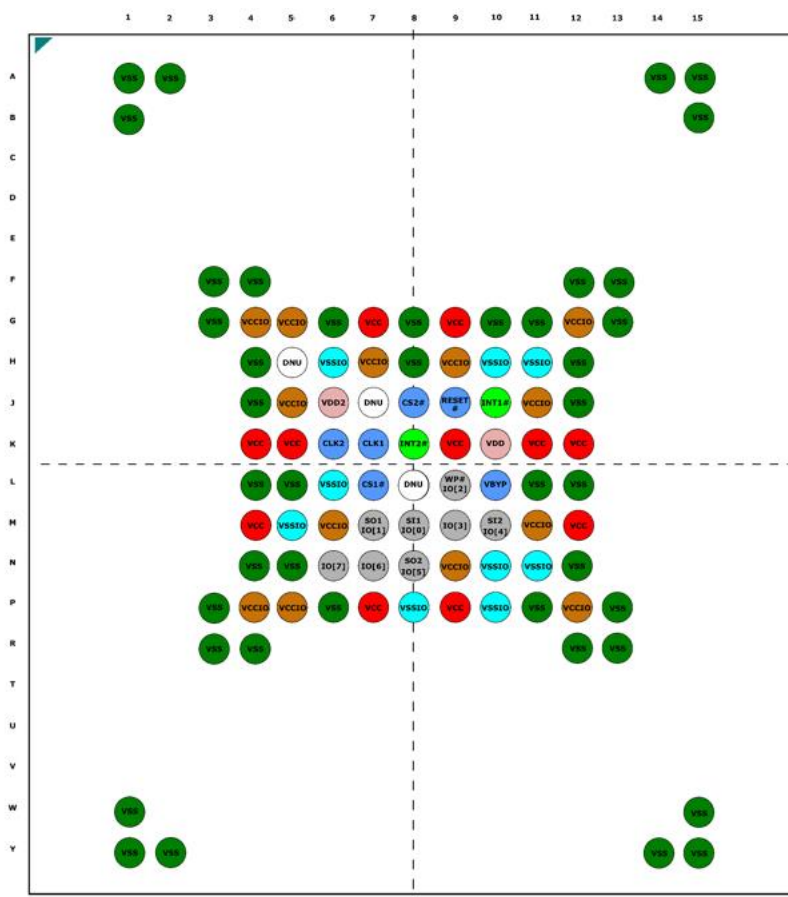
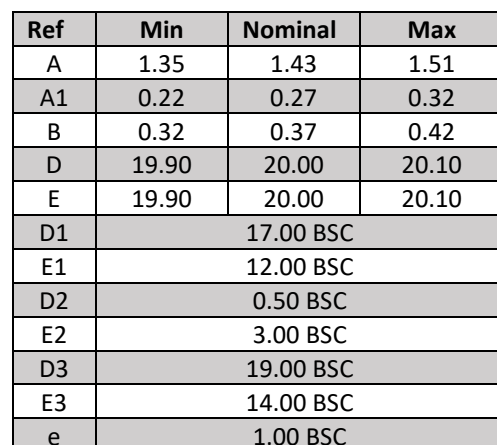


Figure 5: 96-ball FBGA



1. Dimensions in millimeters (mm).
2. The 'e' represents the basic solder ball grid pitch.
3. 'B' (x36) is measurable at the maximum solder ball diameter in a plane parallel to datum.

Solderball diameter refers to post reflow condition. The pre-reflow diameter is 0.37mm.

Architecture

ASxxxx208 is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running up to 54MHz (QPI) DDR mode or 108MHz (QPI) SDR mode, eExecute-In-Place (XIP) functionality, and hardware/software based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB} .

ASxxxx208 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. In Single SPI mode, the device is accessed via the SI / IO[0] pin of a Dual-Quad SPI 1 and the SI / IO[4] pin of a Dual-Quad SPI 2. In Quad mode, the IO[0:3] of a Dual-Quad SPI 1 and the IO[4:7] of a Dual-Quad SPI 2 are used respectively to access the device (consult Figure 2 & Figure 3). Furthermore, Single Data Rate (SDR) and Double Data Rate (DDR) instructions utilize CLK edges differently to transfer information; SDR uses a single CLK edge whereas DDR uses both edges of CLK. **Table 5 & Table 5** summarizes all the different interface modes supported and their respective I/O usage. **Table 6** shows the clock edge used for each instruction component.

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0]) or SO / IO[1]) of a Dual-Quad SPI 1 and (SI / IO[4]) or SO / IO[5]) of a Dual-Quad SPI 2. On the other hand, 4-4-4 represents command, address and data being sent on eight I/Os: (IO[3:0]) of a Dual-Quad SPI 1 and (IO[7:4]) of a Dual-Quad SPI 2 (consult Figure 2 & Figure 3).

All AC timings and waveforms and DC specification are defined in the datasheet using single CS# (Chip Select) and CLK (Serial Clock) signals.

Table 5: Interface Modes of Operations – Device 1

Instruction Component	Single SPI (1-1-1)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[0]	SI / IO[0]	IO[3:0]
Address	SI / IO[0]	IO[3:0]	IO[3:0]
Data Input	SI / IO[0]	IO[3:0]	IO[3:0]
Data Output	SO / IO[1]	IO[3:0]	IO[3:0]

Table 6: Interface Modes of Operations – Device 2

Instruction Component	Single SPI (1-1-1)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[4]	SI / IO[4]	IO[7:4]
Address	SI / IO[4]	IO[7:4]	IO[7:4]
Data Input	SI / IO[4]	IO[7:4]	IO[7:4]
Data Output	SO / IO[5]	IO[7:4]	IO[7:4]

Table 7: Clock Edge Used for instructions in SDR and DDR modes

Instruction Type	Command	Address	Data Input	Data Output
(1-1-1) SDR				 1
(1-1-1) DDR				 1
(1-4-4) SDR				 1
(1-4-4) DDR				 1
(4-4-4) SDR				 1
(4-4-4) DDR				 1

Notes:

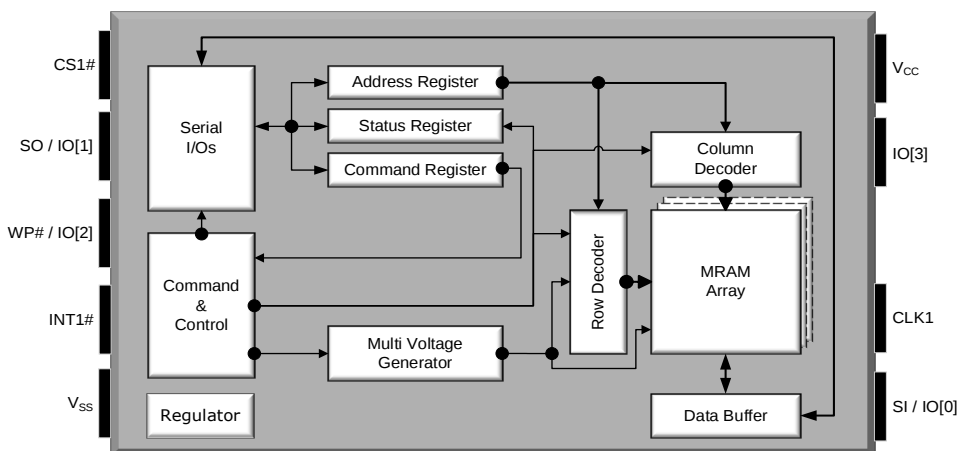
R: Rising Clock Edge

F: Falling Clock Edge

1: Data output from ASxxxx208 always begins on the falling edge of the clock – SDR & DDR

ASxxxx208 supports eXecute-In-Place (XIP) which allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. Thus, XIP mode saves command overhead and reduces random read & write access time. A special XIP byte must be entered after the address bits to enable/disable (Axh/Fxh) XIP.

ASxxxx208 offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

Figure 6: Functional Block Diagram – Dual QSPI Device 1


The block diagram illustrates the internal architecture of the MRAM. Key components include:

- Serial I/Os:** Connected to CS2# and SO / IO[5].
- Command & Control:** Connected to WP# / IO[6] and INT2#.
- Registers:** Address Register, Status Register, and Command Register.
- Decoders:** Column Decoder and Row Decoder.
- MRAM Array:** The central memory array.
- Multi Voltage Generator:** Provides power to the array.
- Regulator:** Connected to V_{SS}.
- Data Buffer:** Connected to the array and SI / IO[4].

External power and control signals are shown on the right: V_{CC}, IO[7], CLK2, and SI / IO[4].

Mode	Current	CS#	CLK	SI / IO[3:0]	SO / IO[3:0]
Standby	I _{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I _{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I _{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z

H: High (Logic '1')
L: Low (Logic '0')
Hi-Z: High Impedance

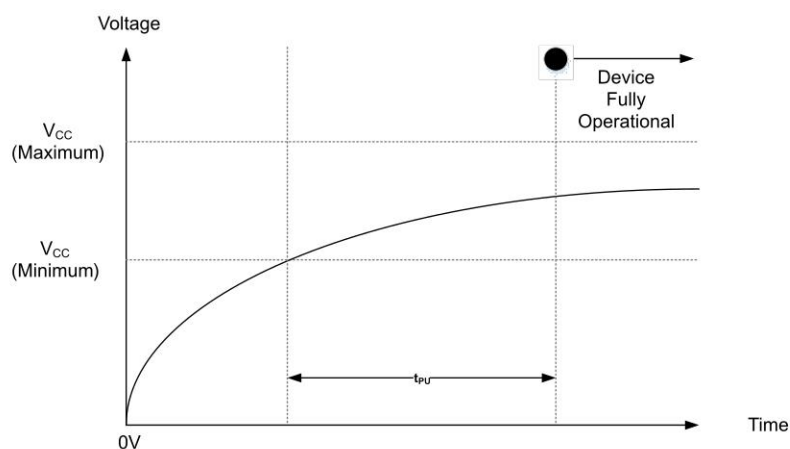
Mode	Current	CS#	CLK	SI / IO[7:4]	SO / IO[7:4]
Standby	I _{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I _{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I _{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z

Normal Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- V_{CC} and V_{CCIO} can ramp up together (R_{VR}), if not possible then V_{CC} first followed by V_{CCIO} . The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-up (CS# must follow the applied voltage on V_{CC} (a 10K Ω pull-up Resistor to V_{CC} is recommended)) until V_{CC} reaches $V_{CC}(\text{minimum})$ and then a further delay of t_{PU} (Figure 8).
- During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences (Figure 9).

Figure 8: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- V_{CC} and V_{CCIO} can ramp down together (R_{VF}), if not possible then V_{CC} first followed by V_{CCIO} . The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-down ($CS\#$ must follow V_{CC} during power-down (a 10K Ω pull-up Resistor to V_{CC} is recommended)) until V_{CC} reaches V_{SS} .
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, when V_{CC} goes below V_{CC_CUTOFF} . The voltage must be dropped below $V_{CC}(\text{Reset})$ for a period of t_{PD} . The power-up timing needs to be observed after V_{CC} goes above $V_{CC}(\text{minimum})$

Figure 9: Power-Down Behavior

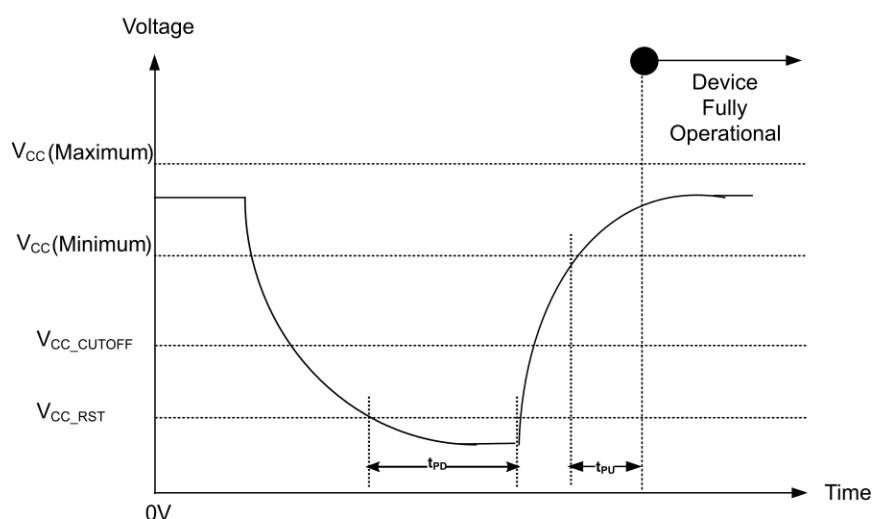


Table 10: Power Up/Down Timing and Voltages

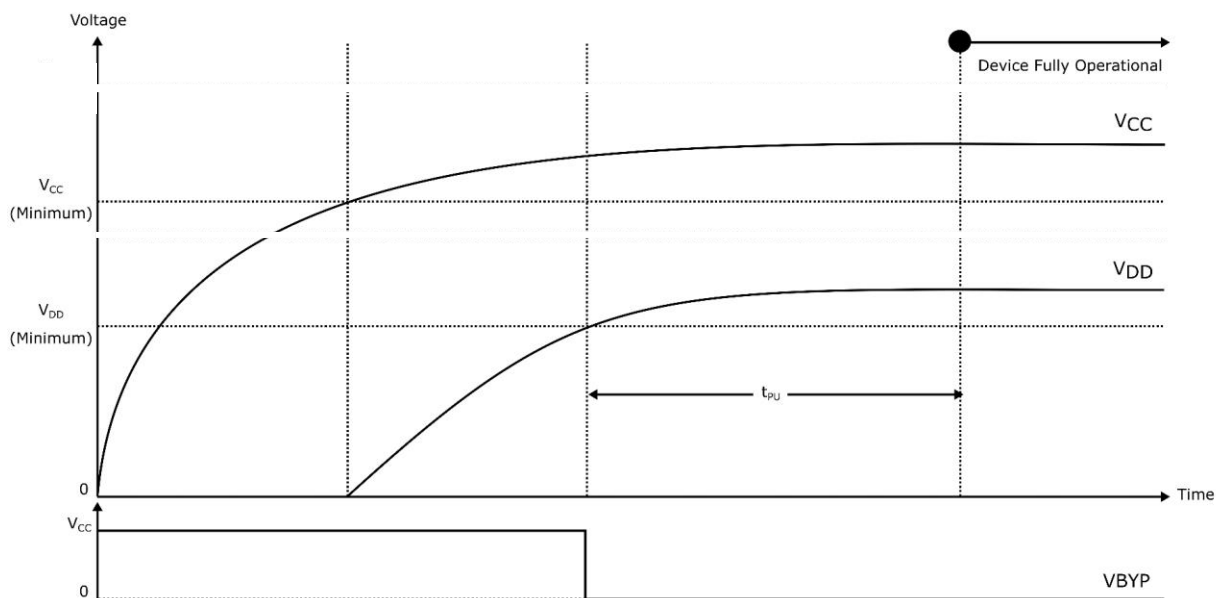
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	$\mu\text{s/V}$
V_{CC} Ramp Down Time	R_{VF}		20	-	-	$\mu\text{s/V}$
V_{CC} Power Up to First Instruction	t_{PU}		1	-	-	ms
V_{CC} (low) time	t_{PD}		1			ms
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} (Reset)	V_{CC_RST}		0		0.3	V

Device Initialization Extended Safe Operating Area

When powering up, the following procedure is required to initialize the device correctly: Ramp up V_{CC} (R_{VR}):

- The following sequence (for V_{CC} , V_{CCIO} , V_{DD}) must be followed to ensure a proper power-up:
 - V_{CC} and V_{CCIO} can Ramp together if not possible then V_{CC} first followed by V_{CCIO} .
 - V_{DD} supply should be kept low until V_{CC} and V_{CCIO} has reached their minimum voltage values.
 - There are no timing requirements between the power supplies if the sequence is followed
- VBYP input value is kept high ($>V_{ih}$) from initial phase of power up sequence until V_{DD} reaches V_{DD} (minimum) then it can be driven low
- It is recommended that no instructions are sent to the device before completion of power up sequence
 - CS# cannot be active during power-up (a 10K Ω pull-up Resistor to V_{CC} is recommended)
- During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences

Figure 10: Power-Up Behavior ESOA



The following procedure is required to power down the device correctly:

- It is recommended to power down all supplies together. If not possible then the following sequence must be followed 1- V_{CC} , 2- V_{CCIO} , 3- V_{DD} .
- Timing for Ramp down rate should follow ramp down time (R_{VF}).
- $CS\#$ cannot be active during power-down (a 10K Ω pull-up Resistor to V_{CC} is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, if V_{CC} goes below V_{CC_CUTOFF} or V_{DD} goes below V_{DD_CUTOFF} . All supply voltages V_{CC} , V_{CCIO} and V_{DD} must be dropped below their respective (RESET) values V_{CC_RST} and V_{DD_RST} for a period of t_{PD} . Figure-10 timing needs to be observed for the subsequence power-up.

Figure 11: Power-Down Behavior ESOA

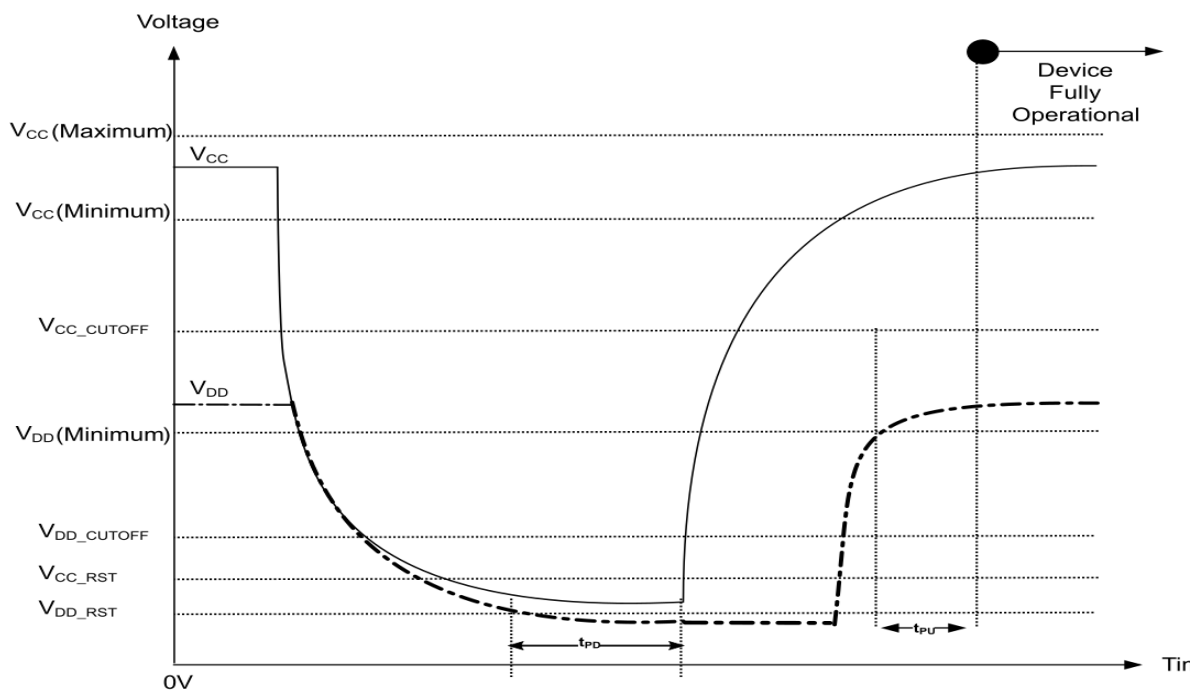


Table 11: Power Up/Down Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V _{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V _{DD} Range			0.90	-	1.05	V
V _{CC} Ramp Up Time	R _{VR}		30	-	-	μs/V
V _{CC} Ramp Down Time	R _{VF}		20	-	-	μs/V
V _{CC} Power Up to First Instruction	t _{PU}		1	-	-	ms
V _{CC} (low) time	t _{PD}		1			ms
V _{CC} Cutoff – Must Initialize Device	V _{CC-CUTOFF}		1.6	-	-	V
V _{CC} (Reset)	V _{CC_RST}		0		0.3	V
V _{DD} Range			0.9	-	1.05	V
V _{DD} Cutoff – Must initialize Device	V _{DD-CUTOFF}		0.6	-	-	V
V _{DD} (Reset)	V _{DD_RST}		0	-	0.15	V

Memory Map

Table 12: Memory Map

Density	Address Range	32-bit Address [31:0]	
1Gb	0000000h – 7FFFFFFFh	[31:27] - Logic '0'	[26:0] - Addressable
2Gb	0000000h – FFFFFFFFh	[31:28] - Logic '0'	[27:0] - Addressable
4Gb	000000h – 1FFFFFFFh	[31:29] - Logic '0'	[28:0] - Addressable
8Gb	000000h – 3FFFFFFFh	[31:30] - Logic '0'	[29:0] - Addressable

Read any Register Addresses

Table 13: Register Addresses

Register Name	Address
Status Register	0x000000h
Interrupt Status Register	0x000001h
Configuration Register 1	0x000002h
Configuration Register 2	0x000003h
Interrupt Configuration Register	0x000004h
ECC Test – Data Input Register	0x000005h
ECC Test – Error Injection Register	0x000006h
ECC Test – Data Output Register	0x000007h
ECC Test – Error Count Register	0x000008h
Device Identification Register	0x000030h
Unique Identification Register	0x000040h
Serial Number Register	0x000050h

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

The WREN bit must be set to “1” to enable write operations. This bit can only be set by executing the Write Enable (WREN) instruction opcode.

The device supports Back-to-Back write operations: WREN is prerequisite to only the first Memory Array Write instruction. The WREN bit doesn’t clear to “0” following subsequent memory write opcodes. WREN disable instruction must be executed to reset WREN.

Table 14 : Status Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – unprotected
SR[6]	SNPEN	Serial Number Protection Enable/Disable	R/W	0	1: S/N Write protected – protection enabled 0: S/N Write protected – protection disabled
SR[5]	TBSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits (Table 14, Table 15)
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Protection Enable/Disable	R	0	1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Table 15: Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Gb	2Gb	4Gb
0	0	0	None	None	None	None
0	0	1	Upper 1/64	7E00000h – 7FFFFFFFh	03FFFFFFh – FFFFFFFFh	0000000h – 1FFFFFFFh
0	1	0	Upper 1/32	7C00000h – 7FFFFFFFh	07FFFFFFh – FFFFFFFFh	0000000h – 1FFFFFFFh
0	1	1	Upper 1/16	7800000h – 7FFFFFFFh	0FFFFFFFh – FFFFFFFFh	0000000h – 1FFFFFFFh
1	0	0	Upper 1/8	7000000h – 7FFFFFFFh	1FFFFFFFh – FFFFFFFFh	0000000h – 1FFFFFFFh
1	0	1	Upper 1/4	6000000h – 7FFFFFFFh	3FFFFFFFh – FFFFFFFFh	0000000h – 1FFFFFFFh
1	1	0	Upper 1/2	4000000h – 7FFFFFFFh	7FFFFFFFh – FFFFFFFFh	0000000h – 1FFFFFFFh
1	1	1	All	000000h – 7FFFFFFFh	000000h – FFFFFFFFh	0000000h – 1FFFFFFFh

Table 16: Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Gb	2Gb	4Gb
0	0	0	None	None	None	None
0	0	1	Lower 1/64	000000h – 01FFFFFFh	000000h – FBFFFFFFh	000000h – 07FFFFFFh
0	1	0	Lower 1/32	000000h – 03FFFFFFh	000000h – F7FFFFFFh	000000h – 0FFFFFFFh
0	1	1	Lower 1/16	000000h – 07FFFFFFh	000000h – EFFFFFFFh	000000h – 1FFFFFFFh
1	0	0	Lower 1/8	000000h – FFFFFFFFh	000000h – DFFFFFFFh	000000h – 3FFFFFFFh
1	0	1	Lower 1/4	000000h – 1FFFFFFFh	000000h – BFFFFFFFh	000000h – 7FFFFFFFh
1	1	0	Lower 1/2	000000h – 3FFFFFFFh	000000h – 7FFFFFFFh	000000h – FFFFFFFFh
1	1	1	All	000000h – 7FFFFFFFh	000000h – FFFFFFFFh	0000000h – 1FFFFFFFh

Table 17: Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status & Configuration Registers	Memory ¹ Array Protected Area	Memory ¹ Array Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	Low	Protected	Protected	Unprotected
1	1	High	Unprotected	Protected	Unprotected

Notes:

High: Logic '1'

Low: Logic '0'

X: Don't Care – Can be Logic '0' or '1'

Protected: Write protected

Unprotected: Writable

Note 1: Memory address range protection based on Block Protection Bits

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 18: Device Identification Register – Read Only

Bits	Avalanche Manufacturer's ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temp	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0010-HP Dual-Quad SPI	0001 - 3V	0010 - -40°C to 125°C	0110 - Reserved	00000001 - 108MHz
				1000 - 1Gb	
				1001 – 4Gb	
				1010 – 8Gb	



Serial Number Register (Read/Write)

Serial Number register is user writable.

Table 19: Serial Number Register – Read and Write

Bits	Name	Description	Read / Write	Default State ¹	Selection Options
SN[63:0]	SN	Serial Number Value	R/W	000000000000 0000h	Value stored is based on the customer

Notes:

1: The default value is how the device is shipped from the factory.

Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 20 : Unique ID Register – Read Only

Bits	Name	Description	Read / Write	Selection Options
UID[63:0]	UID	Unique Identification Number Value	R	Value stored is written in the factory and is device specific

Configuration Register 1 (Read/Write)

Configuration Register 1 (CR1) controls the output drive strength selection, locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register. In addition, CR1 controls the Write Enable protection (WREN – Status Register) reset functionality during memory array writing¹. This functionality makes SPI MRAM compatible to other SPI devices.

Table 21: Configuration Register 1 (CR1) – Read and Write

Bits	Name	Description	Read / Write	Default	Selection Options
CR3[7]	ODSEL[2]	Output Driver Strength Selector	R/W	0	000: 35Ω 001: 75Ω 010: 60Ω 011: 45Ω ¹ 100: 35Ω 101: 40Ω 110: 20Ω 111: 15Ω
CR3[6]	ODSEL[1]			1	
CR3[5]	ODSEL[0]			1	
CR3[4]	RSVD	Reserved	R	0	Reserved for future use
CR3[3]	RSVD	Reserved	R	0	Reserved for future use
CR1[2]	MAPLK	Memory Array Data Protection Lock Enable/Disable (TBSEL, BPSEL[2:0])	R/W	0	0: Memory Array Data Protection Unlocked 1: Memory Array Data Protection Locked
CR1[1]	WRENS[1]	WREN Reset Selector (Memory Array Write Functionality)	R/W	0	00: Normal: WREN is prerequisite to all Memory Array Write instruction. (WREN is reset after CS# goes High) 01: SRAM: WREN is not a prerequisite to Memory Array Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset once CS# goes High) 11: Illegal - Reserved for future use
CR1[0]	WRENS[0]			1	

Notes:

1: Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 1 settings. In other words, all register write instructions require WREN to be set and WREN resets once CS# goes High for the write instruction.

Configuration Register 2 (Read/Write)

Configuration Register 2 (CR2) controls the memory array access latency.

Table 22: Configuration Register 2 (CR2) – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR2[7]	RSVD	Reserved	R	0	Reserved for future use
CR2[6]	RSVD	Reserved	R	0	Reserved for future use
CR2[5]	RSVD	Reserved	R	0	Reserved for future use
CR2[4]	DSSEL		R	0	Reserved for future use
CR2[3]	MLATS[3]	Memory Array Read Latency Selection ¹	R/W	0	0000: 0 Cycles - Default 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles 1001: 9 Cycle 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	MLATS[2]			0	
CR2[1]	MLATS[1]			0	
CR2[0]	MLATS[0]			0	

Notes:

1: Latency is frequency dependent. Please consult Table 27, 28 and 29



Interrupt Configuration Register (Read/Write)

The Interrupt Configuration Register controls different events that trigger INT# pin transitioning from High to Low state. INT# pin can be configured in the INT# configuration register to transition to the active Low state when either ECC error is detected and corrected or transitioning from the busy to the ready state.

This register also enables access to 1 of 4 die sitting on the internal bus. The ECC engine can be tested by enabling the Test Enable bit and selecting 1 of 4 die.

Table 23: Interrupt Configuration Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
INTCR[7]	INTRF	Shows status of ECC error detection	W	0	Selection Options: 1: Unrecoverable ECC error detected 0: No unrecoverable ECC error detected
INTCR[6]	INTR	Clear Interrupt Status	W	0	Selection Options: 1 = Resets Interrupt caused by unrecoverable ECC 0 = No Action
INTCR[5]	ECC_CR	Reset the ECC Error Count Register	W	0	Selection Options: 1 = Resets ECC count register to 0 0 = No Action
INTCR[4]	----	Reserved	-	-	-
INTCR[3:2]	ECCDS	Die Selection	W	0	Die Select Options: 11 = Die 4 selected 10 = Die 3 selected 01 = Die 2 selected 00 = Die 1 selected
INTCR[1]	ECCTE	ECC Test Enable	W	0	ECC Test Engine Test mode: 1 = Enable 0 = Disable
INTCR[0]	ECCDS	ECC Error Detection Selection	W	0	Selection Options: 1 = ECC detection will transition a High to Low state on the INT# pin 0 = ECC detection will not transition the INT# pin

Error Correction Code (ECC) Test – Data Input Register

The contents of this register are entered into the ECC engine data buffer i.e. used as data input to test the ECC engine.

Table 24: ECC Test Data Input Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_In	Data Input	R/W	32'b0	Any value from 0x00000000 to 0xFFFFFFFF

Error Correction Code (ECC) Test – Error Injection

The contents of this register are used as an error mask to inject error to test the ECC engine.

Table 25: ECC Test Error Injection Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Error_Injection	Error Mask	R/W	32'b0	1 in any position injects an error into ECC engine. For example 0x00000003 will inject a two bit error in two LSB bits i.e. the Data in the ECC engine buffer is Exclusive or'd with the error mask.

Error Correction Code (ECC) Test – Data Output Register

The contents of this register are the output of the ECC engine when testing the ECC engine.

Table 26: ECC Test Data Output Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_Out	Output of ECC engine	R	32'b0	None – read only.

Error Correction Code (ECC) – Error Count Register

The Error Count Register is incremented when ECC errors are detected during normal memory read operations. An interrupt is generated on device pin INT# and the interrupt flag is set when an unrecoverable error is detected.

Table 27: ECC Count Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	Error_Count	Number of Errors detected and corrected	R	32'b0	None – read only

**Table 28: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)**

Read Type	Latency	Max Frequency
(1-1-1) SDR	8-15	108MHz
(1-1-1) DDR	8-15	54MHz
(1-4-4) SDR	8-15	108MHz
(1-4-4) DDR	8-15	54MHz
(4-4-4) SDR	8-15	108MHz
(4-4-4) DDR	8-15	54MHz

Table 29: Memory Read Latency Cycles vs. Maximum Clock Frequency (without XIP)

Read Type	Latency	Max Frequency
(1-1-1) SDR	0	50MHz

Table 30 : Read Any Register Command Latency Cycles vs. Maximum Clock Frequency

Read Type	Latency Cycles	Max Frequency
(1-1-1) SDR	8	108MHz
(1-4-4) SDR	2	108MHz
(4-4-4) SDR	2	108MHz

Instruction Set

Table 31: Instruction Set

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-4-4)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite
1	No Operation	NOOP 00h	•						•				108 MHz	
2	Write Enable	WREN 06h	•						•				108 MHz	
3	Write Disable	WRDI 04h	•						•				108 MHz	
4	Enable QPI	QPIE 38h	•		•				•				108 MHz	
5	Enable SPI	SPIE Fh	•				•		•				108 MHz	
6	Read Status Register	RDSR 05h		•					•			1	54 MHz	
7	Read Device ID	RDID 9Fh		•					•			4	54 MHz	
8	Read Any Register - Address Based	RDAR 65h			•				•		•	1 to 8	108 MHz	
9	Write Status Register	WRSR 01h		•					•			1	108 MHz	WREN
10	Write Any Register - Address Based	WRAR 71h			•				•			1 to 8	108 MHz	WREN
11	Read Memory Array - SDR	READ 03h			•				•			1 to ∞	50 MHz	

1Gbit – 8Gbit Dual-Quad SPI P-SRAM Memory

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-4-4)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite
12	Fast Read Memory Array - SDR	RDFT 0Bh			•		•	•	•		•	1 to ∞	108 MHz	
13	Fast Read Memory Array - DDR	DRFR 0Dh			•		•	•		•	•	1 to ∞	54 MHz	
14	Read Quad I/O Memory Read - SDR	RDQI EBh				•		•	•		•	1 to ∞	108 MHz	
15	Read Quad I/O Memory Read - DDR	DRQI EDh				•		•		•	•	1 to ∞	54 MHz	
16	Write Memory Array - SDR	WRTE 02h			•		•		•			1 to ∞	108 MHz	WREN
17	Fast Write Memory Array - SDR	WRFT DAh			•		•	•	•			1 to ∞	108 MHz	WREN
18	Fast Write Memory Array - DDR	DRFW DEh			•			•		•		1 to ∞	54 MHz	WREN
19	Write Quad I/O Memory Array - SDR	WQIO D2h				•		•	•			1 to ∞	108 MHz	WREN
20	Write Quad I/O Memory Array - DDR	DWQO D1h				•		•		•		1 to ∞	54 MHz	WREN

Notes:

1: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O Dual-Quad SPI device 1 (SI / IO[0] or SO / IO[1]) and Dual-Quad SPI device 2 (SI / IO[04] or SO / IO[7]). On the other hand, 1-4-4 represents command being sent on a single I/O Dual-Quad SPI device 1 (SI / IO[0]) and Dual-Quad SPI device 2 (SI / IO[4]) - address/data being sent on four I/Os of Dual-Quad SPI device 1 (IO[3:0]) and Dual-Quad SPI device 2 (IO[7:4])

2: XIP allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. A special mode byte must be entered after the address bits to enable/disable XIP – Axh / Fxh.

3: Fast Read instruction must include Latency cycles to meet higher frequency. They are configurable (Configuration Register 2 – CR2[3:0]) and frequency dependent.

4: WREN prerequisite for array writing is configurable (Configuration Register 1 – CR1[1:0])

Instruction Description and Structures

All communication between a host and ASxxxx208 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from ASxxxx208. All command, address and data information is transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic '1').
- CLK marks the transfer of each bit.
- Each instructions starts out with an 8-bit command. The command selects the type of operation ASxxxx208 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location or register. The address is 32-bit wide.
 - SDR: The address is transferred on the rising edges of CLK.
 - DDR: The address is transferred on both edges of the CLK in DDR.
- The address bits are followed by data bits. For Write instructions:
 - SDR: Write data bits to ASxxxx208 are transferred on the rising edges of CLK.
 - DDR: Write data bits to ASxxxx208 are transferred on both edges of CLK.
- In normal operational mode, Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction. ASxxxx208 offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array. These modes are set in Configuration Register 1.
- Similar to write instructions, the address bits are followed by data bits for read instructions:
 - SDR: Read data bits from ASxxxx208 are transferred on the falling edges of CLK.
 - DDR: Read data bits from ASxxxx208 are transferred on both edges of CLK. The start of read data transfer is always on the falling edge of the CLK.
- ASxxxx208 is a high performance serial memory and at higher frequencies, read instructions require latency cycles to compensate for the memory array access time. The number of latency cycles required depends on the operational frequency and is configurable – Configuration Register 2. The latency cycles are inserted after the address bits before the data comes out of ASxxxx208.
- For Read and Write instructions, ASxxxx208 offers XIP mode. XIP allows similar instructions to be executed sequentially without incurring the command cycles overhead. XIP is enabled by entering byte Axh and disabled by entering byte Fxh. These respective bytes must be entered following the address bits.

- The entire memory array can be read from or written to using a single read or write instruction. After the starting address is entered, subsequent address are internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.
- Read Data Strobe (DS) is used as an additional output signal, driven by the MRAM, to synchronize with other data outputs to validate data transition. DS is edge-aligned with output data and is always enabled in the DDR read operation.

Figure 12 to Figure 17 show the description of SDR instruction types supported.

Figure 12: Description of (1-0-0) Instruction Type

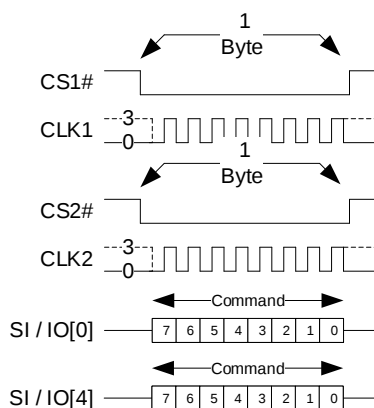


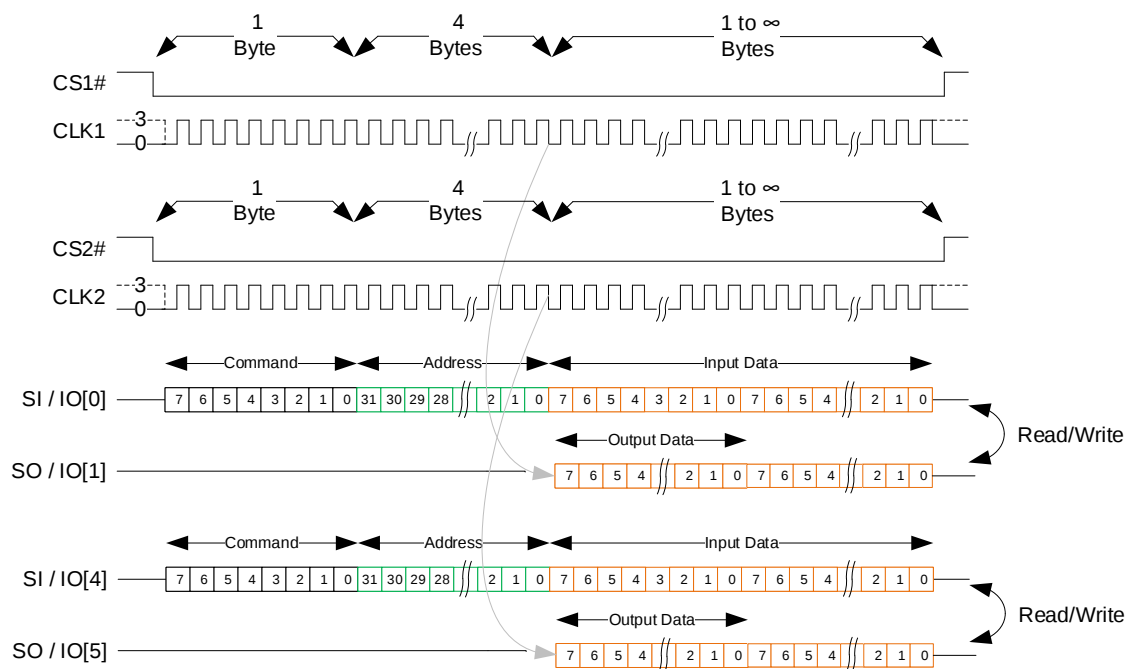
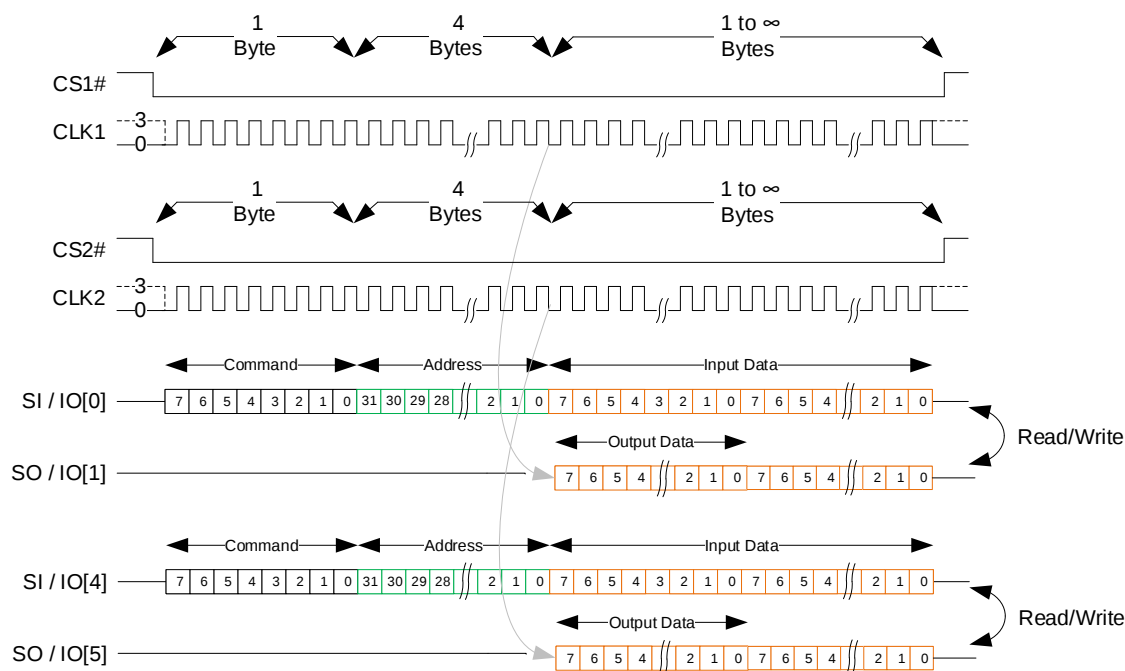
Figure 13: Description of (1-0-1) Instruction Type

Figure 14: Description of (1-1-1) Instruction Type (Without XIP)


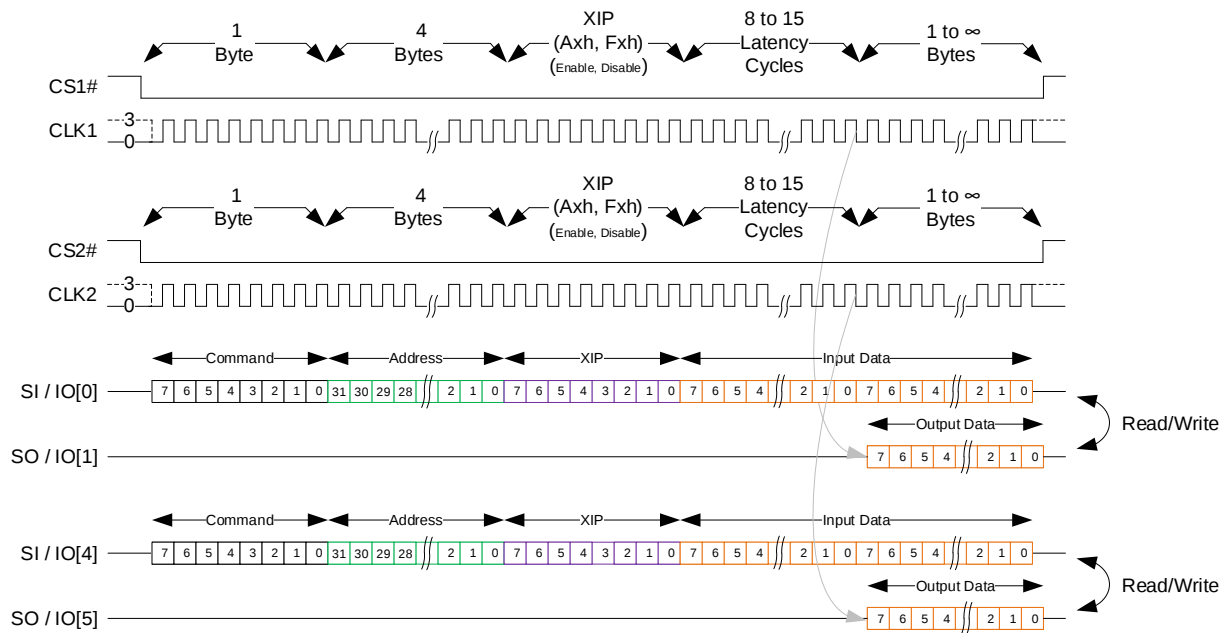
Figure 15: Description of (1-1-1) Instruction Type (With XIP)




Figure 16: Description of (1-4-4) Instruction Type with XIP

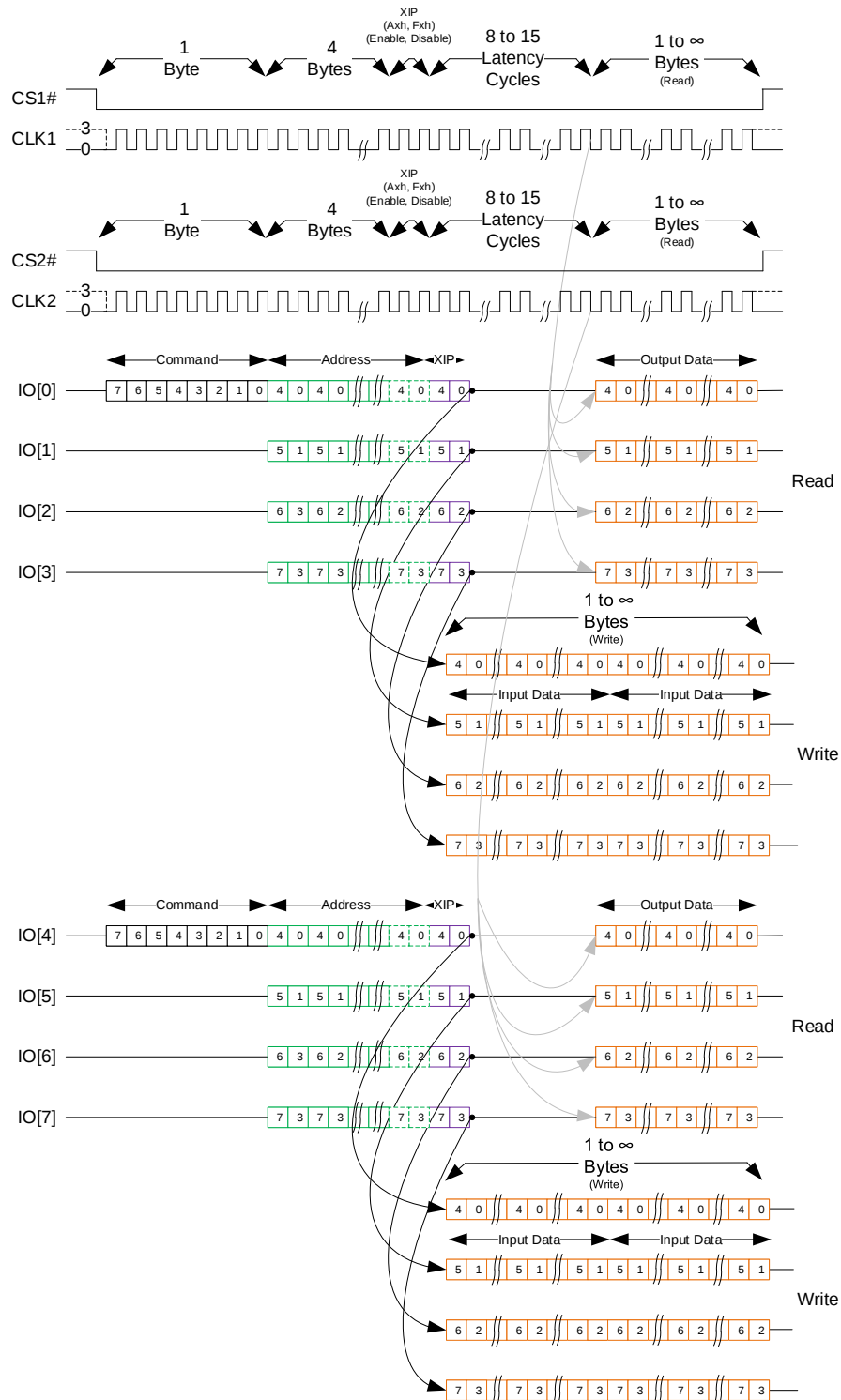


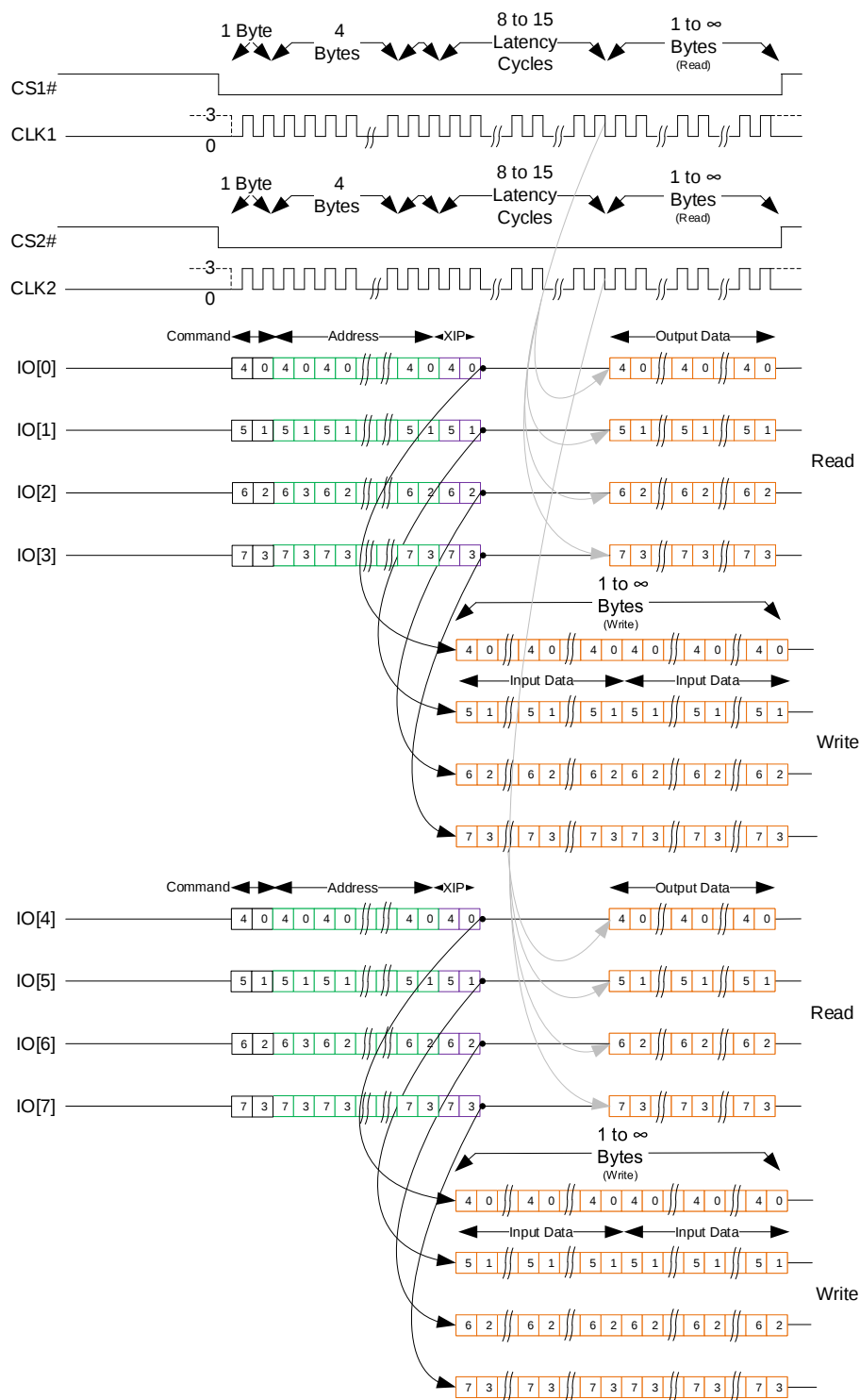
Figure 17: Description of (4-4-4) Instruction Type with XIP


Figure 18 to Figure 19 show the description of DDR instruction types supported.

Figure 18: Description of (1-1-1) DDR Instruction Type (With XIP)

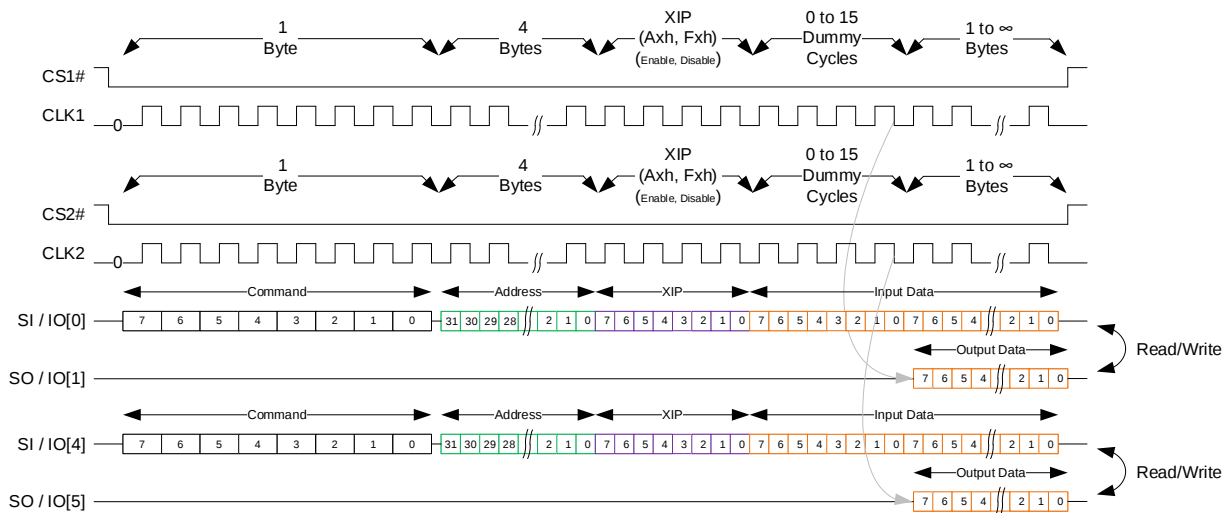
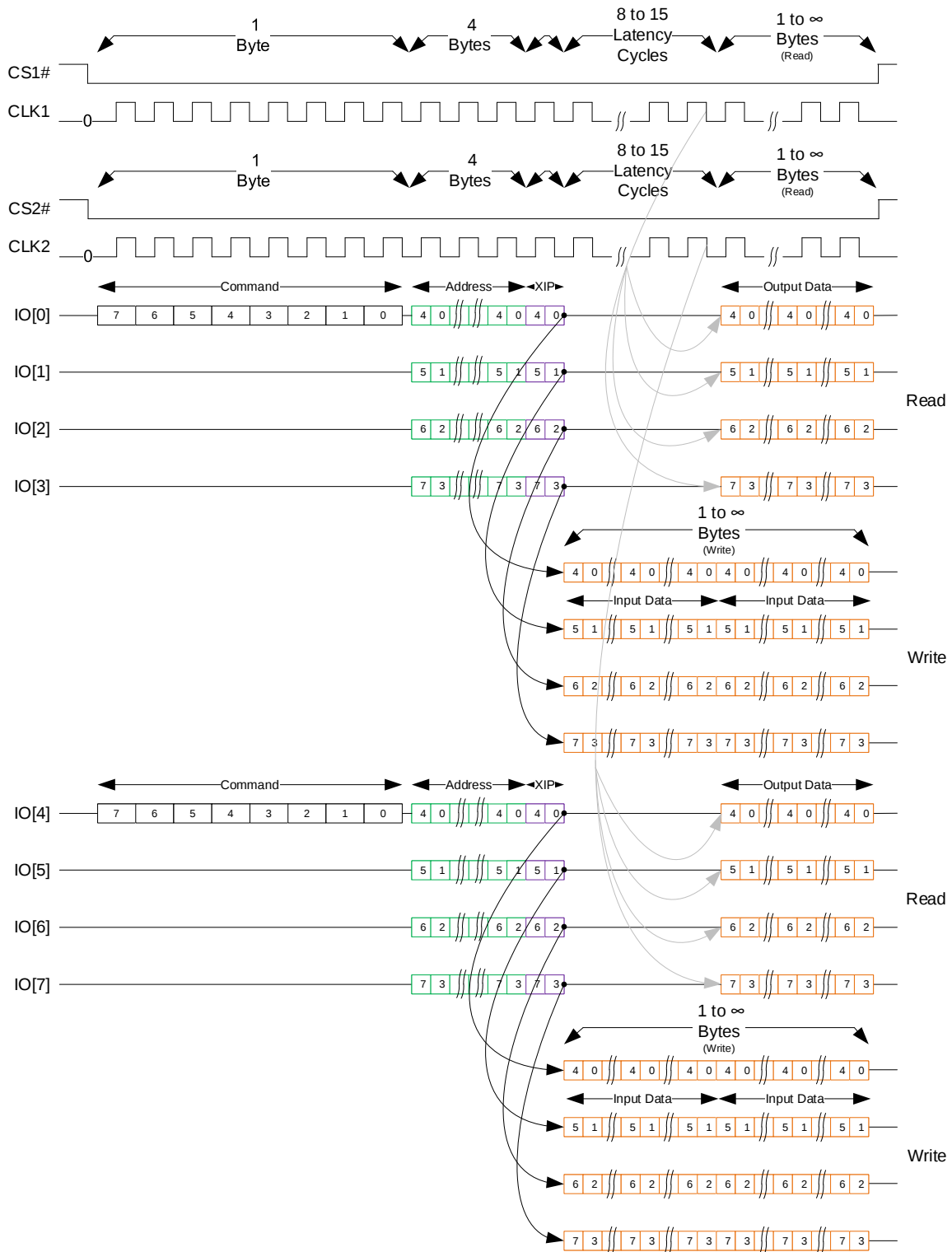


Figure 19: Description of (1-4-4) DDR Instruction Type (With XIP)




Electrical Specifications

Table 32: Recommended Operating Conditions

Parameter / Condition	Minimum	Typical	Maximum	Units
Operating Temperature (T _A)	-40.0	-	125.0	°C
V _{CC} Supply Voltage	2.7	3.0	3.6	V
V _{CCIO} Supply Voltage	1.71	1.8 - 3.0	3.6	V
V _{SS} Supply Voltage	0.0	0.0	0.0	V
V _{SSIO} Supply Voltage	0.0	0.0	0.0	V
V _{DD} Supply Voltage	0.9	1.0	1.05	V
V _{DD2} Supply Voltage	0.9	1.0	1.05	V

Table 33: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V _{IN} = 3.0V	C _{IN}	5.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V _{IN} = 3.0V	C _{INOUT}	6.0	pF

Table 34: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10 ¹⁶	cycles
Data Retention	RET	85°C	20	years

Table 35: DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			Units
				Minimum	Typical ¹	Maximum	
Active Read Current	I _{READ1}	V _{CC} = 3.6V, CLK=108MHz (1-4-4)	1Gb	-	55	200	mA
			2Gb	-	55	200	mA
			4GB	-	75	280	mA
			8Gb	-	115	440	mA
Active Write Current	I _{WRITE1}	V _{CC} = 3.6V, CLK=108MHz (1-4-4)	1Gb	-	60	210	mA
			2Gb	-	60	210	mA
			4GB	-	80	290	mA
			8Gb	-	120	450	mA
Active Read Current	I _{READ2}	V _{CC} = 3.6V, CLK=108MHz (4-4-4)	1Gb	-	55	200	mA
			2Gb	-	55	200	mA
			4GB	-	75	280	mA
			8Gb	-	115	440	mA
Active Write Current	I _{WRITE2}	V _{CC} = 3.6V, CLK=108MHz (4-4-4)	1Gb	-	60	210	mA
			2Gb	-	60	210	mA
			4GB	-	80	290	mA
			8Gb	-	120	450	mA
Standby Current	I _{SB}	V _{CC} = 3.6V, CLK=V _{CCIO} , CS#=V _{CCIO} , SI=WP#=V _{CCIO}	1Gb	-	35	180	mA
			2Gb	-	35	180	mA
			4GB	-	55	260	mA
			8Gb	-	95	420	mA
VDD Standby Current	I _{VDDSB}	V _{CC} =3.6V, V _{CCIO} =3.6V	-	5	10	mA	
VDD Read Current	I _{VDDR}	V _{CC} =3.6V, V _{CCIO} =3.6V	-	10	50	mA	
VDD Write Current	I _{VDDW}	V _{CC} =3.6V, V _{CCIO} =3.6V	-	10	50	mA	
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CCIO} (max)	-	-	±1.0	µA	
Output Leakage Current	I _{LO}	V _{OUT} =0 to V _{CCIO} (max)	-	-	±1.0	µA	
Input High Voltage	V _{IH}		0.7xV _{CCIO}	-	V _{CCIO} +0.3	V	
Input Low Voltage	V _{IL}		-0.3	-	0.3xV _{CCIO}	V	
Output High Voltage Level	V _{OH}	I _{OH} = -100µA	V _{CCIO} -0.2	-	-	V	
		I _{OH} = -1mA	2.4	-	-	V	
Output Low Voltage Level	V _{OL}	I _{OL} = 150µA	-	-	0.2	V	
		I _{OL} = 2mA	-	-	0.4	V	

Note 1: Typical values are at 25°C

Table 36: Magnetic Immunity Characteristics

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	$H_{\text{max_write}}$	24000	A/m
Magnetic Field During Read	$H_{\text{max_read}}$	24000	A/m

Table 37: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CCIO}
Input rise and fall times	3.0ns
Input and output measurement timing levels	$V_{\text{CCIO}}/2$
Output Load	$CL = 30.0\text{pF}$



Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 38: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Temperature Under Bias	-45	130	°C
Storage Temperature	-55 to 150		°C
Supply Voltage Vcc relative to Vss	-0.5	4.0	V
Voltage on any pin except V _{DD} and V _{DD2}	-0.5	Vcc + 0.4	V
Voltage on V _{DD} and V _{DD2}	0.9	1.05	V
DC output current I _{out}	± 20		mA
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ 2000 V		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ 500 V		V
Latch-Up (I-test) JESD78	≥ 100 mA		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---



CS# Operation & Timing

Figure 20: CS# Operation & Timing

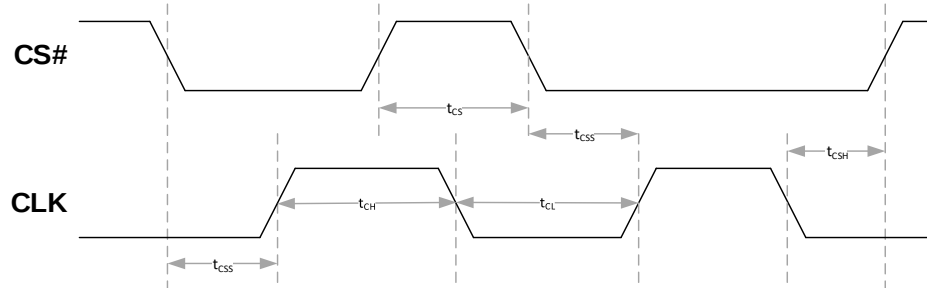


Table 39: SDR CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	108 (SDR)	MHz
Clock Low Time	t_{CL}	$0.45 * 1 / f_{CLK}$	-	ns
Clock High Time	t_{CH}	$0.45 * 1 / f_{CLK}$	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Write Cycle (SPI)	t_{CS3}	250	-	ns
Chip Deselect Time after Write Cycle (QPI)	t_{CS5}	420	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:

Power supplies must be stable

1:SDR operation only

Table 40: DDR CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1.0	54 (DDR)	MHz
Clock Low Time	t_{CL}	$0.45 * 1 / f_{CLK}$	-	ns
Clock High Time	t_{CH}	$0.45 * 1 / f_{CLK}$	-	ns
CS# High Time (End of Read)	t_{CS1}	20.0	-	ns
CS# High Time (End of Memory Array Write) SPI	t_{CS3}	120.0	-	ns
CS# High Time (End of Memory Array Write) QPI	t_{CS5}	120.0	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5.0	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4.0	-	ns

Notes:

Power supplies must be stable

Command, Address, XIP and Data Input Operation & Timing

Figure 21: SDR Command, Address and Data Input Operation & Timing

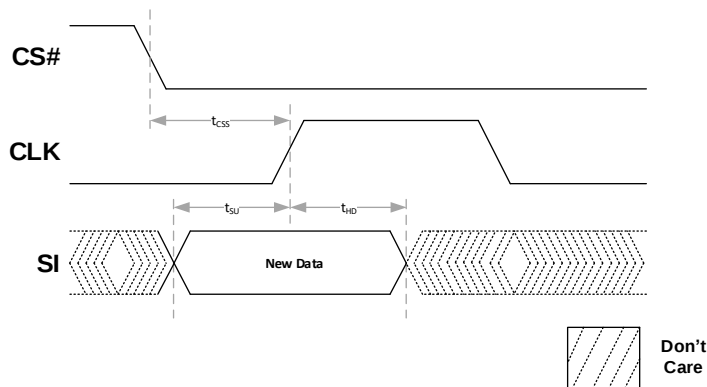


Table 41: SDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	2.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	3.0	-	ns

Notes: Power supplies must be stable

Figure 22: DDR Command, Address and Data Input Operation & Timing

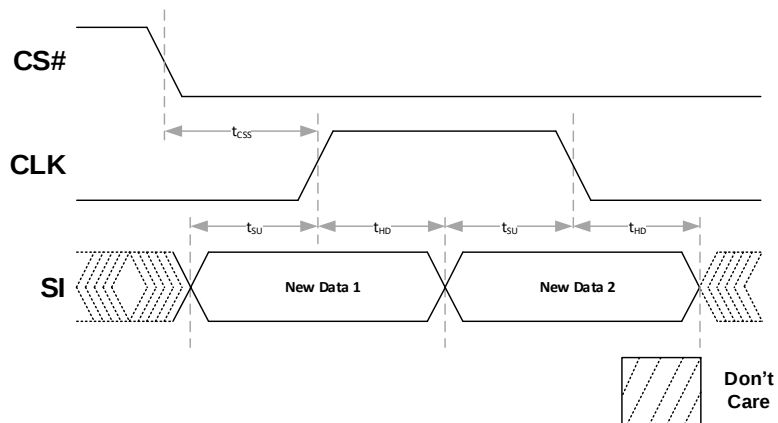


Table 42: DDR Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	4.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	4.0	-	ns

Notes: Power supplies must be stable

Data Output Operation & Timing

Figure 23: SDR Data Output Operation & Timing

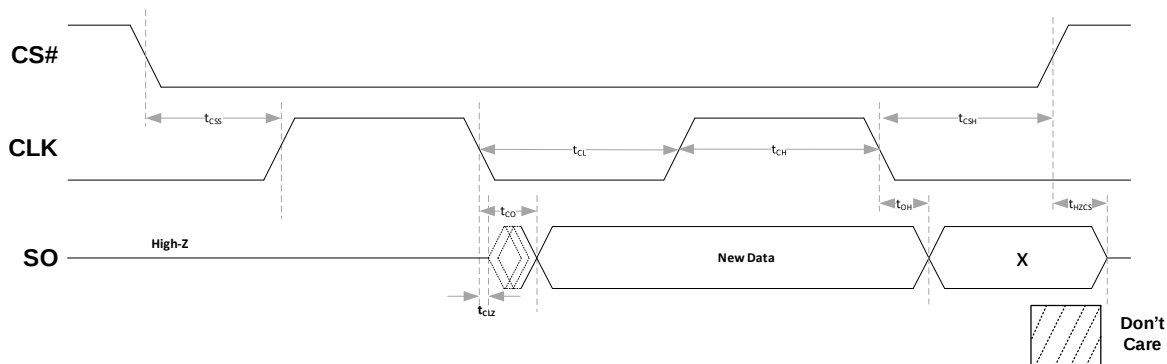
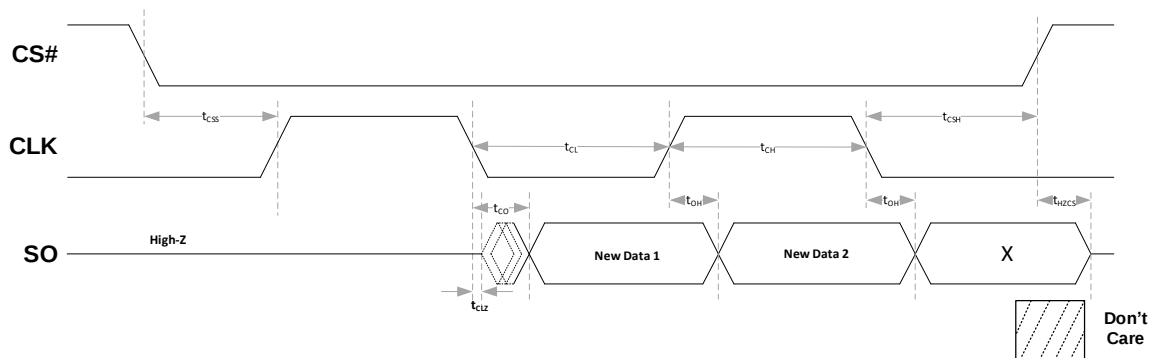


Table 43: SDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	7.0	ns

Notes:

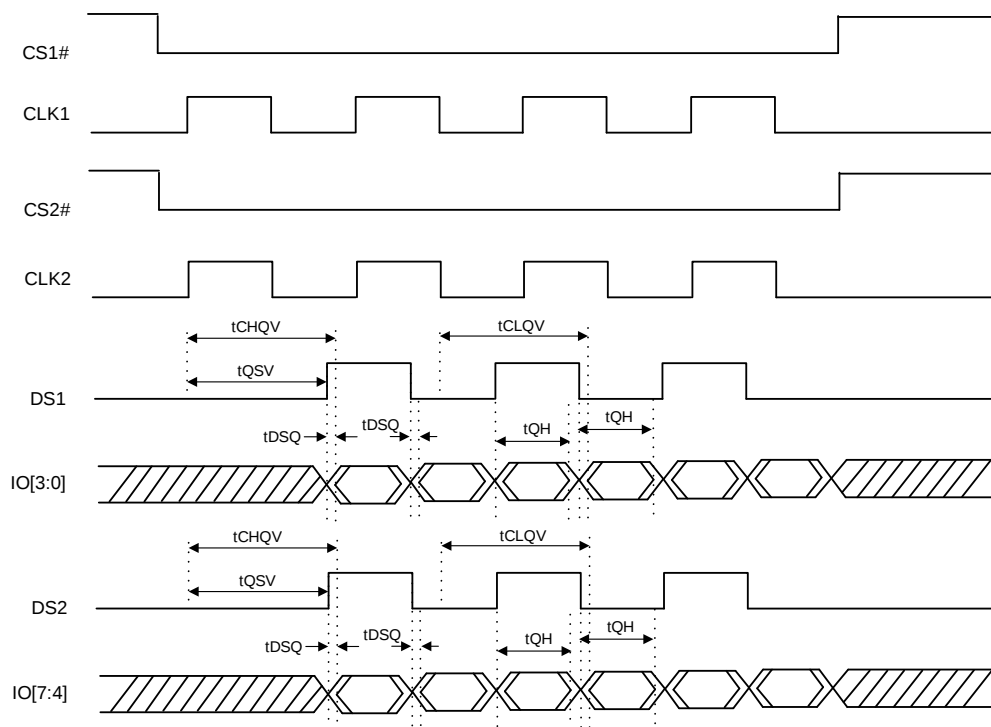
Power supplies must be stable

Figure 24: DDR Data Output Operation & Timing

Table 44: DDR Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	6.0	ns

Notes:

Power supplies must be stable

Figure 25: DDR Data Strobe (DS) Output Timing

Table 45: DDR Data Strobe (DS) Output Timing

Parameter	Symbol	Minimum	Maximum	Units
Clock Transient to Output Valid (30pF Loading)	t_{CLQV} / t_{CHQV}	-	5.0	ns
I/O Valid Skew Related to DS (30pF Loading)	t_{DSQ}	-	1.0	ns
I/O Hold Time Related to DS	t_{QH}	$(t_{CL} / t_{CH}) - t_{QHS}$	-	ns
I/O Hold Skew Factor (30pF Loading)	t_{QHS}	-	1.0	ns
DS Clock Transient to DS Valid Time	t_{QSV}	-	5.0	ns

WP# Operation & Timing

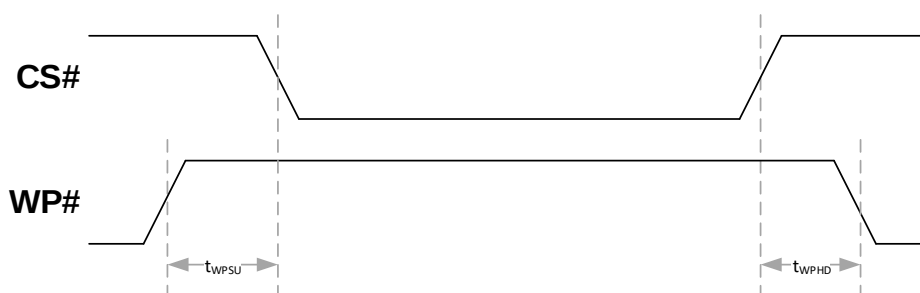
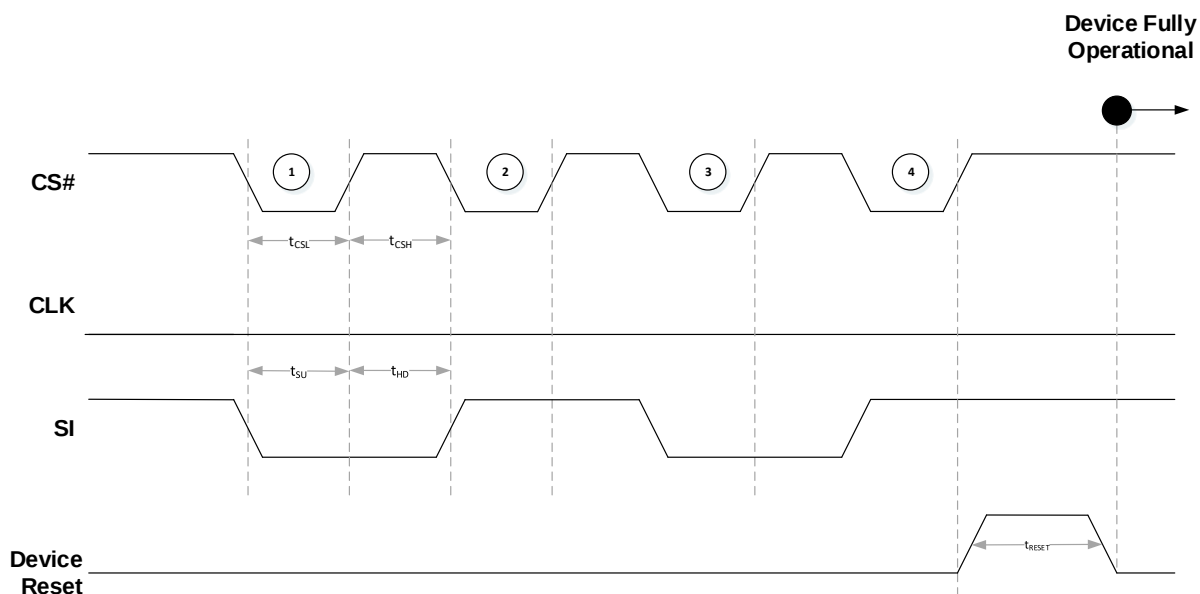
Figure 26: WP# Operation & Timing


Table 46: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:

Power supplies must be stable

JEDEC Reset Operation & Timing
Figure 27: JEDEC Reset Operation & Timing

Table 47: JEDEC Reset Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CS# Low Time	t_{CL}	1.0	-	μ s
CS# High Time	t_{CH}	1.0	-	μ s
SI Setup Time (w.r.t CS#)	t_{SU}	5.0	-	ns
SI Hold Time (w.r.t CS#)	t_{HD}	5.0	-	ns
JEDEC Hardware Reset	t_{RESET}	-	450.0	μ s

Notes:

Power supplies must be stable



Thermal Resistance

Table 48: Thermal Resistance Specifications

Parameter	Description	Test Conditions	88 Ball FBGA (1Gb)				Unit
			1Gb	2Gb	4Gb	8Gb	
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	17.89	17.89	17.90	TBD	°C/W
θ_{JC}	Thermal resistance (junction to case)		2.10	2.10	2.19	TBD	

Notes:

- 1: These parameters are guaranteed by characterization; not tested in production.
- 2: Ambient temperature, T_A 25 °C
- 3: Worst case Junction temp specified for Top die (θ_{JA}) and Bottom die (θ_{JC})

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Revision History

Revision	Date	Change Summary
REV A	01/10/2022	Initial release Package pinout updated to reflect Dual QSPI Removed DS1 & DS2 (Will not require a data strobe at these frequencies) Added 2 interrupt pins to the package Added 2Gb to the densities supported
REV B	3/30/2022	Changed signal description of Vccio. It wasn't clear that it is referring to I/O supply. Removed option of 1.8V Vcc supply Updated package pin definition: Changed Vccq to Vccio Added Pin assignment table Removed Deep Power down Enter and Exit commands Changed DDR max freq. from 80MHz to 54MHz Defined V _{DD2} for 8Gb devices as Ball J6. This is a NC ball on the 1, 2 & 4Gb devices. Changed density field from 4 digits to 3 digits in part number. Added V _{DD} Currents to DC Characteristics
	05/16/2022	Updated DC Characteristics Table: Current numbers are based on UMC's analysis of their current 22nm process. Added V _{DD} to supply line on Front page
	05/23/2022	Updated Ball assignment table: N12 was not shown as Vss Updated Power sequencing description under DEVICE INITIALIZATION Added Absolute Maximum Ratings Table Called out specific voltages are allowed for V _{CCIO} on front page.
	05/25/2022	Added Thermal Resistance table Added Absolute Maximum Rating on V _{DD} and V _{DD2} Changed the height of the package to allow for stacking of 8 rather than 4 devices. This increase nominal height "A" from 1.39 to 1.85
REV C	06/01/2022	Changes the outer limit of package dimension to allow compatibility between 1-4 and 8Gb densities. See Figure 5. See Changes to E and E2. Changed the nominal height "A" to be compatible with Gen 3 parallel devices: Nominal Height/Thickness in Figure 5 changed to 1.43 Leaded ball options added to Order Option table
	07/20/2022	Removed Performance Table Added Figures to ToC Added Tables to ToC Updated SDR Data Output Operation & Timing Updated DDR Data Output Operation & Timing Renamed from 88Ball to 96Ball (Included mechanical support balls) Added Extended Safe Operating Area as well as Normal Operating Conditions