Space Grade Parallel Persistent SRAM Memory

(AS301GB32, AS304GB32)

Features

- Interface
  - Parallel Asynchronous x32
- Technology
  - pMTJ STT-MRAM
    - Virtually unlimited Endurance and Data Retention (see Table 16)
- Density
  - 1Gb, 4Gb
- Memory Array Organization
  - 1Gb
    - 33,554,432 x 32
  - 4Gb
    - 134,217,728 x 32
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.0V, 3.3V ***
- Operating Temperature Range
  - -40°C to 125°C
- Packages
  - 142-ball FBGA (15mm x 17mm)
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

* Leaded Balls available

** PEMS-INST-001 Flow available as custom option

*** V_{CCIO} can be set to any voltage within the following range: 1.71V – 3.60V

Table of Contents

General Description

AS3xxx332 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in 1Gbit and 4Gbit. MRAM technology is analogous to Flash technology with SRAM compatible 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution. Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @85°C.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, high endurance, high performance and scalable memory technology.

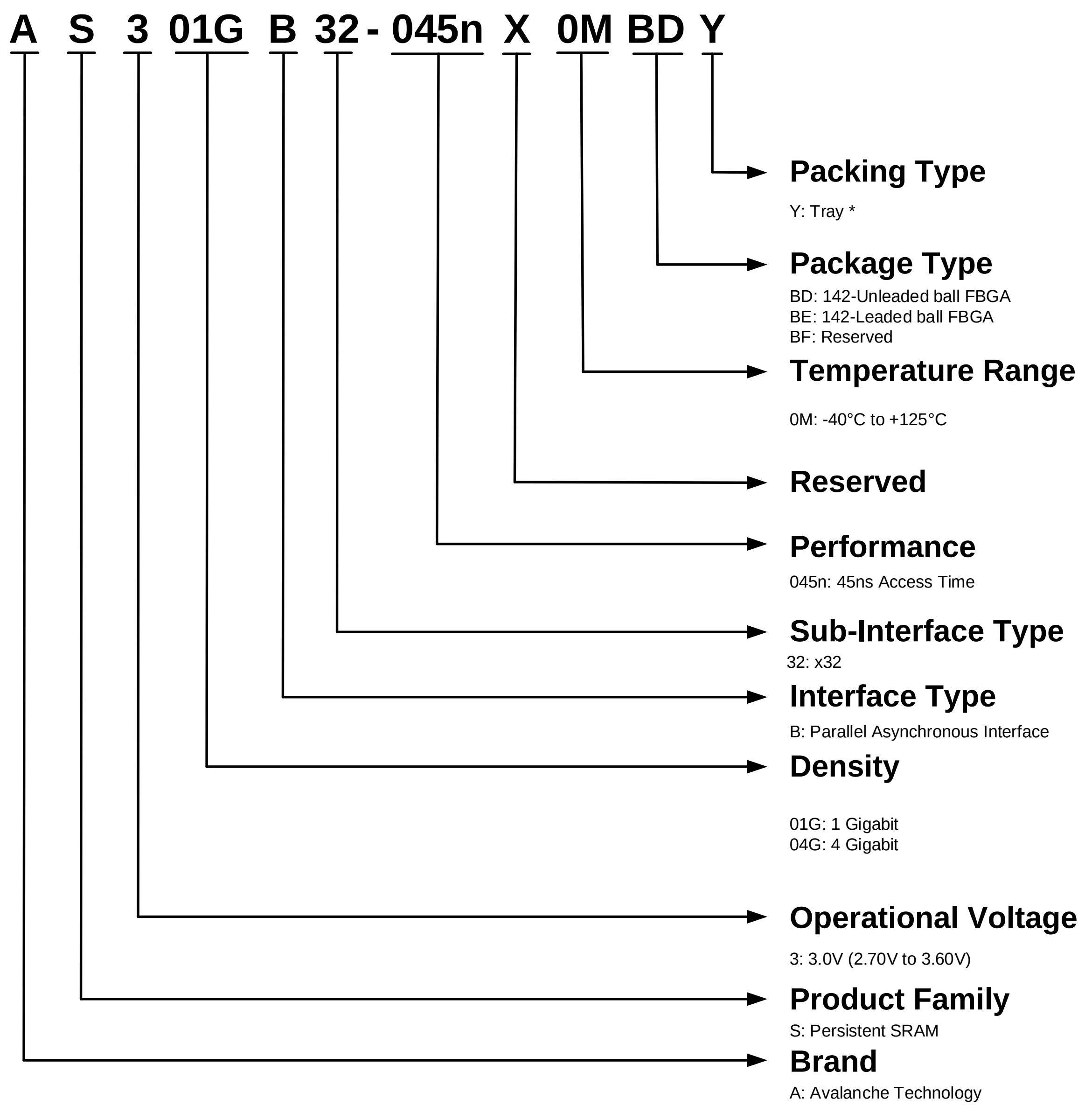
AS3xxx332 is available in small footprint (15mm x 17mm) 142 ball BGA package.

AS3xxx332 is offered with industrial extended (-40°C to 125°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Part Number Ordering Options



* Tape & Reel available as custom option: Contact your sales representative for an official quote

Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2: Valid Combinations List

Valid Combinations – 45ns				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS301GB32-045nX	0M	BD	Y	AS301GB32-045nX0MBDY
AS304GB32-045nX	0M	BD	Y	AS304GB32-045nX0MBDY
AS301GB32-045nX	0M	BE	Y	AS301GB32-045nX0MBEY
AS304GB32-045nX	0M	BE	Y	AS304GB32-045nX0MBEY

Signal Description and Assignment

Figure 2: Device Pinout

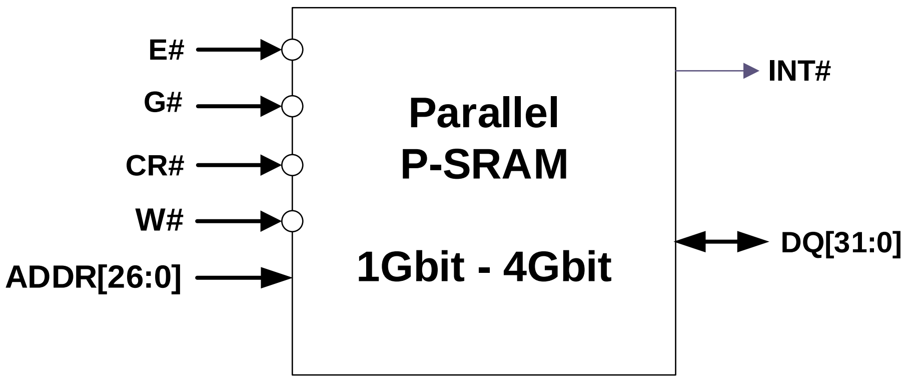


Table 3: Signal Description

Signal	Ball Assignment	Type	Description
E#	P8	Input	**Chip enable:** Enables or disables the MRAM.
G#	P7	Input	**Output enable:** Enables the output drivers for data transfer I/Os.
CR#	J2	Input	**Configuration Register enable:** Enables access to the Configuration registers
W#	M8	Input	**Write enable:** Transfers serial data from the host system to the MRAM when Low (Logic '0').Transfers serial data from the MRAM to the host system when High (Logic '1').
ADDR[26:0]	M2, L4, K13, M3, L3, M7, P12, L12, N11, N6, P6, L13, M13, P10, N10, M12, N13, L11, M11, P5, P3, N5, N4, M4, N2, N9, M9	Input	**Address:** I/Os for address transfer 1G: ADDR[24:0] – 25 Address pins for 1Gb x32 devices.* 4G: ADDR[26:0] – 27 Address pins for 4Gb x32 devices.
DQ[31:0]	E2, F2, D2, E3, E12, D10, C9, C7, G4, G3, F13, D13, C10, E8, F6, E5, E13, G11, E10, F9, C8, C6, D6, D4, G12, C12, D11, D9, E7, C5, D5, C3	Input / Output	**Data inputs/outputs:** The bidirectional I/Os transfer data [15:0].

Signal	Ball Assignment	Type	Description
INT#	G13	Output	**Interrupt:** Output generated by the MRAM when an unrecoverable ECC error is detected during read operation (output goes low on error).
V_{CCIO}	F12, J12, E11, M10, D8, N8, D7, N7, M5, E4, F3, J3	Supply	I/O power supply.
V_{SSIO}	F10, L10, E9, L9, F8, L8, F7, L7, E6, L6, G5,	Supply	I/O ground supply.
V_{CC}	C13, P13, D12, N12, C11, F11, H11, J11, K11, P11, C4, F4, H4, J4, K4, P4, D3, N3, C2, P2	Supply	Core power supply.
V_{SS}	A14, B14, C14, H13, R14, T14, A13, T13, A12, G10, H10, J10, K10, F5, L5, A2, T2, A1, B1, R1, T1	Supply	Core ground supply.
DNU	J13, H12, K12, P9, M6, H5, J5, K5, H3, G2, H2, K2, L2		**Do Not Use:** DNUs must be left unconnected.
RFU	K3		**Reserved for Future Use:** requires to have an external pull-up resistor (10KΩ)

* Unused ADDR[26:25] balls should be connected to Ground

Package Options

142-Ball FBGA (Bottom View)

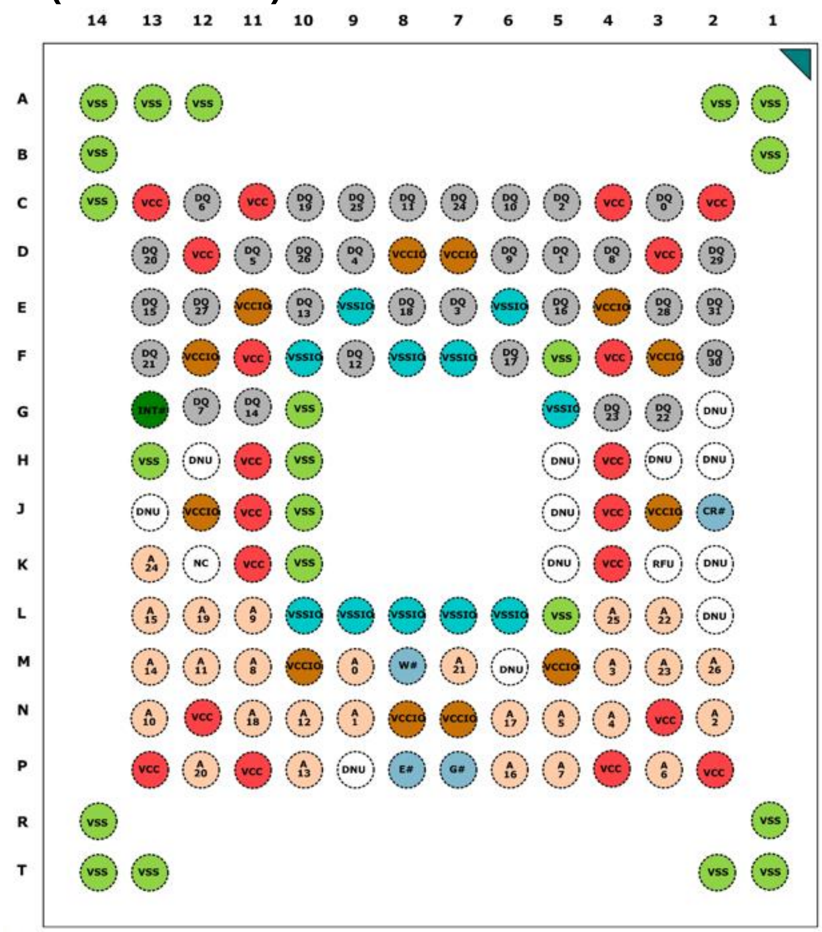
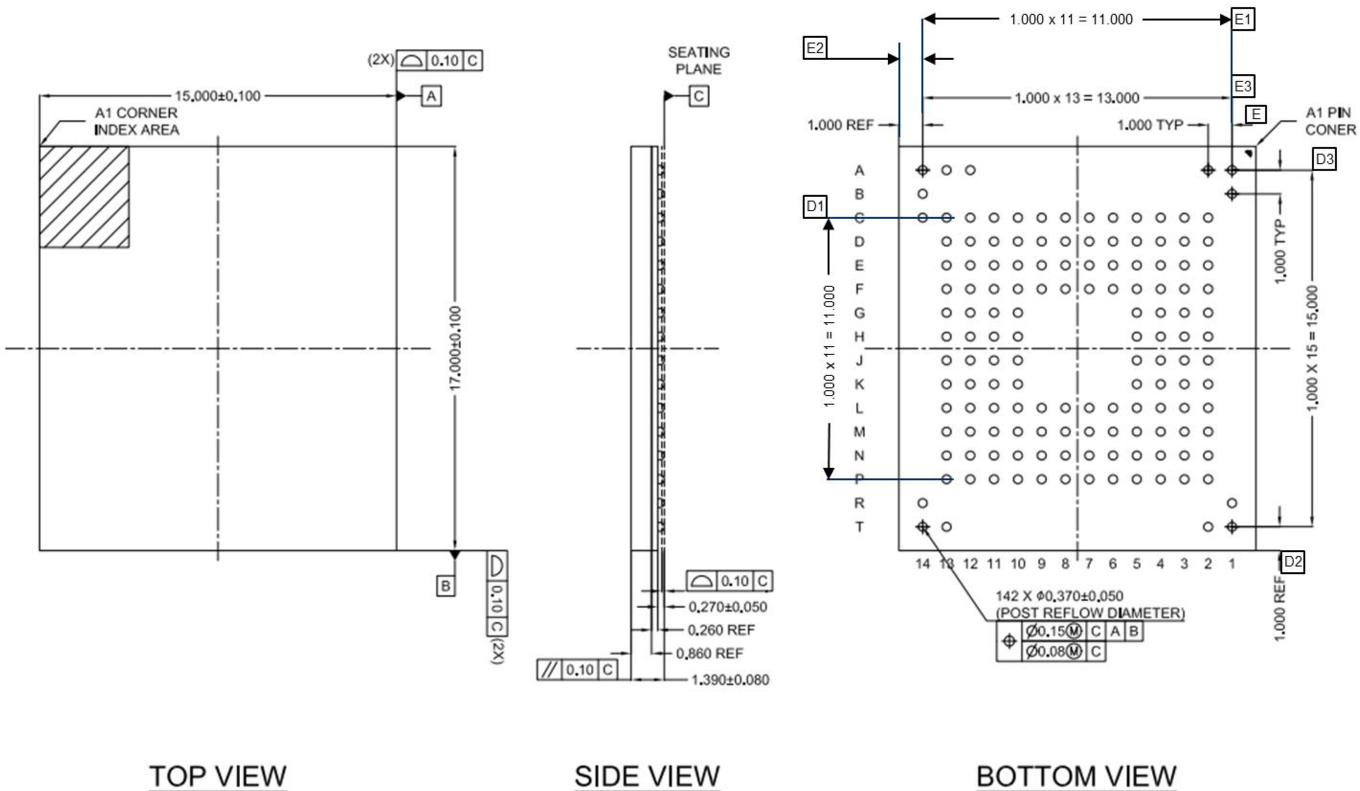


Figure 3: 142-ball FBGA

142-Ball FBGA

Figure 4: 142-ball FBGA



Architecture

AS3xxx332 is a high performance MRAM device. Writing to and reading from the device are performed as follows:

To write to the device, drive Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[31]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[26]).

To read from the device, drive Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[26]) to appear on I/O pins (DQ[0] to DQ[31]).

Figure 5: Functional Block Diagram

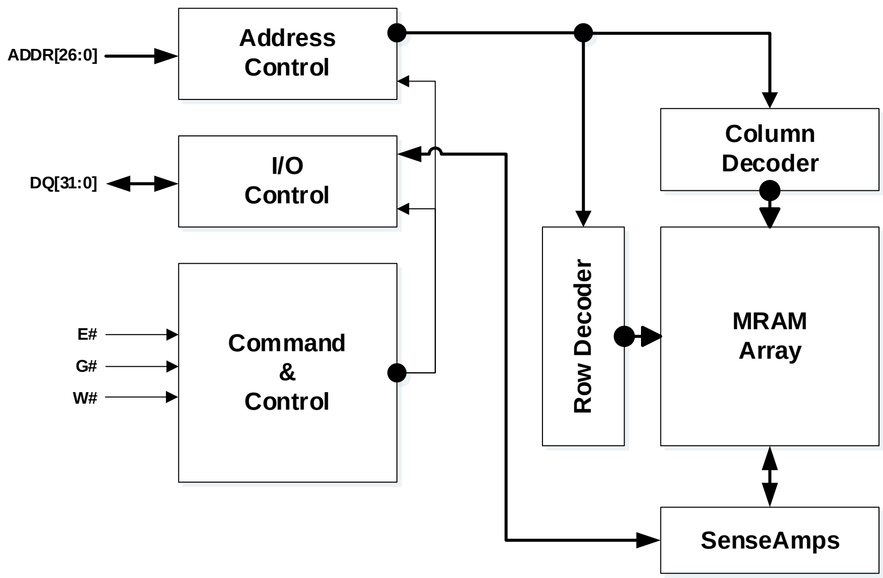


Table 4: Modes of Operation

Mode	E#	G#	W#	Current	DQ[31:0]
Not Selected	H	X	X	I_{SB}	Hi-Z
Output Disabled	L	H	H	I_{READ}	Hi-Z
Output Disabled	L	X	X	I_{READ}	Hi-Z
Read Word	L	L	H	I_{READ}	Data-out
Write Word	L	X	L	I_{WRITE}	Data-in

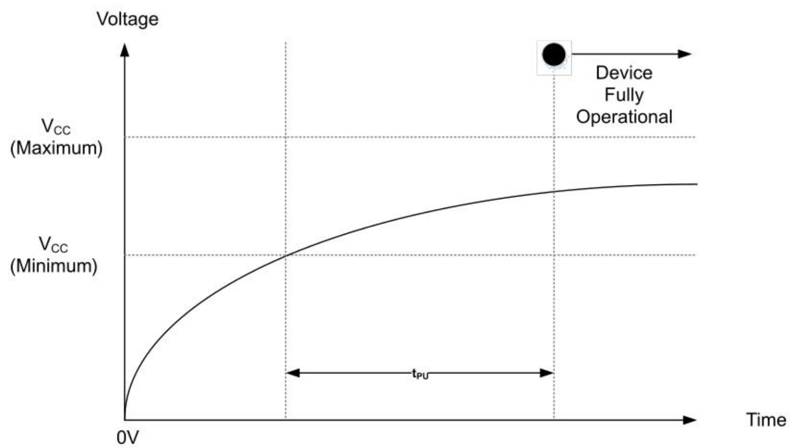
Notes:
H: High (Logic '1') X: Don't Care
L: Low (Logic '0') Hi-Z: High Impedance

Normal Device Initialization:

When powering up, the following procedure is required to initialize the device correctly:

- V_{CC} and V_{CCIO} can ramp up together (R_{VR}), if not possible then V_{CC} first followed by V_{CCIO}. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-up (E# must follow the applied voltage on V_{CC} (a 10KΩ pull-up Resistor to V_{CC} is recommended)) until V_{CC} reaches V_{CC}(minimum) and then a further delay of t_{PU} (Figure 8).
- During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences (Figure 9).

Figure 6: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- V_{CC} and V_{CCIO} can ramp down together (R_{VF}), if not possible then V_{CC} first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-down (E# must follow V_{CC} during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended)) until V_{CC} reaches VSS.
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, when V_{CC} goes below $V_{CC-CUTOFF}$. The voltage must drop below V_{CC}(Reset) for a period of t_{PD}. The power-up timing needs to be observed after V_{CC} goes above V_{CC}(minimum)

Figure 9: Power-Down Behavior

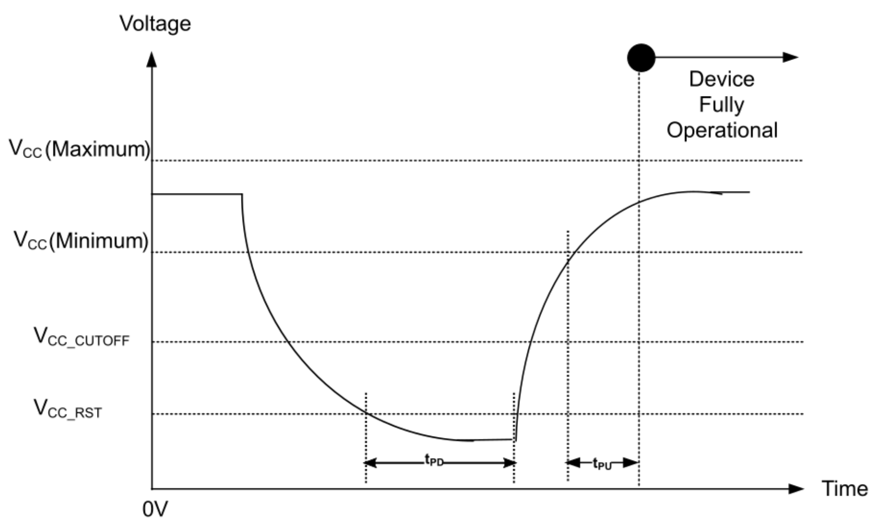


Table 4: Power Up/Down Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		1	-	-	ms
V_{CC} (low) time	t_{PD}		1			ms
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} (Reset)	V_{CC_RST}		0		0.3	V

Table 5: Device Initialization Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		250	-	-	µs
V_{CC} Cutoff – Must Initialize Device	$V_{CC\text{-}CUTOFF}$		1.6	-	-	V

Electrical Specifications

Table 6: Recommended Operating Conditions

Parameter / Condition	Minimum	Typical	Maximum	Units
Operating Temperature (T_A)	-40.0	-	125.0	°C
V_{CC} Supply Voltage	2.7	3.0	3.6	V
V_{CCIO} Supply Voltage	1.71	1.8 - 3.0	3.6	V
V_{SS} Supply Voltage	0.0	0.0	0.0	V
V_{SSIO} Supply Voltage	0.0	0.0	0.0	V
Vwi Write Inhibit Voltage	2.1	2.3	2.5	V

Table 7: Pin Capacitance

Parameter	Symbol	Test Conditions	Density	Maximum	Units
Input Pin Capacitance	C_{IN}	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	1Gb	10.0	pF
			4Gb	20.0	
Input / Output Pin Capacitance	C_{INOUT}	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	1Gb	10.0	pF
			4Gb	20.0	

Table 8: DC Characteristics

Parameter	Symbol	Test Conditions	Density	3.0V Device (2.7V-3.6V)				
				Min	Typical[1]	85°C	Max[1]	Units
Read Current	I_{READ}	V_{CC} (max), I_{OUT}=0mA	1Gb		25	50	80	mA
			4Gb		70	200	300	
Write Current	I_{WRITE}	V_{CC} (max)	1Gb		20	50	80	
			4Gb		65	200	300	
Standby Current (-40°C to 125°C)	I_{SB}	E#=V_{IH}, V_{CC} (max)	1Gb		25	50	75	
			4Gb		60	180	280	
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-		±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-		±1.0	µA
Input High Voltage	V_{IH}			0.8xV_{CC}	-		V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.5	-		0.2xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -1.6mA		V_{CC}-0.5	-		-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1.6mA		-	-		0.4	V

1. Typical measured at 25°C Max measured at 125°C

Table 9: Magnetic Immunity Characteristics

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	H_{max_write}	24000	A/m
Magnetic Field During Read	H_{max_read}	24000	A/m

Table 10: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	5ns
Input and output measurement timing levels	V_{CC}/2
Output Load	CL = 30pF

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 11: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Temperature Under Bias	-45	130	°C
Storage Temperature	-55 to 150		°C
Supply Voltage Vcc relative to Vss	-0.5	4.0	V
Voltage on any pin except V_{DD}	-0.5	Vcc + 0.4	V
Voltage on V_{DD}	1.8		V
DC output current Iout	± 20		mA
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test) JESD78	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Write Operation

Figure 7: Write Operation

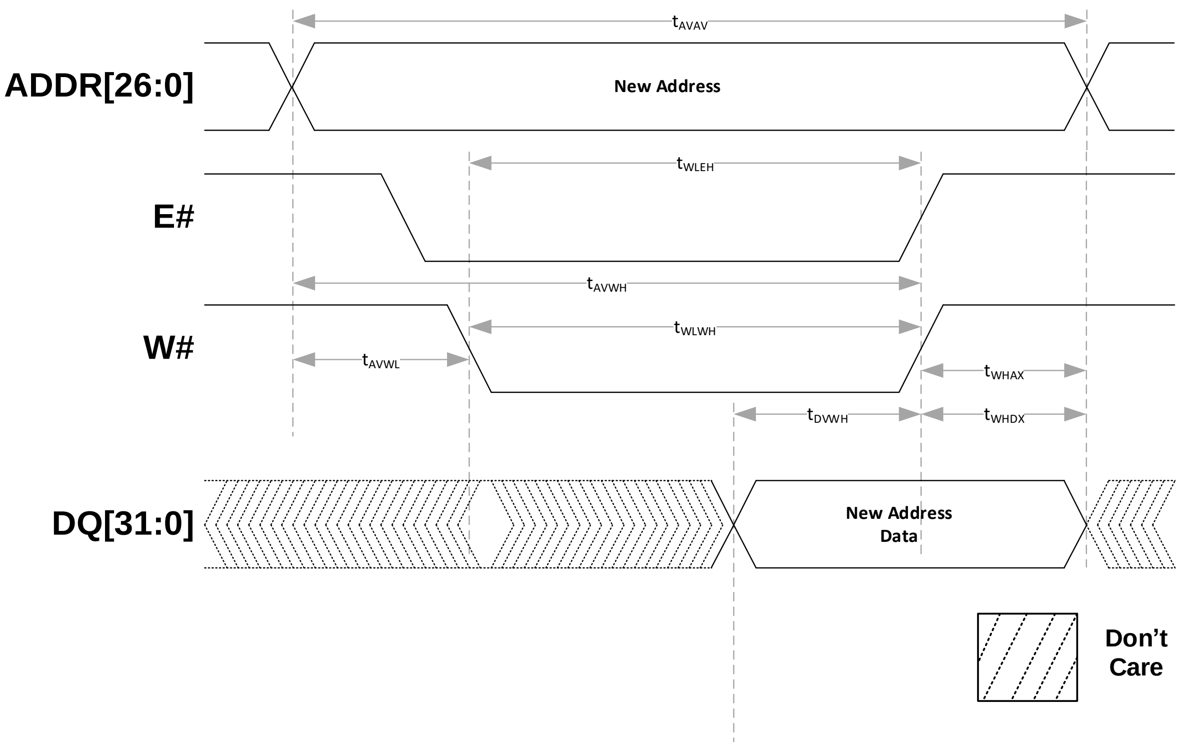


Table 12: Write Operation (W# Controlled)

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{AVAV}	45	-	ns
Address Set-Up Time	t_{AVWL}	0	-	ns
Address Valid to end of Write (G# High)	t_{AVWH}	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVWH}	30	-	ns
Write Pulse Width (G# High)	t_{WLWH}, t_{WLEH}	25	-	ns
Write Pulse Width (G# Low)	t_{WLWH}, t_{WLEH}	25	-	ns
Data Valid to end of Write	t_{DVWH}	15	-	ns
Data Hold Time	t_{WHDX}	0	-	ns
Write recovery Time	t_{WHAX}	12	-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

Figure 8: Write Operation (E# Controlled)

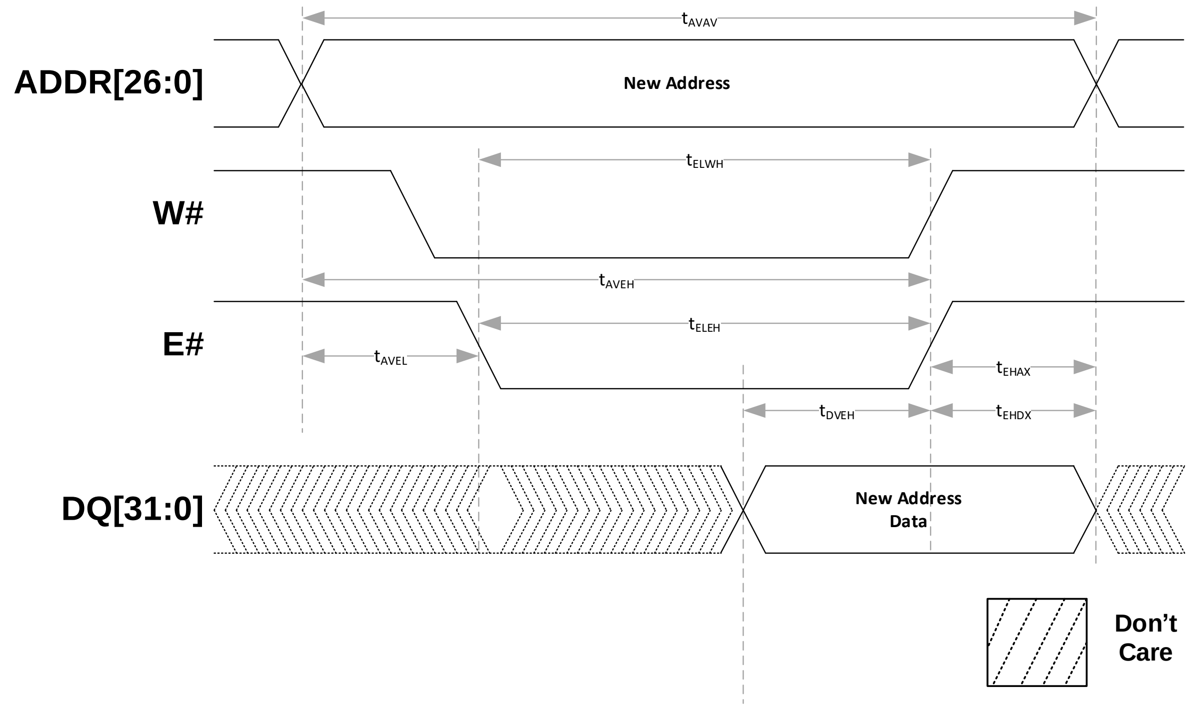


Table 13: Write Operation (E# Controlled)

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{AVAV}	45	-	ns
Address Set-Up Time	t_{AVEL}	0	-	ns
Address Valid to end of Write (G# High)	t_{AVEH}	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVEH}	30	-	ns
Write Pulse Width (G# High)	t_{ELWH}, t_{ELEH}	25	-	ns
Write Pulse Width (G# Low)	t_{ELWH}, t_{ELEH}	25	-	ns
Data Valid to end of Write	t_{DVEH}	15	-	ns
Data Hold Time	t_{EHDX}	0	-	ns
Write recovery Time	t_{EHAX}	12	-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as W# goes low

Bus Turnaround Operation – Read to Write

Figure 9: Bus Turnaround Operation

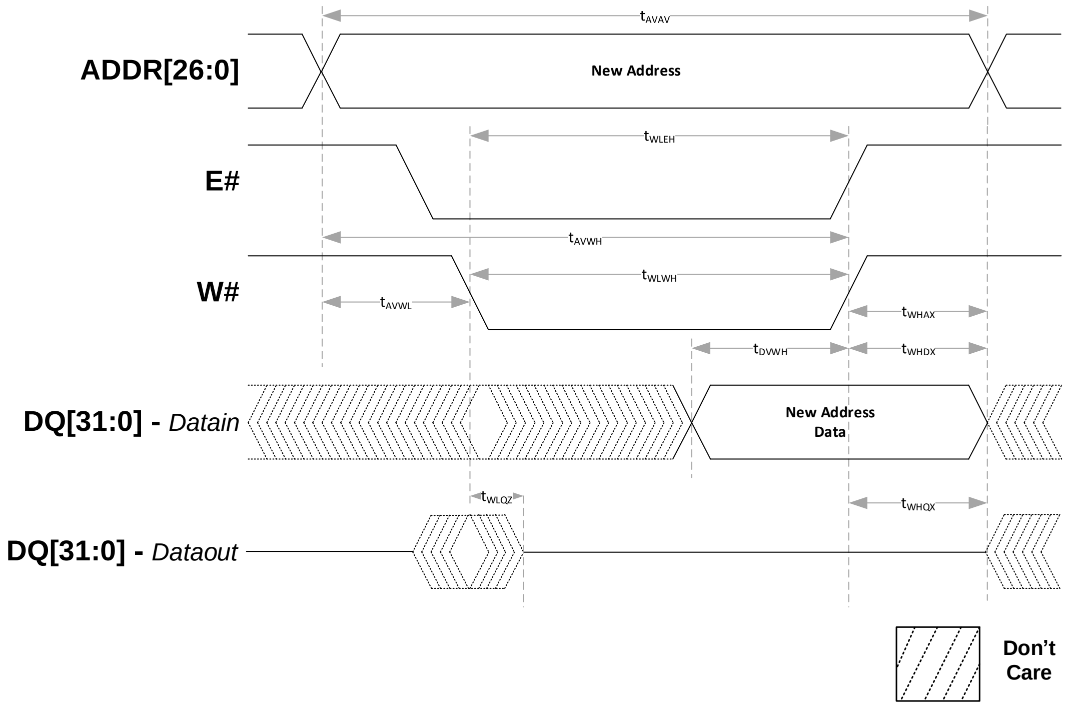


Table 14: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
W# Low to Data Hi-Z	t_{WLQZ}	0	15	ns
W# High to Output Active	t_{WHQX}	3	-	ns

Notes:
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

Read Operation

Figure 10: Read Operation

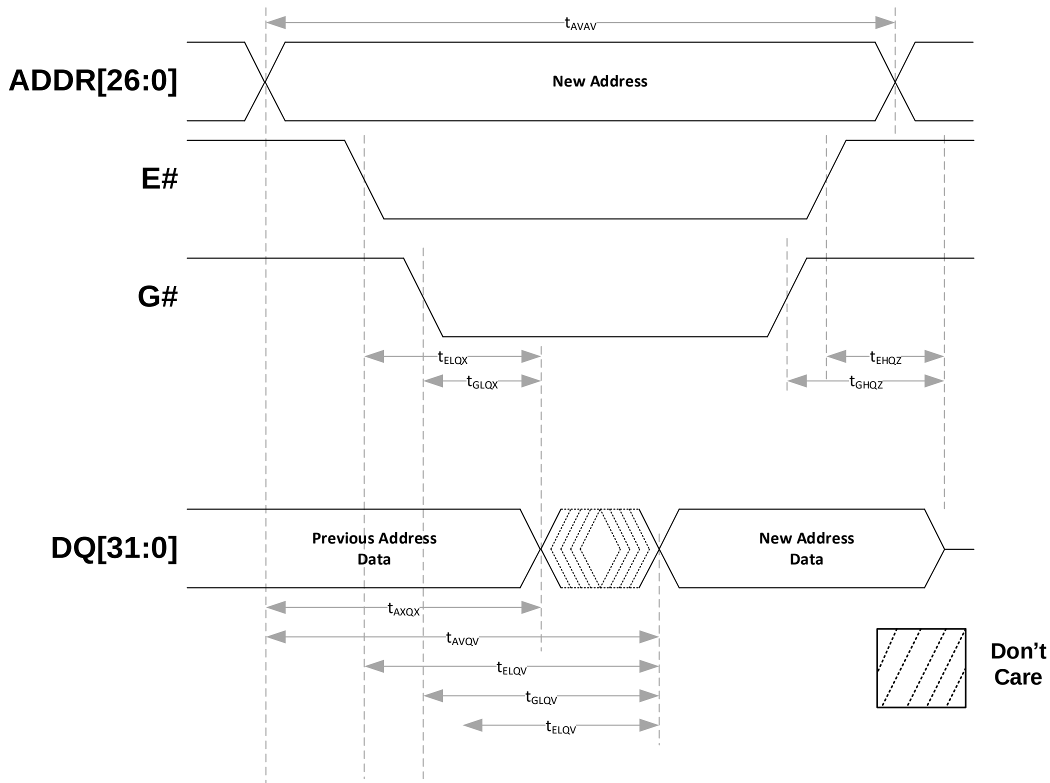


Table 15: Read Operation

Parameter	Symbol	Minimum	Maximum	Units
Read Cycle Time	t_{AVAV}	45	-	ns
Address Cycle Time	t_{AVQV}	-	45	ns
Chip Enable Access Time	t_{ELQV}	-	45	ns
Output Enable Access Time	t_{GLQV}	-	25	ns
Output Hold From Address Change	t_{AXQX}	3	-	ns
Chip Enable Low to Output Active	t_{ELQX}	3	-	ns
Output Enable Low to Output Active	t_{GLQX}	0	-	ns
Chip Enable High to Output Hi-Z	t_{EHQZ}	0	15	ns
Output Enable High to Output Hi-Z	t_{GHQZ}	0	15	ns

Notes:
W# is High (Logic '1') for Read operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

Endurance and Data Retention

Table 16: Endurance and Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	125°C	10	years
		105°C	10	
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

Thermal Resistance

Table 17: Thermal Resistance Specifications

Parameter	Description	Test Conditions	142 Ball FBGA (1Gb)	142 Ball FBGA (4Gb)	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	17.89	17.90	ºC/W
θ_{JC}	Thermal resistance (junction to case)		2.10	2.19	

Notes:
1: These parameters are guaranteed by characterization; not tested in production.
2: Ambient temperature, T_A 25 ℃
3: Worst case Junction temp specified for Top die (θ_{JA}) and Bottom die (θ_{JC})

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Revision History

Revision	Date	Change Summary
REV A	11/19/2019	Preliminary release
REV B	12/19/19	Removed commercial grade Added x32 configuration Removed 54-pin TSOP Added 92-ball FBGA Updated DC characteristics and pin capacitance Updated part number options
REV C	02/19/2020	Added 125 degrees option Updated 92-ball package
REV D	10/8/2020	Removed 256Mb density and added 2Gb density Removed Industrial, Industrial Extended temp grade options, added military temp grade option Removed 35ns performance option Updated 92-FBGA dimensions Added radiation specs Updated OPN decoder and valid combinations Updated Electrical Specifications, write operation specifications and read operation specifications. Added Endurance and Retention specs
REV E	10/23/2020	Removed radiation specs
REV F	3/15/2021	Added 4Gb device option Changed 92-ball BGA to 142-ball BGA; updated package ball assignments and outline drawing Added Asynchronous Page Mode Removed Industrial and Industrial Plus temp grades Removed sleep mode
REV G	5/27/2021	Updated BGA Pin assignments
REV H	6/15/2021	Corrected INT# pin assignment and updated package drawings
REV I	6/15/2021	Remove restrictions of use in Military applications Changed temp spec to -40. Plastic parts will only be qualified to -40 degrees Centigrade.
REV J	6/21/2021	Updated Package Ball assignment to conform to JEDED standard
REV K	8/23/2021	Updated Page mode timing : Tpwc in table 15. Corrected Isb in summary table Added Pin descriptions for E# and PG#. Updated timing diagrams (Figures 15, 16 & 17) to show E# instead of CE#; W# instead of WE# and G# instead of OE#. Removed Byte enable from Table 14
REV L	9/3/2021	Updated package dimension to show Ball diameter Removed redundant notes describing dimensions on package dimension page. Fixed I/O Power legend to show VCCQ
REV M	9/29/2021	Removed 512Mb and 2Gb densities Removed Tape & Reel as an ordering option Added Vccio to the specification
REV N	10/20/2021	Added 64 and 256Mb densities Added Hardware RST# pin Temp spec in Part number corrected to show 0M
REV O	12/09/2021	Added V_{DD} and V_{BYP} pin description and PowerUp/Powerdown sequence
REV S	12/20/2021	Updated Table 5 with Vcc Ramp time

REV T	01/18/2022	Removed 64 and 256Mb densities from this data sheet
REV U	03/31/2022 04/29/2022 05/16/2022 05/23/2022 05/25/2022	Renamed VCCQ to VCCIO Added pin assignment table Relaxed Vdd spec to +-7.5% from +-5% Added ball assignment of ADDR[17:12] to signal description table Added package thermal Updated Pictures with new Figure # Updated DC Characteristics Table: Current numbers are based on UMC's analysis of their current 22nm process. Added V_{DD} to supply line on Front page Updated Power sequencing description under DEVICE INITIALIZATION Added Absolute Maximum Ratings Table Called out specific voltages are allowed for V_{CCIO} on front page. Removed Power sequencing case of VDD going low before VCC Added Absolute Maximum rating on V_{DD}
REV V	07/01/2022	Changed the nominal height to be compatible with Gen 3 Serial devices: Nominal Thickness in Figure 5 changed from 1.39 to 1.43. Leaded ball options added to Order Option Table
REV W	07/19/2022	Removed Performance table Added Extended Safe Operating Area as well as Normal Operating Conditions Removed redundant Package drawing table Fixed wording on use of V_{BYP} in pin definition table
REV X	12/15/2022	Ball K3 (previously designated as #PG) is re-assigned as Reserved and must be pulled high to Vccio through a 10kΩ resistor (This is the fast page function. For compatibility with SRAM devices, this function is now reserved and only available for custom designs). This device is now available for use in LEO. The Extended Safe Operating Area (ESOA) is no longer described here and is only available through our partner program: As such Ball K12 (previously external Vdd) is now NC and H13 (previously V_{BYP}) has to be connected to Vss. Added 85℃ power consumption to DC Characteristics Table