

Space Grade Parallel Persistent SRAM Memory

(AS301GB32, AS302GB32, AS304GB32, AS308GB32)

Features

- Interface
 - Parallel Asynchronous x32
- Technology
 - pMTJ STT-MRAM
 - Virtually unlimited Endurance and Data Retention (see Table 17)
- Density
 - 1Gb, 2Gb, 4Gb, 8Gb
- Memory Array Organization
 - 1 Gb : 33,554,432 x 32
 - 2 Gb : 67,108,864 x 32
 - 4 Gb : 134,217,728 x 32
 - 8 Gb : 268,435,456 x 32
- Radiation Exposure Limits *:
 - ≤ 75K RAD TID,
 - LET ≤ 37 MeV cm2/mg

- Voltage Range
 - Operating V_{cc}: 2.50V 3.60V
 - Vccio: 1.8V, 2.5V, 3.3V
 - Under Radiation: V_{CC}: 2.50V 3.00V *
 - Vccio: 1.8V, 2.5V, 3.3V *
- Temperature Range
 Operating -40°C to 125°C
 - Operating under radiation -40°C to 85°C *
- Packages
 - 142-ball FBGA (15mm x 17mm)
- Qualification
 - JESD47H.01,
 - 48 Hr Burn in
- RoHS & REACH Compliant **

* To assure a Safe Operating Area, limit the device to these specifications.

** Leaded Balls available



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General Description

AS3xxx332 is a Spin-transfer torque Magneto-resistive random-access memory (STT-MRAM). It is offered in 1Gbit and 4Gbit. MRAM technology is analogous to Flash technology with SRAM compatible 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution. Data is always non-volatile with 10¹⁶ write cycles endurance and greater than 20-year retention @85°C.

Table	1:	Technology	Comparison
-------	----	------------	------------

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	-	\checkmark	\checkmark	\checkmark
Write Performance	\checkmark	-	-	\checkmark
Read Performance	\checkmark	_	_	\checkmark
Endurance	\checkmark	_	_	\checkmark
Power	_	_	_	\checkmark

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, high endurance, high performance and scalable memory technology.

AS3xxx332 is available in small footprint (15mm x 17mm) 142 ball BGA package. In 1,2,4Gb densities the device uses one chip select E#. In this configuration one contigious address space of 1,2,4Gb is formed. In 8Gb configuration the package has two banks of 4 dies each selctable separately and not at the same time. Each bank is selectable using either E1# and E2#. In the 8Gb configuration E1# and E2# MUST NOT be selected simultaneously as the two banks share the same I/O pins.

AS3xxx332 is offered with industrial extended (-40°C to 125°C) operating temperature ranges: This is measured as the junction temperature.



Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Part Number Ordering Options





Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations – 45ns							
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number			
AS301GB32-045nX	OM	BD	Y	AS301GB32-045nX0MBDY			
AS302GB32-045nX	OM	BD	Y	AS302GB32-045nX0MBDY			
AS304GB32-045nX	OM	BD	Y	AS304GB32-045nX0MBDY			
AS308GB32-045nX	OM	BD	Y	AS308GB32-045nX0MBDY			
AS301GB32-045nX	OM	BE	Y	AS301GB32-045nX0MBEY			
AS302GB32-045nX	OM	BE	Y	AS302GB32-045nX0MBEY			
AS304GB32-045nX	OM	BE	Y	AS304GB32-045nX0MBEY			
AS308GB32-045nX	OM	BE	Y	AS308GB32-045nX0MBEY			

Table 2: Valid Combinations List

Marking Specification — Standard

The device will be marked according to the following specification:

Line #1 & Line #2 will match the part number in Table 2

Line #3 Will show: 5 digit Alphanumeric Code + Country of Origin + Date Code

Line #4 May or May not be marked. This field is reserved for Avalanche Technology

Line #5 May or May not be marked. This field is reserved for Avalanche Technology

Figure 2: Device Marking

XX	хх-уууу	 Line #5
		LOGO
AS304GB32-	ļ	Line #1
045nX0MBDY	+	Line #2
KM0YG KR 2337	+	Line #3
	bbbbbb	 Line #4

Signal Description and Assignment



Figure 3: Device Pinout

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Table 3: Signal Description

Signal	Ball Assignment	Туре	Description			
E#/E1#	P8	Input	 1,2,4Gb (E#) : Chip enable: Enables the MRAM array 8Gb (E1#) : Chip enable: Enables the 1st bank of 4 MRAM die. There is an internal 10k Pullup. THIS SIGNAL MUST NOT BE ACTIVE AT THE SAME TIME AS E2#. 			
DNU / E2#	К5	DNU/Input	1,2,4Gb (DNU) : It can be left floating and not connected. 8Gb (E2#) : Chip enable: Enables the second bank of 4 MRAM die. THIS SIGNAL MUST NOT BE ACTIVE AT THE SAME TIME AS E1#.			
G#	P7	Input	Output enable: Enables the output drivers for data transfer I/Os.			
CR#	J2	Input	Configuration Register enable: Enables access to the Configuration registers			
PG#	K3	Input	Page Mode: Enables Page mode access			
W#	M8	Input	Write enable: Transfers data from the host system to the MRAM when Low (Logic '0').Transfers data from the MRAM to the host system when High (Logic '1').			
ADDR[26:0]	M2, L4, K13, M3, L3, M7, P12, L12, N11, N6, P6, L13, M13, P10, N10, M12, N13, L11, M11, P5, P3, N5, N4, M4, N2, N9, M9	Input	Address: I/Os for address transfer1G:ADDR[24:0] – 25 Address pins for 1Gbx32 devices.*2G:ADDR[25:0] – 26 Address pins for 2Gbx32 devices.**4G:ADDR[26:0] – 27 Address pins for 4Gbx32 devices.			
DQ[31:0]	E2, F2, D2, E3, E12, D10, C9, C7, G4, G3, F13, D13, C10, E8, F6, E5, E13, G11, E10, F9, C8, C6, D6, D4, G12, C12, D11, D9, E7, C5, D5, C3	Input / Output	Data inputs/outputs: The bidirectional I/Os transfer data [31:0].			
INT# ***	G13	Output	Interrupt: Output generated by the MRAM when an unrecoverable ECC error is detected during read operation (output goes low on error): requires to have an external pull-up resistor $(4.7K\Omega)$			
Vссю	F12, J12, E11, M10, D8, N8, D7, N7, M5, E4, F3, J3	Supply	I/O power supply.			
Vssio	F10, L10, E9, L9, F8, L8, F7, L7, E6, L6, G5,	Supply	I/O ground supply.			
Vcc	C13, P13, D12, N12, C11, F11, H11, J11, K11, P11, C4, F4, H4,	Supply	Core power supply.			



Signal	Ball Assignment	Туре	Description
	J4, K4, P4, D3, N3, C2, P2		
Vss	A14, B14, C14, H13, R14, T14, A13, T13, A12, G10, H10, J10, K10, F5, L5, A2, T2, A1, B1, R1, T1	Supply	Core ground supply.
DNU	J13, H12, K12, P9, M6, H5, J5, H3, G2, H2, K2, L2		Do Not Use: DNUs must be left unconnected.

* Unused ADDR[26:25] balls should be connected to Ground

** Unused ADDR[26] balls should be connected to Ground

*** INT# is latched and must be reset/cleared by writing to the ECC Control register.

Special Configuration Options

There are eight user accessible registers that control ECC, output drive strength and array write protection. All registers are 32-bit wide. These registers are only available during device configuration and not accessible to the user. In a multi-die configuration (2Gb, 4Gb) each 1Gb die has its own set of registers and need to be programmed individually. Each die needs to be selected using the upper 2 MSB address bits.

ECC Registers

There are 6 registers that allow access to the ECC engine during the life of the product to access the functionality of the circuits. During normal use, the ECC engine will correct any soft errors.

INT# functionality

As explained in the pinout, the INT# will go active if uncorrectable error is encountered. This is an open collector output which requires a pullup. In a multi-chip configuration (2G, 4G) the pin is shared between the dies. The recommended next steps are up to the system architect. The host must interrogate each die to identify which one/ones caused the interrupt to clear the INT Flag register.

		•			
Bits	Name	Description	Read / Write	Default State	Select Options
[31:2]	RSVD	Reserved	R	31'b0	Reserved for future use
[1]	Interrupt Reset	Resets the interrupt generated in response to detection of an unrecoverable error and clears the interrupt flag.	W		0: Don't reset 1: Reset ECC unrecoverable error interrupt
[0]	Error_Count_Reset	Resets the ECC Error Count Register	W	0	0: Don't reset 1: Reset ECC Error Count Register to zero

ECC Control Register – Read and Write

Output Drive Strength Register

The default setting of this register is 00.

Output Drive	Strenath	Reaister –	Read	and Write
	••••g•••			

Bits	Name	Description	Read / Write	Default State	Selec	ct Optior	าร	
[31:3]	RSVD	Reserved	R	0	Rese	rved for	future us	se
[2]	Enable_ Drive_Strength	Enables or disables the drive strength setting	R/W	0	0: De 1: Us settin	fault se e outpu g	tting t drive str	ength
						1.8V	2.5V	3.3V
[1:0]	Output_Drive_	Output drive	R/W	00	00	1mA	2.5mA	4mA
	Strength_Setting	strength			01	3mA	5mA	8mA
					10	5mA	10mA	14mA
					11	7mA	14mA	18mA

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Device Protection Register

It is possible to write protect the Memory array as shown in the table below. Note; The term full array is defined as an array of 1Gb.

			-		
Bits	Name	Description	Read /	Default	Select Options
			Write	State	
[31:3]	RSVD	Reserved	R	29'b0	Reserved for future use
[2:0]	BPSEL[2:0]	Enables or	R/W	3'b0	000 – Disabled
		disables block			001 – Protect upper 1/64 array
		protection			010 – Protect upper 1/32 array
					011 – Protect upper 1/16 array
					100 – Protect upper 1/8 array
					101 – Protect upper 1/4 array
					110 – Protect upper 1/2 array
					111 – Protect full arrav

Device Protection Register – Read and Write



Package Options

142-Ball FBGA – 1,2,4Gb AS301GB32, AS302GB32, AS304GB32 (Bottom View)



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avalanche technology 1 Gb x32, 2 Gb x32, 4Gb x32, 8Gb x32: MRAM Memory 142-Ball FBGA – 8Gb AS308GB32 (Bottom View) 14 13 12 11 10 9 8 7 6 5 4 3 2 1 Α VSS VSS VSS VSS VSS в VSS VSS (DQ 25) $\begin{pmatrix} DQ\\ 11 \end{pmatrix}$ $\begin{pmatrix} DQ \\ 24 \end{pmatrix}$ $\begin{pmatrix} DQ\\ 10 \end{pmatrix}$ $\begin{pmatrix} DQ \\ 2 \end{pmatrix}$ $\begin{pmatrix} DQ \\ 0 \end{pmatrix}$ DQ 6 DQ 19 vcc С VSS vcc vcc) vcc D DQ 20 DQ 5 DQ 4 DQ 9 DQ 1 DQ 8 DQ 29 DQ 26 VCCIO vcc VCC DQ 3 DQ 28 DQ 31 DQ 27 DQ 13 DQ 18 DQ 16 DQ 15 Е CCIO SSIO SSI0 VCCIO DQ 12 DQ 17 F CCIO vcc SSIC SSIC SSIO VSS vcc VCCIO DQ 30 DQ 7 DQ 14 vss DQ DQ 23 (DNU) G /SSI (DNU) (DNU) (DNU) н VSS VCC VSS DNU vcc J CR# /CCIO VCCIO DNU DNU vcc vcc (DNU) (DNU) A 24 vss PG# κ vcc E2# vcc A 19 L A 9 A 25 A 22 (DNU) A 15 SSIC SSIC SSIO /SSIC vss SSIC A 23 Μ $\left(\begin{array}{c} A\\11\end{array}\right)$ A 8 A 0 W# (A 21) A) A 26 A 14 CCIO VCCIO DNU) Ν (A) A 1 A) (A 18) A) A) vcc VCCIO vccio A 2 A 10 1 vcc Ρ A 7 $\left(\begin{array}{c} A\\ 6\end{array}\right)$ A 20) A 13 vcc vcc (DNU) E1# G# A) vcc vcc R VSS vss т VSS VSS

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Figure 4: 142-ball FBGA

142-Ball FBGA Mechanical Drawing

Figure 5: 142-ball FBGA Mechanical Drawing - 1,2,4 Gb



[NOTES] 1. SOLDER BALL SIZE IS

0.35 mm before reflow

0.37 (+/-0.05) mm post reflow

2. SOLDER RESIST OPENING IS

0.300 mm

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Figure 6: 142-ball FBGA Mechanical Drawing - 8 Gb



[NOTES]

1. SOLDER BALL SIZE IS

0.35 mm before reflow

0.37 (+/-0.05) mm post reflow

2. SOLDER RESIST OPENING IS

0.300 mm

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Architecture

AS3xxx332 is a high performance MRAM device. Writing to and reading from the device are performed as follows:

To write to the device, drive Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[31]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[26]).

To read from the device, drive Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[26]) to appear on I/O pins (DQ[0] to DQ[31]).

In the case of the 8Gb device: This architecture is duplicated. Each bank of 4 dies is controlled with a separate chipselect: E1#, E2#.



Figure 7: Functional Block Diagram

Table 4: Modes of Operation

Mode	E#	G#	W#	Current	DQ[31:0]
Not Selected	Н	Х	Х	Isb	Hi-Z
Output Disabled	L	Н	Н	IREAD	Hi-Z
Read Word	L	L	Н	IREAD	Data-out
Write Word	L	Х	L	IWRITE	Data-in

Notes:

H: High (Logic '1') L: Low (Logic '0')

X: Don't Care Hi-Z: High Impedance



Normal Device Initialization:

When powering up, the following procedure is required to initialize the device correctly:

- V_{CC} and V_{CCIO} can ramp up together (R_{VR}), if not possible then V_{CC} first followed by V_{CCIO}. The maximum difference between the two voltages should not exceed 0.7V before reaching the final value of V_{CCIO}.
- The device must not be selected at power-up (a 10KΩ pull-up Resistor to V_{CCIO} on E# is recommended). Then a further delay of t_{PU} (Figure 8) until V_{CC} reaches V_{CC}(minimum).
- During Power-up, recovering from power loss or brownout, a delay of tPU is required before normal operation commences (Figure 6).



Figure 8: Power-Up Behavior

When powering down, the following procedure is required to turn off the device correctly:

- V_{CC} and V_{CCIO} can ramp down together (R_{VF}), if not possible then V_{CC} first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-down (a 10KΩ pull-up Resistor to V_{CCIO} on E# is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, when V_{CC} goes below V_{CC-CUTOFF}. The voltage must drop below V_{CC}(Reset) for a period of tPD. The power-up timing needs to be observed after V_{CC} goes above V_{CC}(minimum)



Figure 9: Power-Down Behavior

Table 4: Power U	p/Down & Device	Initialization	Timing and	Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
Vcc Range			2.45	-	3.6	V
V _{cc} Ramp Up Time	R _{VR}		30	-	-	µs/V
Vcc Ramp Down Time	Rvf	All operating voltages	20	-	-	µs/V
Vcc Power Up to First Instruction	tPU	and temperatures	1	-	-	ms
V _{cc} (low) time	t _{PD}		1			ms
Vcc Cutoff – Must Initialize Device	Vcc_cutoff		1.6	-	-	V
V _{cc} (Reset)	Vcc_rst		0		0.3	V



Electrical Specifications

	Parameter / Condition	Minimum	Typical	Maximum	Units
	Operating Temperature (T _A)	-40.0	-	125.0	°C
Normal Operation	Vcc Supply Voltage	2.45	3.0	3.6	V
oporation	V _{CCIO} Supply Voltage		1.8 – 2.5 – 3.3		V
	Operating Temperature (T _A)	-40.0	-	85.0	°C
Under Radiation	Vcc Supply Voltage	2.45	2.5 - 3.0	3.05	V
Naciation	Vccio Supply Voltage		1.8 – 2.5 – 3.3		V
	Vss Supply Voltage	0.0	0.0	0.0	V
	V _{SSIO} Supply Voltage	0.0	0.0	0.0	V
V	wi Write Inhibit Voltage	2.0	2.2	2.4	V

Table 6: Pin Capacitance

Parameter	Symbol	Test Conditions	Density	Maximum	Units
			1Gb	10.0	
Input Pin Capacitance	CIN	TEMP = 25°C; f = 1 MHz; V _{IN} = 0V	2/4Gb	20.0	
			8Gb	40.0	
			1Gb	10.0	pF
Input / Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V _{IN} = 0V	2/4Gb	20.0		
			8Gb	40.0	

Table 7: DC Characteristics

Parameter	Symbol	al Toot Conditions	Donoity	3.0V Device (2.5V-3.6V)				
Falailletei	Symbol	Test conditions	Density	Min	Typical ¹	85℃ ²	Max ³	Units
			1Gb		25	50	80	
Read Current	Iread	V _{CC} (max), I _{OUT} =0mA	2Gb		50	100	150	
			4Gb		70	200	300	
			8Gb		140	400	600	

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Parameter	Parameter Symbol Test Conditions Densit		Donaity	3.0)V Device (2.	.5V-3.6V)		
	Symbol	Test Conditions	Density	Min	Typical ¹	85°C ²	Max ³	Units	
			1Gb		20	50	80		
Write Current	hupter		2Gb		50	100	150		
while Guirent	IWRITE		4Gb		65	200	300		
			8Gb		130	400	600		
			1Gb		25	50	75		
Standby Current		Е#=Vін,	2Gb		45	100	140		
(-40°C to 125°C)	ISB	V _{CC} (max)	4Gb		60	180	280		
			8Gb		120	360	560		
Input Leakage Current	١Lı	V _{IN} =0 to V _{CC} (max)		-	-		±1.0	μA	
Output Leakage Current	ILO	V _{OUT} =0 to V _{CC} (max)		-	-		±1.0	μA	
Input High Voltage (Vccio=1.71-2.2)				0.65* V _{CCIO} -		Vecio			
Input High Voltage (Vccio=2.2-2.7)	Vih	Vih			1.8			+0.2	V
Input High Voltage (V _{CCI0} =2.7-3.6)				2.2					
Input Low Voltage (Vccio=1.71-2.2)					-		0.35* V _{CCIO}		
Input Low Voltage (Vccio=2.2-2.7)	VIL			-0.2			0.7	V	
Input Low Voltage (V _{CCI0} =2.7-3.6)							0.8		
Output Low Voltage (Vccio=1.71-2.2)		I _{OL} = 0.1mA					0.2		
Output Low Voltage (Vccio=2.2-2.7)	Vol	I _{OL} = 0.1mA		-			0.4	V	
Output Low Voltage (V _{CCI0} =2.7-3.6)		$I_{OL} = 2.0 \text{mA}$					0.4		
Output High Voltage (Vccio=1.71-2.2)		loн = -0.1mA		1.4					
Output High Voltage (Vccio=2.2-2.7)	Vон	loн = -0.1mA		2.0			-	V	
Output High Voltage (V _{CCI0} =2.7-3.6)		I _{OH} = -1.0mA		2.4					

¹ Typical values are measured at 25°C Notes:

² 85°C values are guaranteed by characterization; not tested in production

³ Max values are measured at 125°C

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	H _{max_write}	24000	A/m
Magnetic Field During Read	H _{max_read}	24000	A/m

Table 8: Magnetic Immunity Characteristics

Table 9: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to Vcc
Input rise and fall times	5ns
Input and output measurement timing levels	Vcc/2
Output Load	CL = 30pF

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Parameter	Minimum	Maximum	Units
Magnetic Field During Write		24000	A/m
Magnetic Field During Read		24000	A/m
Junction temperature		150	°C
Storage Temperature	-55 to	150	°C
Supply Voltage Vcc	-0.5	4.0	V
I/O Voltage Vccio	-0.5	3.8	V
Voltage on any pin except Vcc	-0.5	Vccio + 0.2	V
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ 200	00 V	V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ 50	0 V	V
Latch-Up (I-test) JESD78	≥ 100) mA	mA
Latch-Up (Vsupply over-voltage test) JESD78	Pas	sed	

Table 10: Absolute Maximum Ratings



Write Operation





Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t _{AVAV}	45	-	ns
Address Set-Up Time	t _{AVWL}	0	-	ns
Address Valid to end of Write (G# High)	t _{avwh}	28	-	ns
Address Valid to end of Write (G# Low)	t _{avwh}	30	-	ns
Write Pulse Width (G# High)	twlwh, twleh	25	-	ns
Write Pulse Width (G# Low)	twlwh, twleh	25	-	ns
Data Valid to end of Write	t _{DVWH}	15	-	ns
Data Hold Time	twhdx	0	-	ns
Write recovery Time	t WHAX	12	-	ns

Notes:

G# is High (Logic '1') for Write operation Power supplies must be stable Addresses valid either before or at the same time as E# goes low

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Table 12	: Write	Operation	(E# Controlled)
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Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t _{AVAV}	45	-	ns
Address Set-Up Time	t _{AVEL}	0	-	ns
Address Valid to end of Write (G# High)	t _{AVEH}	28	-	ns
Address Valid to end of Write (G# Low)	t _{AVEH}	30	-	ns
Write Pulse Width (G# High)	t _{ELWH} , t _{ELEH}	25	-	ns
Write Pulse Width (G# Low)	t _{ELWH} , t _{ELEH}	25	-	ns
Data Valid to end of Write	t _{DVEH}	15	-	ns
Data Hold Time	t _{EHDX}	0	-	ns
Write recovery Time	t _{EHAX}	12	-	ns

Notes:

G# is High (Logic '1') for Write operation

Power supplies must be stable

Addresses valid either before or at the same time as W# goes low

In case of the 8G device: E# is represented by E1# or E2#

Bus Turnaround Operation – Read to Write



Figure 12: Bus Turnaround Operation

Table 13: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
W# Low to Data Hi-Z	twlqz	0	15	ns
W# High to Output Active	twнqx	3	-	ns

Notes:

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low In case of the 8G device: E# is represented by E1# or E2#



Read Operation



Figure 13: Read Operation

	Table	14: Read	Operation
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Parameter	Symbol	Minimum	Maximum	Units
Read Cycle Time	t _{AVAV}	45	-	ns
Address Cycle Time	t _{AVQV}	-	45	ns
Chip Enable Access Time	t _{ELQV}	-	45	ns
Output Enable Access Time	t GLQV	-	25	ns
Output Hold From Address Change	t _{AXQX}	3	-	ns
Chip Enable Low to Output Active	t _{ELQX}	3	-	ns
Output Enable Low to Output Active	t GLQX	0	-	ns
Chip Enable High to Output Hi-Z	t _{EHQZ}	0	15	ns
Output Enable High to Output Hi-Z	tgнqz	0	15	ns

Notes:

W# is High (Logic '1') for Read operation

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

In case of the 8G device: E# is represented by E1# or E2#

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Asynchronous Page Mode

Asynchronous page mode is an extension of the legacy asynchronous read and write operations that improves the performance of the MRAM memory, as shown in Figure 11. On power up or reset, the MRAM memory defaults to legacy asynchronous mode to enable controllers to immediately access the memory. Page mode is also immediately available after asserting PG# low and E# high. No special commands or setup are necessary.

Figure 14: 4-Word Asynchronous Page Mode Comparison with Legacy Asynchronous Mode

Figure 12 shows the page mode functional block diagram. During a page write, a new page is accessed by changing any of the upper addresses A[max:2]. A subsequent write commands (W# toggle) can load the data buffers with new data to be written to any of the adjacent addresses A[1:0]. During page read, an initial asynchronous read access if executed during which 4 data words are read from the memory array simultaneously, and loaded into an internal page buffer, while the first data word is output onto the memory bus. Subsequent reads are output from the data buffer, providing up to two times the read and write access speed of conventional asynchronous reads.

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Asynchronous Page Mode Read Operation

Asynchronous page mode reads are initiated by the memory controller in the same way as asynchronous single-word reads by asserting E# or changing any of the upper addresses A[max:2]. In Figure 13; an address is placed on the address bus, and E# and G# are asserted. Multiple data words are "sensed" simultaneously, and loaded into an internal page buffer while the first data word is being output onto the data bus. After the initial-access delay (t_{AA}), read data is driven onto the data bus and then sampled by the memory controller. When the next read address is within the page-buffer range A[1:0], subsequent data is output from the page buffer, not from the MRAM array. A shorter access delay (t_{AAP}) occurs when data is read from the page buffer. The low-order address bits are used to access the page buffer, and determine which word is output. Four-word page access uses A[1:0];



Figure 16: Asynchronous Page Read Operation

Notes:

In case of the 8G device: E# is represented by E1# or E2#

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Asynchronous Page Mode Write Operation

For Asynchronous page mode write, shown in Figure 14, the first write pulse defines the first write access (t_{PWC}). While E# is maintained LOW, a subsequent write pulse along with a new adjacent address A[1:0] executes a page mode write access. E# must be LOW upon completion of a page write access. Asserting E# HIGH at the beginning or the middle of a page access will abort it.



Figure 17: Asynchronous Page Write Operation

Notes:

In case of the 8G device: E# is represented by E1# or E2#

Asynchronous Page Mode Write to Single Write

On power up or reset, the MRAM memory defaults to the legacy asynchronous mode. The page mode is immediately available after asserting PG# low while maintaining E# HIGH for t_{PGSL}. Returning to legacy mode can be achieved by asserting PG# HIGH and E# for t_{PGSH}.

Figure 18: Page Write to Single Write Timing Diagram

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Notes:

In case of the 8G device: E# is represented by E1# or E2#

Asynchronous Page Mode AC Timing

Parameters	Description	Min	Max	Unit
twa	Write access time	45	-	ns
twc	Chip enable LOW to write enable HIGH	30	-	ns
t _{WHAX}	Write recovery time	15	-	ns
t _{WLWH}	Write enable low time	25	-	ns
t _{AS}	Address setup time (to E# Low)	0	-	ns
t _E	Chip enable access time	-	45	ns
t _{AA}	Address access time	-	45	ns
to	Output enable access time	-	15	ns
t _{PWC}	Page mode write access	15		ns
t _{WP}	Page mode write enable low time	7.5		ns
t _{WPH}	Page mode write enable high time	7.5		ns
t _{AHP}	Page mode address hold time (to W# High)	6		ns
t _{ASP}	Page mode address setup time (to W# High)	7.5		ns
t _{AAP}	Page mode address access time	-	15	ns
t _{OHP}	Page mode output hold time	5	-	ns
t _{PGSL}	Page mode select to E# Low	10	-	ns
t _{PGSH}	Page mode unselect to E# Low	10	-	ns
t _{PGH}	Page mode high time	45	-	ns
t _{EH}	E# High time	10	-	ns
t _{OH}	Output hold time	5	-	ns
t _{EP}	Page mode E# low time	45	-	ns
t _{DSP}	Page mode data setup time (to W# High)	7.5	-	ns
t _{DHP}	Page mode data hold time (to W# High)	6	-	ns

Table 15: Page Mode AC Timing

Endurance and Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units	
Write Endurance	END	-	10 ¹⁶	cycles	
		125°C	10		
	RET	105°C	10		
Data Retention		85°C	1,000	years	
		75°C	10,000		
		65°C	1,000,000		

Table 16: Endurance and Data Retention

Thermal Resistance

Parameter	Description	Test Condition	1Gb	2Gb	4Gb	8Gb	Units
θја	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	17.89	TBD	17.90	TBD	
θις	Thermal resistance (junction to case)		2.10	TBD	2.19	TBD	-c/ W

Table 17: Thermal Resistance Specifications 142 Ball BGA

Notes:

 $1\!\!:\!$ These parameters are guaranteed by characterization; not tested in production.

2: Ambient temperature, T_A 25 °C

3: Worst case Junction temp specified for Top die ($\theta_{JA})$ and Bottom die ($\theta_{JC})$



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Revision History

Revision	Date	Change Summary
REV A	11/19/2019	Preliminary release
REV B	12/19/19	Removed commercial grade
		Added x32 configuration
		Removed 54-pin TSOP
		Added 92-ball FBGA
		Updated DC characteristics and pin capacitance
		Updated part number options
REV C	02/19/2020	Added 125 degrees option
		Updated 92-ball package
REV D	10/8/2020	Removed 256Mb density and added 2Gb density
		Removed Industrial, Industrial Extended temp grade options, added
		military temp grade option
		Removed 35ns performance option
		Updated 92-FBGA dimensions
		Added radiation specs
		Updated OPN decoder and valid combinations
		operation specifications
		Added Endurance and Retention specs
REV E	10/23/2020	Removed radiation specs
REVE	3/15/2020	Added 4Gb device option
	0/10/2021	Changed 92-ball BGA to 142-ball BGA: undated package ball assignments
		and outline drawing
		Added Asynchronous Page Mode
		Removed Industrial and Industrial Plus temp grades
		Removed sleep mode
REV G	5/27/2021	Updated BGA Pin assignments
REV H	6/15/2021	Corrected INT# pin assignment and updated package drawings
REV I	6/15/2021	Remove restrictions of use in Military applications
		Changed temp spec to -40. Plastic parts will only be qualified to -40
		degrees Centigrade.
REV J	6/21/2021	Updated Package Ball assignment to conform to JEDED standard
REV K	8/23/2021	Updated Page mode timing : Tpwc in table 15.
		Corrected Isb in summary table
		Added Pin descriptions for E# and PG#.
		Updated timing diagrams (Figures 15, 16 & 17) to show E# instead of CE#;
		W# instead of WE# and G# instead of OE#.
	0/0/0004	Removed Byte enable from Table 14
REVL	9/3/2021	Updated package dimension to show Ball diameter
		Removed redundant notes describing dimensions on package dimension
		page.
DEV M	0/20/2024	Fixed I/O Power legend to show VCCQ
	9/29/2021	Removed 512MD and 2GD densities
		Added Verio to the specification
REV N	10/20/2021	Added 64 and 256Mb densities
	10/20/2021	Added Hardware RST# nin
		Temp spec in Part number corrected to show 0M
REV O	12/09/2021	Added V_{PP} and V_{RVP} pin description and Powerl In/Powerdown sequence
REV M REV N REV O	9/29/2021 10/20/2021 12/09/2021	Fixed I/O Power legend to show VCCQ Removed 512Mb and 2Gb densities Removed Tape & Reel as an ordering option Added Vccio to the specification Added 64 and 256Mb densities Added Hardware RST# pin Temp spec in Part number corrected to show 0M Added V _{DD} and V _{BYP} pin description and PowerUp/Powerdown sequence

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REV S	12/20/2021	Updated Table 5 with Vcc Ramp time
REV T	01/18/2022	Removed 64 and 256Mb densities from this data sheet
REV U	03/31/2022	Renamed VCCQ to VCCIO
		Added pin assignment table
		Relaxed Vdd spec to +-7.5% from +-5%
0.1	04/29/2022	Added ball assignment of ADDR[17:12] to signal description table
11.2	05/16/2022	Added package thermal
0.2	05/10/2022	Updated DC Characteristics Table: Current numbers are based on LIMC's
		analysis of their current 22nm process
		Added V_{DD} to supply line on Front page
U.3	05/23/2022	Updated Power sequencing description under DEVICE INITIALIZATION
		Added Absolute Maximum Ratings Table
		Called out specific voltages are allowed for V _{CCIO} on front page.
U.4	05/25/2022	Removed Power sequencing case of VDD going low before VCC
		Added Absolute Maximum rating on VDD
REVV	07/01/2022	Changed the nominal height to be compatible with Gen 3 Serial devices:
		Nominal Inickness in Figure 4 changed from 1.39mm to 1.43mm.
	07/10/2022	Permoved Performance table
	01/19/2022	Added Extended Safe Operating Area as well as Normal Operating Conditions
		Removed redundant Package drawing table
		Fixed wording on use of V _{BYP} in pin definition table
REV X	12/15/2022	Ball K3 (previously designated as #PG) is re-assigned as Reserved and
		must be pulled high to vocio through a TUK Ω resistor (This is the fast page function. For compatibility with SPAM devices, this function is new
		reserved and only available for custom designs)
		This device is now available for use in LEO. The Extended Safe Operating
		Area (ESOA) is no longer described here and is only available through our
		partner program: As such Ball K12 (previously external Vdd) is now NC
		and H13 (previously V _{BYP}) has to be connected to Vss.
		Added 85°C power consumption to DC Characteristics Table 8.
X.1	03/28/2023	Nominal Thikcness in Figure 4 changed from 1.43mm to 1.51mm.
X.Z	04/10/2023	Added 4.7KΩ pull up to IN I#
		always been in the silicon. It is now fully tested and verified effective with
		date code: 2250 for 1Gb devices and 2240 for 4Gb devices
X.3	05/01/2023	Voltage Ramp Up rate has been clarified in the Normal Device
		Initialization.
		Input & Output Low & High Voltage levels have been redefined as
		references to V_{CCIO} rather than V_{CC} in the DC Characteristics Table 8.
X.4	05/08/2023	Page Mode write Timing was updated to match the read timing. Lead cycle
		is the same 45ns for Read and Write.
¥ 5	07/20/2023	Specified wax temp to be junction rather than amplet
X.5	07/20/2023	Added 2Gb density
	00/01/2020	Updated Input & Output Low and High Voltage levels DC Charaterstics
		table 8 to be consistent at 1.8V operation
		Clarification that PEMS-INST-001 flow version of product will be supplied
		through a partner
		Table 3: Signal desciption: Corrected definition of W# and removed RFU.
		Table 11: Corrected signal name: Changed V_{DD} to V_{CC}
		Guideline on normal device initialization corrected to say: pullup on E# is to
X.7	10/17/2023	Fixed Typo in Signal pin description Table 3 DQ[31:0]
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		Added Special Configuration Registers
		Lindated Maximum rating table 11
	12/13/2023	Updated Solder ball and Solder resist opening dimensions on the Package drawing
	01/04/2024	Updated Table 16 Page Mode AC Timing signal name/descriptions Package naming convention: Ball assignement pictures used to say: Top View. The label should have read: Bottom View.
	01/18/2024	Added Mechanical drawing for 8Gb
X.8	03/26/2024	Corrected Modes Of Operation Table "Removed Output Disabled mode with E#, G#, W# set to L, X, X".
		Removed DC output Current lout from Absolute Maximum Ratings Table: Correct Maximum Current should be taken from the DC Charcterstics table base don number of dies in the device.
		INT# definition was updated: When triggered this signal remains low and must be cleared by writing to the ECC Control register.
REV Y	03/28/2024	Added Safe Operating Area Specification: Extended the Operational
	04/05/2024	voltage to 2.5V as a minimum.
	04/00/0004	Added Marking Specification.
	04/09/2024	Corrected 8Gb Ball Map to be consistent with the 1/2/4Gb Ball Map.
	05/20/2024	Corrcted the address line that needs to be gounded for 2Gb device A[26].
REV Z	06/24/2024	Added Radiation Tolerance level to the datasheet. Please refer to te
		Radiation test report for this family to decide suitability for your mission.
	07/15/2024	Updated Power UP Behavior to allow for Vcc and Vccio mismatch