AS104MA1F2A
AS108MA1F2A

Datasheet

4Mb/8Mb QSPI

40MHz SPnvSRAM™

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Product Features

pMTJ SST-MRAM Technology

- Density: 4Mb and 8Mb

Fast Quad SPI interface

- Up to 40 MHz Clock frequency
- Single SPI, Dual SPI, Quad SPI Modes
- No Wait Writes
- Supports SPI Mode 0 and Mode 3

Low-Voltage Operation

- $V_{CC/VCCQ}$ = 1.7V to 2.0V

Data Protection

- Hardware Protect Mode (HPM):
  - Enable/Disable Protection with WP# Pin
- Software Protect Mode (SPM):
  - Write-Protect All or Portion of the Memory Array using BP2, BP1, BP0 Bits

Power Consumption

- Standby Current: 200µA (typ.), 800µA (max.)
- Operating Supply Current: 30mA (max.) at Quad I/O 40MHz

Superior Reliability

- Compared with nvSRAM, SPnvSRAM does not require backup battery or capacitor(s)
- Compared with F-RAM, SPnvSRAM has non destructive Reads
- Virtually Unlimited Endurance: 10^{14} Read/Write Cycles
- Superior Data Retention: More than 20 Years

Package

- 8-Pin WSON
- 16-Pin SOIC

Temperature Range

- Commercial: 0°C to +85°C
- Industrial: -40°C to +85°C
- Extended: -40°C to +105°C

Compliance

- RoHS

Table of Contents

Figures & Tables

1 Description

The 4Mb/8Mb QSPI 40MHz SPnvSRAM™ is a SPI Non-Volatile SRAM device utilizing advanced pMTJ STT-MRAM technology. The device offers an SPI compatible serial bus running up to 40MHz clock frequency with superior reliability and greater than 20-year data retention.

The 4Mb/8Mb QSPI 40MHz SPnvSRAM™ is an ideal memory solution for the MCU applications that require an external SRAM extension. The product offers fast throughput (Quad SPI), low power consumption, minimum pin count and small form factor, making it a suitable solution for embedded, network switches, automotive, and Internet of Things (IoT) applications.

Memory Organization:

- The 4Mb memory array is organized as 32 blocks. Each block contains 8,192 words of 16-bit. The whole memory consists of 524,288 bytes.
- The 8Mb memory array is organized as 32 blocks. Each block contains 16,384 words of 16-bit. The whole memory consists of 1,048,576 bytes.

The 4Mb/8Mb QSPI 40MHz SPnvSRAM™ is available in 8-Pin WSON and 16-Pin SOIC packages.

2 Pinouts

2.1 8-Pin WSON Pin-Out

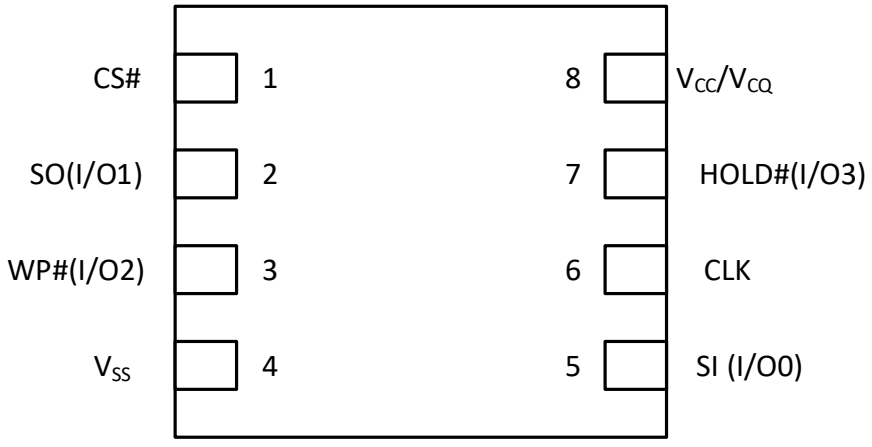


Figure 1: 8-Pin WSON Pin-out

2.2 16-Pin SOIC Pin-Out

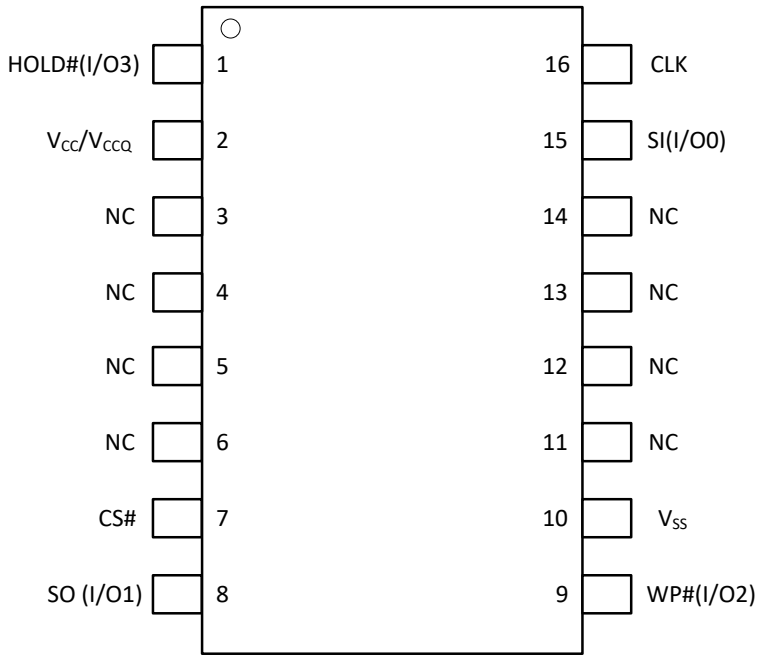


Figure 2: 16-Pin SOIC Pin-Out

3 Pin Description

Signal	Type	Description
SO(I/O1)	Input/output	**Serial Data Input/Output** - Transfers data serially out of the device on the falling edge of CLK - Acts as output during SPI mode - Act as I/O pin during DUAL and QUAD modes - When the device is not selected (CS# driven High), SO(I/O1) pin remains in High Z
SI(I/O0)	Input/output	**Serial Data Input/Output** - Transfers data serially into the device on rising edge of CLK commands, addresses, write data and are latched on the rising edge of CLK - Acts as input during SPI mode - Acts as I/O during DUAL and QUAD modes
CLK	Input	**Serial Clock** - Provides serial interface clock - Rising edge latches commands, addresses, write data on SI(I/O0)

Signal	Type	Description
		- Falling edge triggers output on SO(I/O1) - All data inputs and outputs are synchronized with CLK
CS#	Input	**Chip Select** - When driven Low, places the device in active power mode - When drive High, deselects the device and places SO(I/O1) at high Z - CS# falling edge is required after power-up before a command is written - When a write operation is NOT in progress, the device is in standby power mode
WP#(I/O2)	Input/output	**Serial Data Input/Output** - Transfers data serially into the device on rising edge of CLK commands, addresses, write data and are latched on the rising edge of CLK - Acts as input in SPI mode. When driven Low, the WP# input prevents write operations in the Status Register - Acts as I/O during QUAD modes
HOLD#(I/O3)	Input/output	**HOLD/Serial Data Input/Output** - When driven Low, pauses any serial communications without deselecting the device and places SO(I/O1) at high Z while SI(I/O0) and CLK are ignored - Hold condition requires that CS# is driven Low - Acts as I/O pin during QUAD modes.
V_{CC}	Input	**Supply Core Voltage**
V_{CCQ}	Input	**Supply I/O Voltage**
V_{SS}	Input	**Ground**
NC	-	**Not Connected**

4 SPI Mode

The SPnvSRAM™ devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of CLK, and output data is available from the falling edge of CLK.

The difference between the two modes, as shown below, is the clock polarity when the bus master is in standby mode and not transferring data.

- CLK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- CLK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

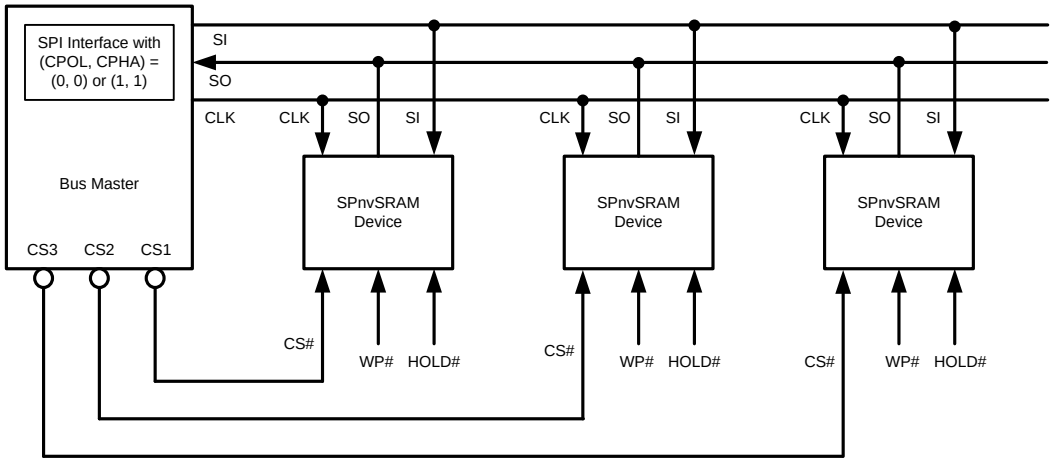


Figure 3 : Bus Master and Memory Devices on the SPI Bus

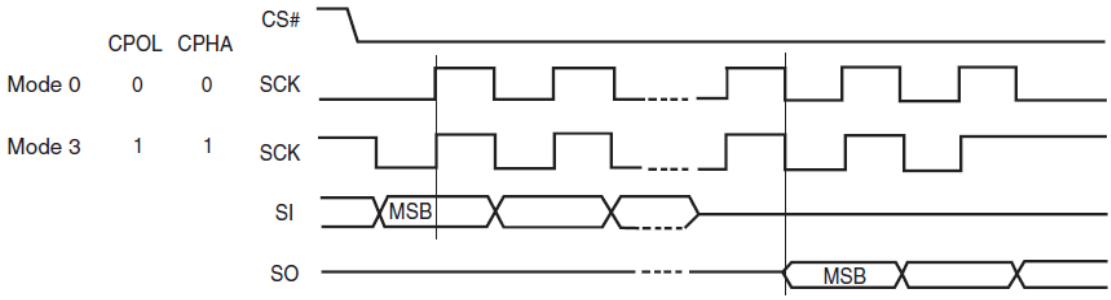


Figure 4 : Supported SPI Modes

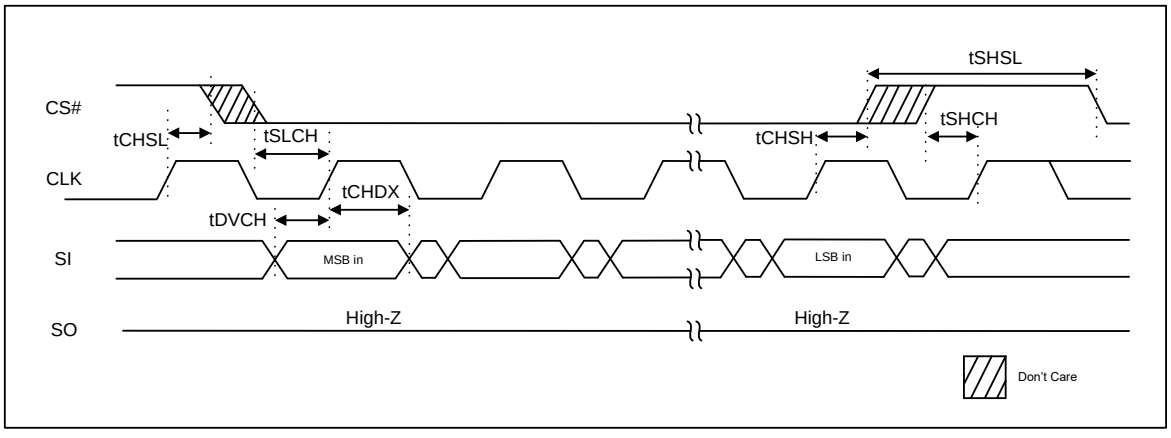


Figure 5: Serial Input Timing

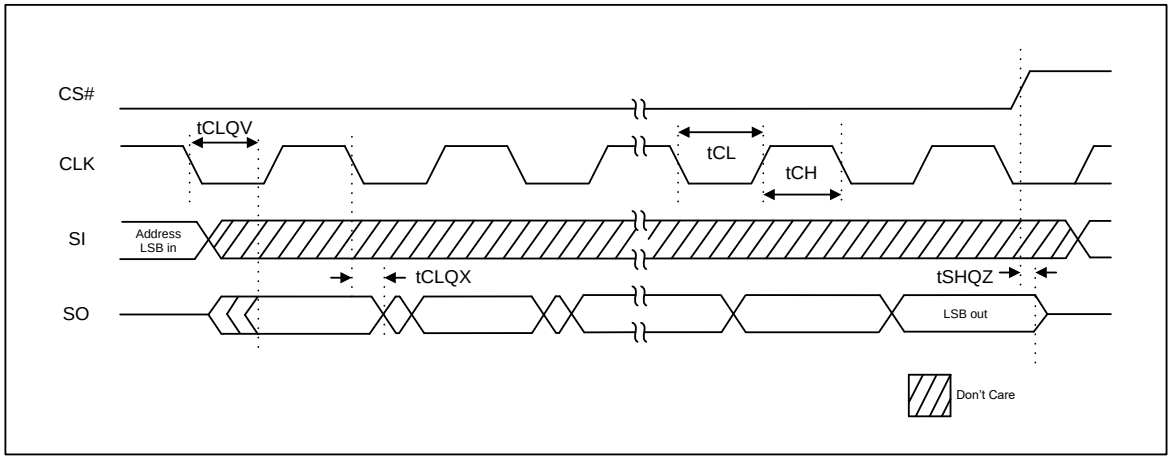


Figure 6: Serial Output Timing

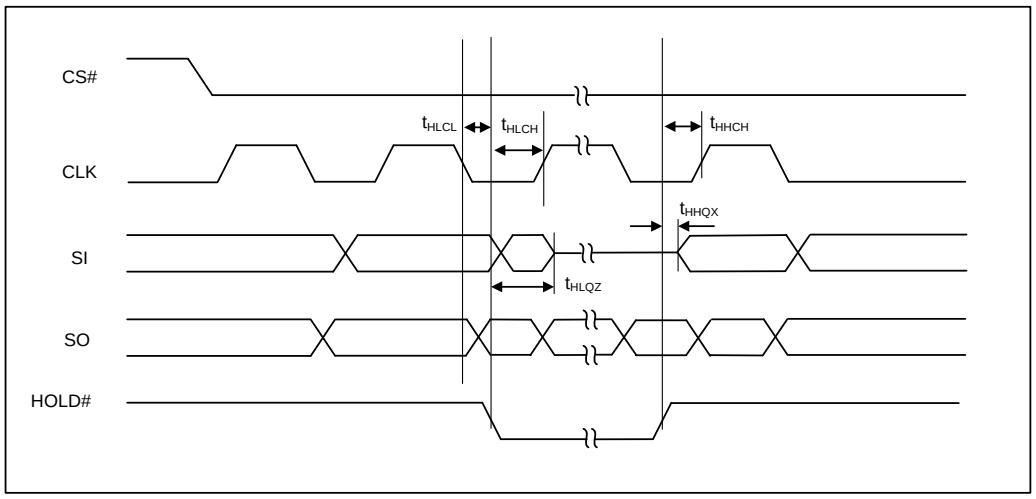


Figure 7: HOLD# Timing

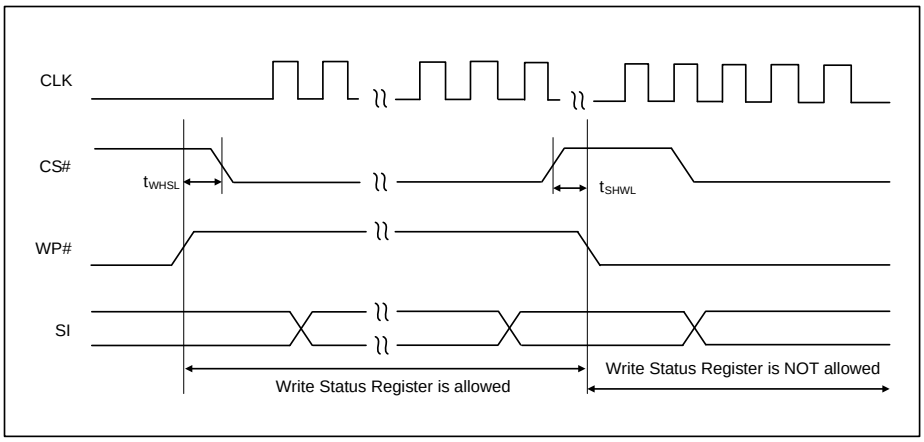


Figure 8: WP# Timing

5 Block Diagram

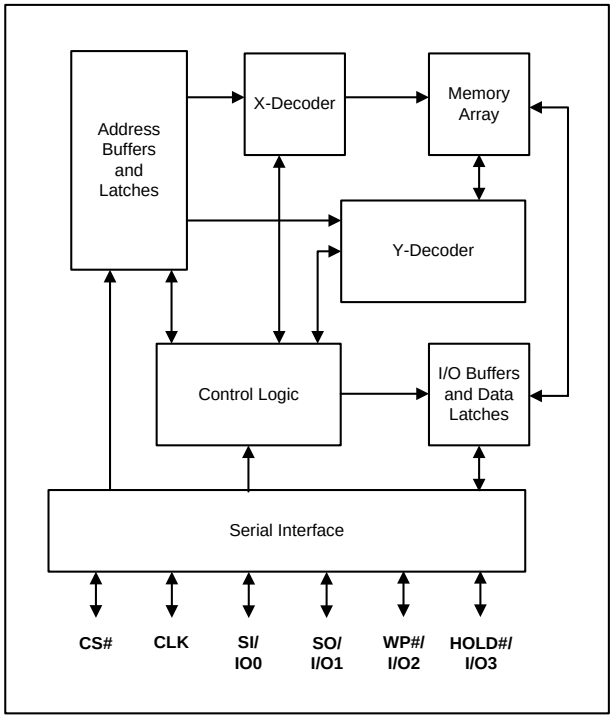


Figure 9: Block Diagram

6 Commands

- Before a command is issued, status register should be check to ensure that the SPnvSRAM is ready.
- Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by 3-byte (24-bit) address plus dummy cycles and data byte(s), as indicated in Table 2 – Command Set.
- The SPnvSRAM always powers up with WEL bit in Status Register reset to 0 to prevent inadvertent Write operations.
- A write memory array operation requires two command opcodes: WREN followed by the WRITE opcode, address and data. The WEL bit is set after the WREN command is issued, and is reset to 0 on the rising edge of CS# at the end of a write operation. Reading the Status Register between the WREN and WRITE opcodes will not clear the WEL bit.
- All commands, addresses, and dummy bits are shifted in the SPnvSRAM device with the most significant bit first. The data bits are also shifted in or out of the SPnvSRAM with the most significant bit.
- CLK continues to toggle during fast read access latency period. At the end of the read latency cycles, the first read data bits are outputted on CLK falling edge.
- The 4Mb SPnvSRAM only requires 19-bit [18:0] address. Therefore the first 5 bits [23:19] must be entered as 0s.
- The 8Mb SPnvSRAM only requires 20-bit [19:0] address. Therefore the first 4 bits [23:20] must be entered as 0s.
- The SPnvSRAM's SPI pins can be configured to work in Dual I/O or Quad I/O modes. When configured in the Dual I/O mode, the SI pin and SO pin become I/O0 pin and I/O1 pin. When configured in the Quad I/O mode, the SI pin, SO pin, WP# pin, and HOLD# pin become I/O0 pin, I/O1 pin, I/O2 pin, and I/O3 pin.
- All attempts to access the memory array during a write cycle are ignored, and the internal cycle, write cycle continues unaffected.
- If the command returns data to the host in a read memory array operation, the SPnvSRAM will continue return data to the host with the same one command until the host drives CS# high. When the highest address is reached, the address counter will roll back to 000000h, and allow the read sequence to be continued indefinitely. The read memory array operation can be terminated by driving CS# high at any time during data output.
- Note: Output Hi-Z is defined as the point where data out is no longer driven.

Table 1 : Command Set

Operation	Command	Description	Command Code (hex)	Address Clock Cycles	Dummy Clock Cycles	Data Byte Cycles	
Control	WREN	Write Enable	06h	0	0	0	
	WRDI	Write Disable	04h	0	0	0	
	DP	Deep-Power Down	B9h	0	0	0	
	RDP	Release from Deep Power Down Mode	ABh	0	0	0	
	RDSR	Read Status Register	05h	0	0	1	
	WRSR	Write Status Register	01h	0	0	1	
Write	WRITE	Write	02h	24	0	2 to 2,048	8Mb
						2 to 1,024	4Mb
	DIW	Dual Input Write	A2h	24	0	2 to 2,048	8Mb
						2 to 1,024	4Mb
	QIW	Quad Input Write	32h	24	0	2 to 2,048	8Mb
						2 to 1,024	4Mb
Read	READ	Read Data Bytes	03h	24	0	1 to ∞	
	FR	Fast Read	0Bh	24	8	1 to ∞	
	DOFR	Dual Output Fast Read	3Bh	24	8	1 to ∞	
	QOFR	Quad Output Fast Read	6Bh	24	8	1 to ∞	
	RDID	Read Identification	9Fh	0	0	1 to 3	

7 Device Operation

7.1 Write Enable (WREN)

The command sequence is shown in Figure 10. The Write Enable (WREN) command puts the device in the write operation modes by setting the WEL bit in the Status Register to 1. The Write Enable command must be followed by any write operations.

The Write Enable (WREN) command is entered by driving Chip Select (CS#) Low, sending the command code, and then driving Chip Select (CS#) High. The WEL bit will be automatically cleared after a WRDI, WRSR or a Write operation completion.

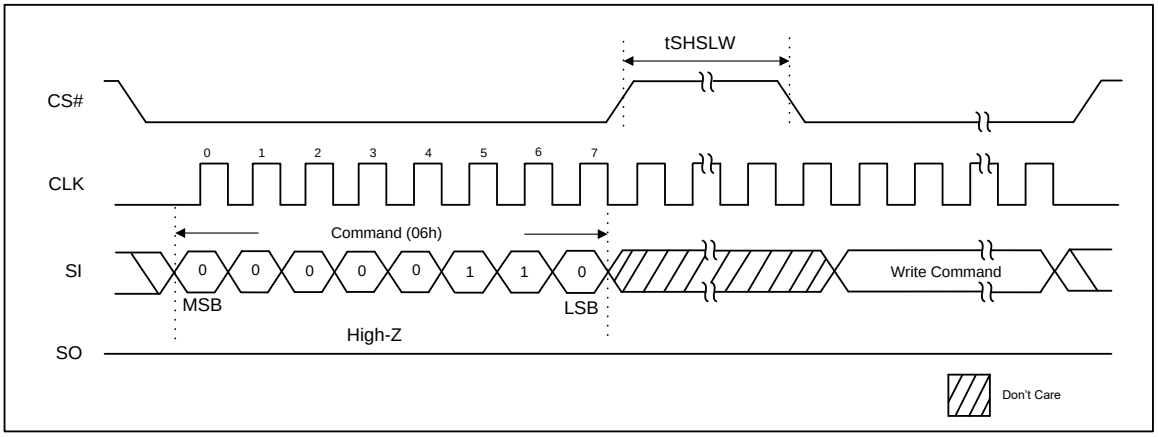


Figure 10: Write Enable (WREN) Command Sequence

7.2 Write Disable (WRDI)

The command sequence is shown in Figure 11. The Write Disable (WRDI) command allows the device to exit the write operation mode.

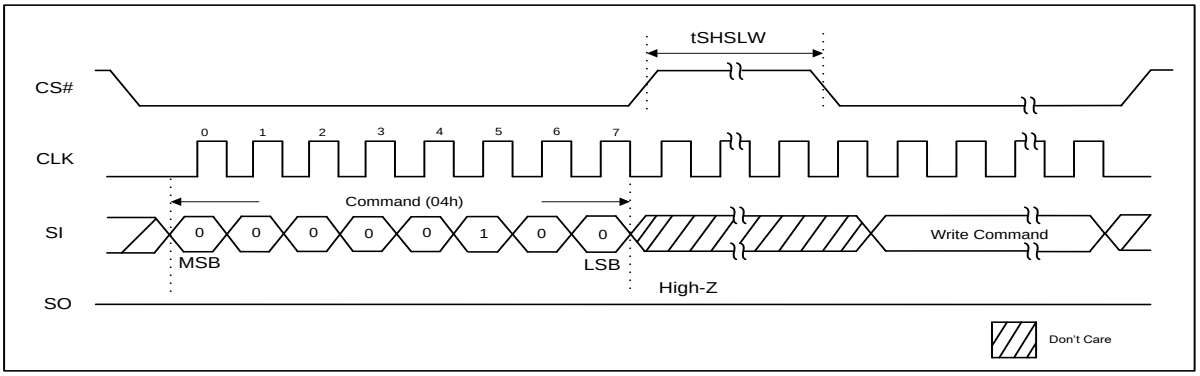


Figure 11: Write Disable (WRDI) Command Sequence

7.3 Read Status Register (RDSR)

The command sequence is shown in Figure 12. The Read Status Register (RDSR) indicates status on whether the memory device is Write enabled, and the state of the memory Write protection. The definition of the status register bits is as below:

Table 2 : Status Register Format

Bit	Description	Field Name	Memory Type	R/W	Default State
7	Write Protect Enable 1 = Protects when WP# is LOW 0 = No protection even WP# is LOW	WPEN	NV	R/W	0
6	Reserved	-	-	-	0
5	Not Used	-	-	-	0
4	Block Protect Bits	BP2	NV	R/W	0
3		BP1	NV	R/W	0
2		BP0	NV	R/W	0
1	Write Enable Latch 1 = Write Operation Enabled 0 = Write Operation Disabled	WEL	V	R	0
0	Reserved	-	-	-	0

7.3.1 WEL Bit

The WEL bit indicates the state of the Write Enable Latch. The Write Enable command set the WEL bit to 1 to enable any Write memory array or Write Register commands. The Write Disable command resets the WEL bit to "0" to prevent all write commands from execution. The Write Status Register command does not affect the WEL bit.

WEL bit is clear (reset to 0) after the following operations:

- Hardware Reset or Software Reset
- WRDI command completion
- After a WRITE memory array command completion
- After a Write Status Register command completion

7.3.2 Block Protect (BP2, BP1, BP0) Bits

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against write command. These bits are written with the Write Status Register (WRSR) command. When one or more of the Block Protect (BP2, BP1, BP0) bits is set to "1", the relevant memory area (as

defined in Table 4) becomes protected. These bits can be written provided that the hardware protected mode has not been set.

7.3.3 Write Protect Enable (WPEN) Bit

The Write Protect Enable (WPEN) bit is operated in conjunction with the Write Protect (WP#) Signal. The Write Protect Enable (WPEN) bit and the Write Protect Signal allow the device to be put in the Hardware Protected Mode (HPM). In this mode, the non-volatile bits of the Status Register (WPEN, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) command is no longer accepted for execution. The hardware protected (HPM) mode can be entered:

- By setting the Write Protect Enable (WPEN) bit to "1" after driving Write Protect (WP#) Low
- Or by driving Write Protect (WP#) LOW after setting the Write Protect Enable (WPEN) bit to "1"

The only way to exit the Hardware Protected Mode (HPM) once entered is to drive Write Protect (WP#) High.

If Write Protect (WP#) is permanently tied high, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the block protect (BP2, BP1, BP0) bits of the Status Register, can be used.

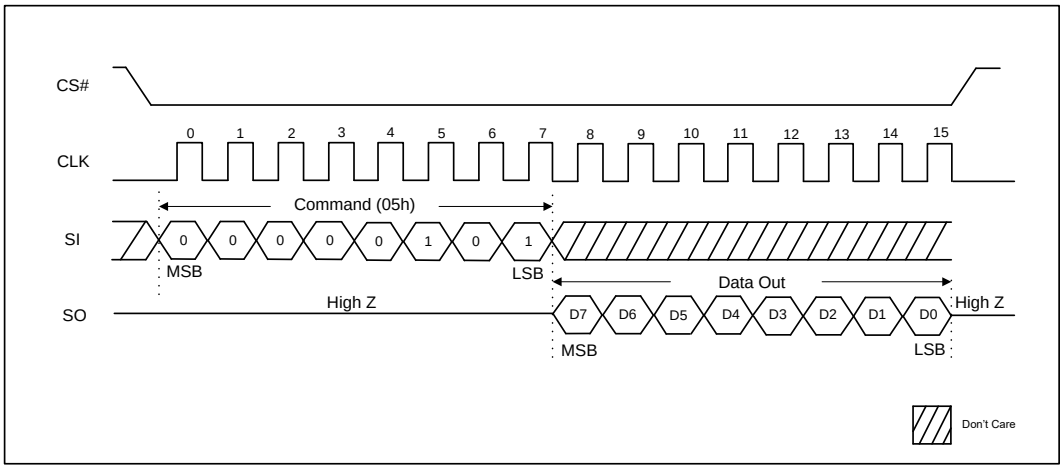


Figure 12: Read Status Register (RDSR) Command Sequence

7.4 Write Status Register (WRSR)

The command sequence is shown in Figure 13. The Write Status Register (WRSR) command allows new values to be written to the status register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable latch (WEL) in the Read Status Register (RDSR).

The Write Status Register (WRSR) command is entered by driving Chip Select (CS#) Low, followed by the command code and the 1 data byte on serial data input (DQ0).

The Write Status Register (WRSR) command has no effect on bit1 and bit0 of the status register.

Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed.

The Write Status Register (WRSR) command allows the user to change the values of the block protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 5. The Write Status Register (WRSR) command is not executed once the hardware protected mode is entered.

When the Write Protect Enable (WPEN) bit of the status register is 0 (its initial delivery state), it is possible to write to the status register provided that the Write Enable latch (WEL) bit has previously been set by a Write Enable (WREN) command, regardless of whether Write Protect (WP#) is driven High or Low.

When the Write Protect Enable (WPEN) bit of the status register is set to '1', two cases need to be considered, depending on the state of Write Protect (WP#):

- If Write Protect (WP#) is driven high, it is possible to write to the status register provided that the Write Enable latch (WEL) bit has previously been set by a Write Enable (WREN) command.
- If Write Protect (WP#) is driven Low, it is not possible to write to the Status register even if the Write Enable latch (WEL) bit has previously been set by a Write Enable (WREN) command (attempts to write to the status register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are Software protected (SPM) by the block protect (BP2, BP1, BP0) bits of the status register, are also hardware protected against data modification.

Table 3: Protection Modes

WEL Bit	WPEN Bit	WP# Signal	Status Register	Memory Content	
				Protected Area	Unprotected Area
0	X	X	Protected	Protected	Protected
1	0	X	Unprotected	Protected	Unprotected
1	1	LOW	Protected	Protected	Unprotected
1	1	HIGH	Unprotected	Protected	Unprotected

Table 4: 4Mb/8Mb Block Addresses

Block Protect			Protected Area
BP2	BP1	BP0	
0	0	0	None
0	0	1	Upper 1/32th of Memory Array
0	1	0	Upper 1/16th of Memory Array
0	1	1	Upper 1/8th of Memory Array
1	0	0	Upper 1/4th of Memory Array
1	0	1	Upper 1/2th of Memory Array
1	1	0	Full Memory
1	1	1	Full Memory

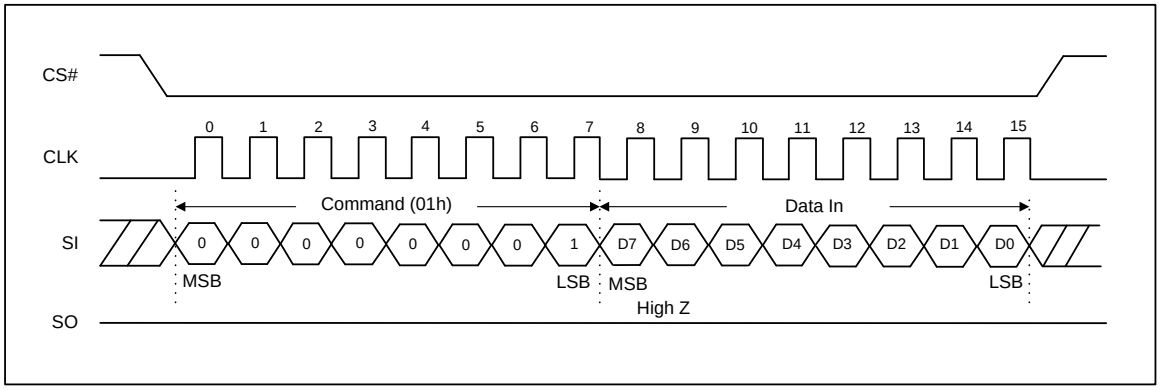


Figure 13: Write Status Register (WRSR) Command Sequence

7.5 Hold Condition

The command sequence is shown in Figure 14. The HOLD# Signal is used to pause a serial communication underway with the SPnvSRAM device without resetting the clocking sequence.

To perform a Hold operation, CS# must be driving Low. The Hold mode begins on the falling edge of the HOLD# Signal coincides with CLK being low. The Hold mode ends when the HOLD# Signal's rising edge coincides with the CLK being low.

During the Hold mode, SO will be in high-impedance while SI and CLK are Don't Care.

If CS# is driven high during a Hold condition, the internal logic of the SPnvSRAM device is reset. As long as HOLD# Signal is low, the device remains in the Hold condition. To resume communication with the SPnvSRAM device, HOLD# must be driven High, and then CS# must be driven Low. This prevents the SPnvRAM device from going back to the Hold condition.

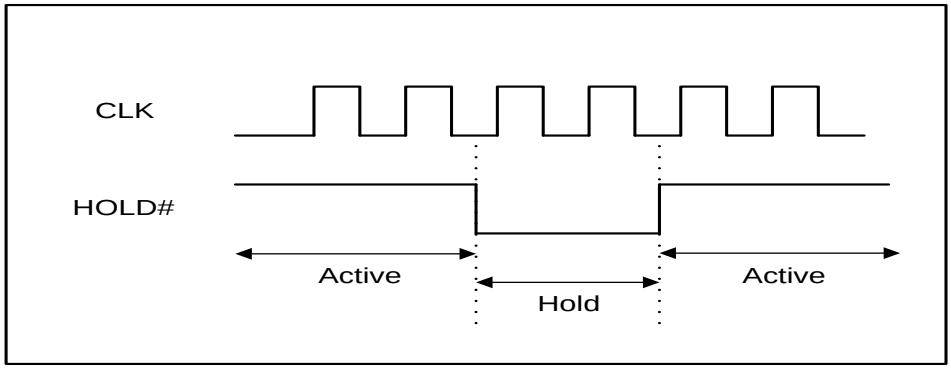


Figure 14: Hold Condition

7.6 Write (WRITE)

The command sequence is shown in Figure 15. The Write (WRITE) command allows bytes to be written in the memory.

To perform a write operation, two commands are required: Write Enable (WREN), which is one byte, and a WRITE sequence, which consists of four bytes for command and address plus data. If only two bytes to be written, the CS# must be driven High after the last bit (LSB) of data is shifted in.

For WRITE operation, there are three requirements:

1. Address should be 2-byte aligned (A0 = 0)
2. Number of written bytes should be multiple of 2
3. Data transfer length per command must be within 1,204-byte (4Mb) or 2,048-byte (8Mb) boundary

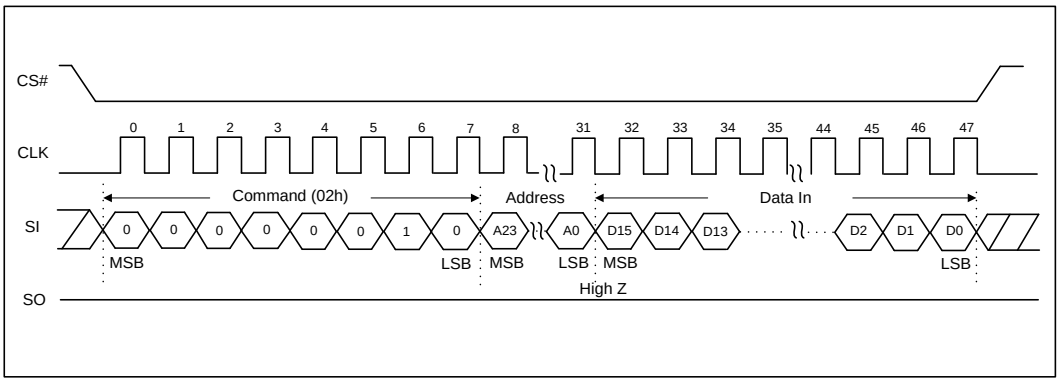


Figure 15: Write (WRITE) Command Sequence

7.7 Dual Input Write (DIW)

The command sequence is shown in Figure 16. The Dual Input Write (DIW) command is similar to the WRITE command, except that the Dual Input Write (DIW) command allows data to be written in the memory using two pins: I/O1 and I/O0, instead of only one pin SI for the WRITE command. The Dual Input Write (DIW) operation is two times the data transfer bandwidth compared to the WRITE operation.

To perform a Dual Input Write (DIW) operation, two commands are required: Write Enable (WREN), which is one byte, and a Dual Input Write sequence, which consists of four bytes for command and address plus data using two input pins at the same time at a maximum frequency f_C.

For Dual Input Write operation, there are three requirements:

1. Address should be 2-byte aligned (A0 = 0)
2. Number of written bytes should be multiple of 2
3. Data transfer length per command must be within 1,204-byte (4Mb) or 2,048-byte (8Mb) boundary

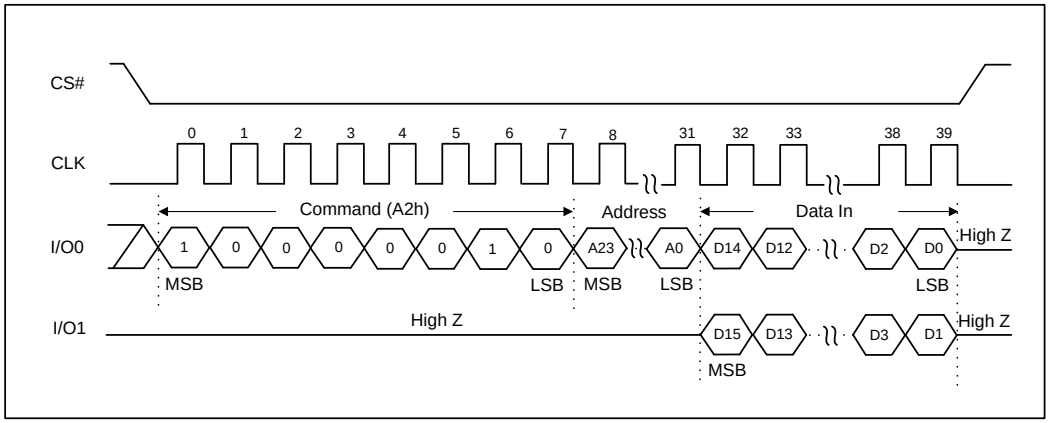


Figure 16: Dual Input Write (DIW) Command Sequence

7.8 Quad Input Write (QIW)

The command sequence is shown in Figure 17. The Quad Input Write (QIW) command is similar to the WRITE command, except that the Quad Input Write (QIW) command allows data to be written in the memory using four pins: I/O3, I/O2, I/O1 and I/O0, instead of only one pin SI for the WRITE command.

To perform a Quad Input Write (QIW) operation, two commands are required: Write Enable (WREN), which is one byte, and a Quad Input Write sequence, which consists of four bytes for command and address plus data using four input pins at the same time at a maximum frequency f_C.

For Quad Input Write operation, there are four requirements:

1. Address should be 2-byte aligned (A0 = 0)
2. Number of written bytes should be multiple of 2
3. Data transfer length per command must be within 1,204-byte (4Mb) or 2,048-byte (8Mb) boundary
4. t_{HLCL} delay is required after the last bit of address (A0) for input data to be valid

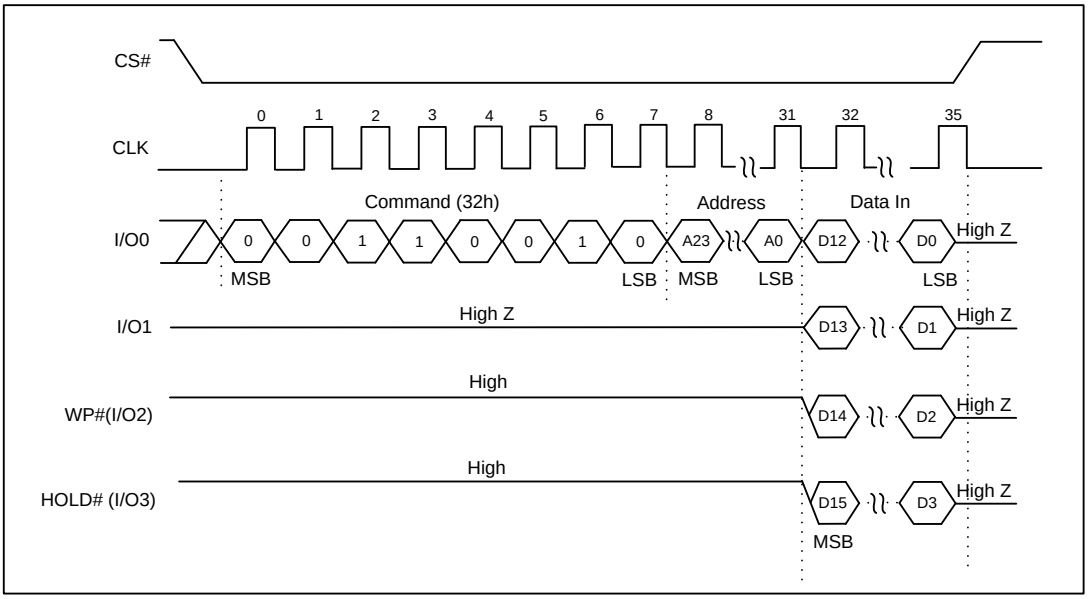


Figure 17: Quad Input Write (QIW) Command Sequence

7.9 Read Data Bytes (READ)

The command sequence is shown in Figure 18. The address is latched on rising edge of CLK, and data shifts out on the falling edge of CLK at a maximum frequency f_R. The address is automatically incremented to the next higher address after every byte of data is shifted out. The whole memory can, therefore, be read with a

Single Read Data Bytes (READ) command. When the highest address is reached, the address counter will roll back to 000000h, and allow the read sequence to be continued indefinitely.

The Read Data Bytes (READ) command is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) command while a write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

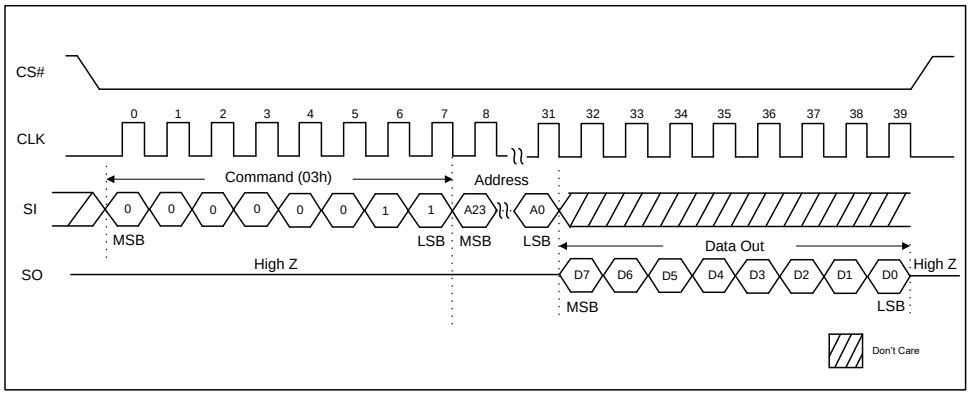


Figure 18: Read Data Bytes (READ) Command Sequence

7.10 Fast Read (FR)

The command sequence is shown in Figure 19. The Fast Read (FR) command is Similar to the read data bytes (READ) command with the addition of 8 dummy cycles after the address and before the first data is sent out.

The address is latched on rising edge of CLK, and data shifts out on the falling edge of CLK at a maximum frequency f_C. The address is automatically incremented to the next higher address after every byte of data is shifted out. The whole memory can, therefore, be read with Single Fast Read (FR) command. When the highest address is reached, the address counter will roll over to 000000h, and allow the read sequence to be continued indefinitely.

The Fast Read (FR) command is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Fast Read (FR) command while a write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

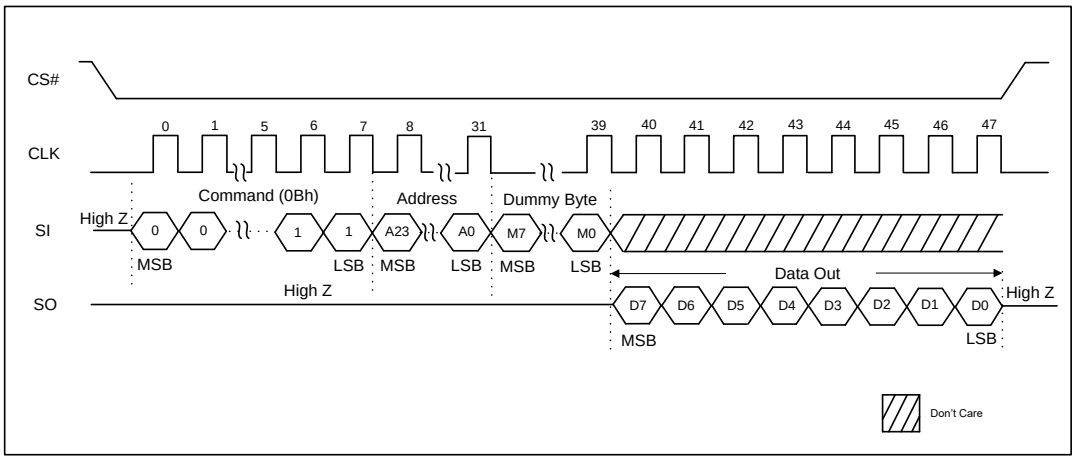


Figure 19: Fast Read (FR) Command Sequence

7.11 Dual Output Fast Read (DOFR)

The command sequence is shown in Figure 20. The Dual Output Fast Read (DOFR) command is Similar to the Fast Read (FR) command, except that the Dual Output Fast Read (DOFR) command allows data to be read from the memory using two pins: I/O1 and I/O0 instead of only one pin SI for the Fast Read (FR) command. The Dual Output Fast Read (DOFR) operation doubles the data transfer bandwidth compared to the Fast Read (FR) operation.

The Dual Output Fast Read (DOFR) command is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Dual Output Fast Read (DOFR) command while a write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

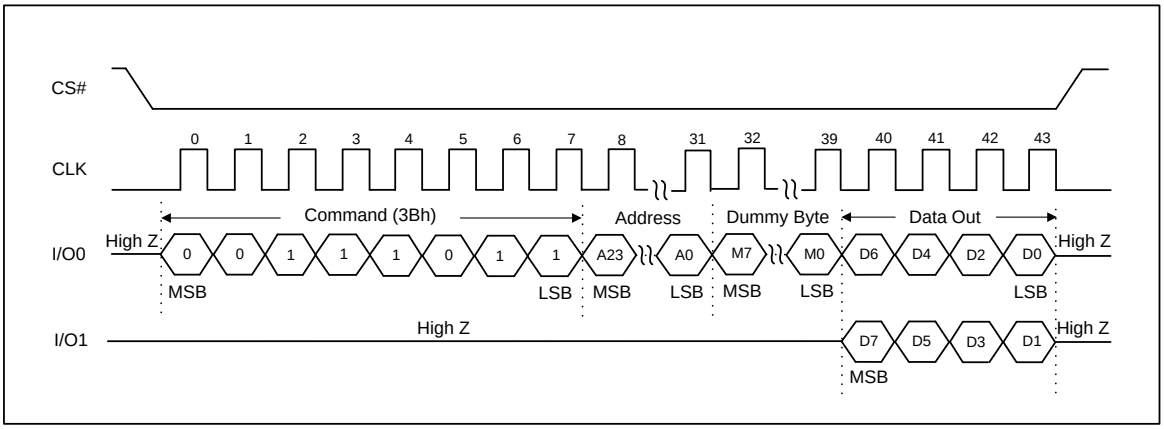


Figure 20: Dual Output Fast Read (DOFR) Command Sequence

7.12 Quad Output Fast Read (QOFR)

The command sequence is shown in Figure 21. The Quad Output Fast Read (QOFR) command is similar to the Fast Read command, except that the data is shifted out four bits at a time on four pins I/O3, I/O2, I/O1 and I/O0 instead of only one. The Quad Output Fast Read (QOFR) operation doubles the data transfer bandwidth compared to the Dual Output Fast Read operation, and is four times the data transfer bandwidth compared to the Fast Read operation.

The Quad Output Fast Read (QOFR) command is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Quad Output Fast Read (QOFR) command while a write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

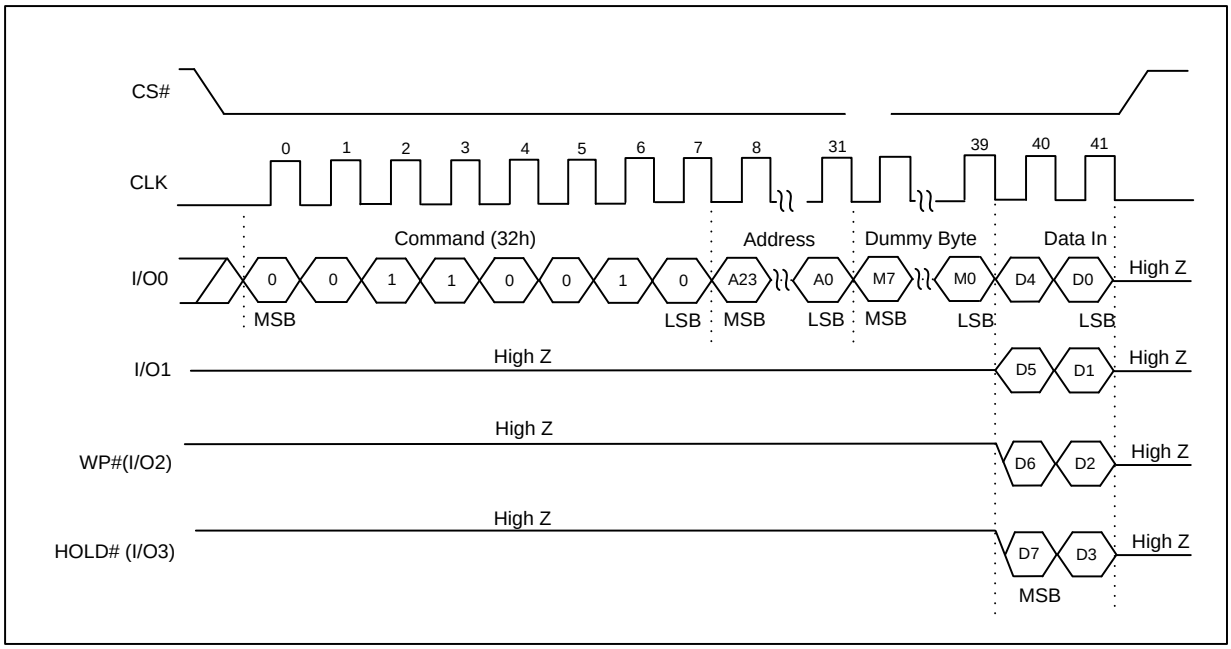


Figure 21: Quad Output Fast Read (QOFR) Command Sequence

8 Power Modes

8.1 Active Power and Standby Power

When Chip Select (CS#) is Low, the device is enabled and in the Active Power mode. When CS# is High, the device is disabled but could remain in the Active Power mode until all internal operations have completed. The device then goes into the Standby Power mode. The device consumption drops to I_{SB}.

8.2 Deep Power-Down (DP)

The command sequence is shown in Figure 22. The Deep Power-Down mode can only be entered by executing the Deep Power-Down (DP) command. As a result, the device consumption drops to I_{DPD}. It can also be used as a Software protection mechanism, while the device is not in active use, as in this mode, the device ignores all commands except the Release From Deep Power-Down (RDP) command.

The Deep Power-Down (DP) command is entered by driving Chip Select (CS#) Low, followed by the command code on serial data input SI.

Chip Select (CS#) must be driven High after the eighth bit of the command code has been latched in, otherwise the Deep Power-Down (DP) command is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{EDP} before the supply current is reduced to I_{DPD} and the Deep Power-Down mode is entered.

To take the device out of Deep Power-Down mode, the RDP command must be issued. No other command must be issued while the device is in Deep Power-Down mode.

The Deep Power-Down mode automatically stops at power-down and the device always powers up in the Standby power mode. The device rejects any DP command issued while it is executing a Write or Write Status Register operation, and continues the operation uninterrupted.

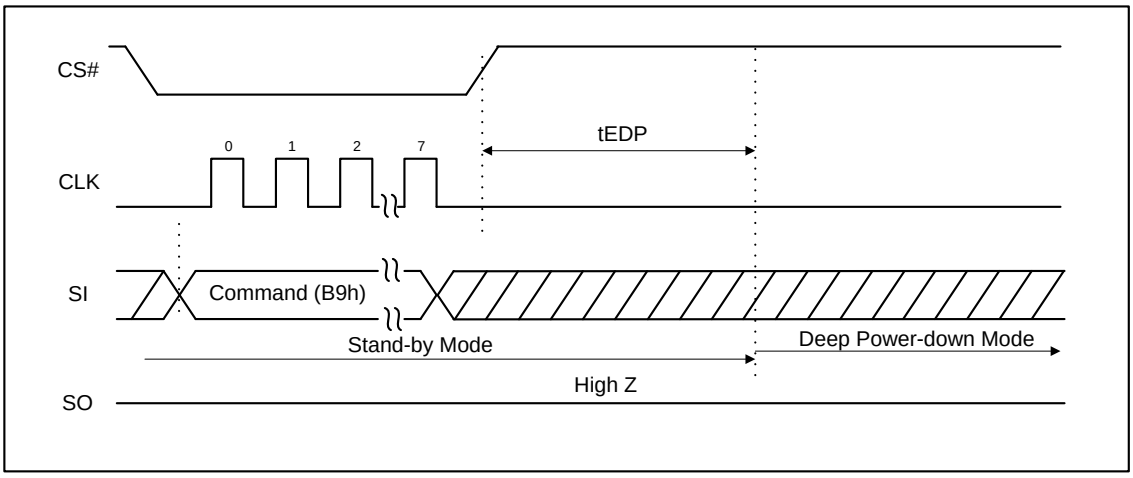


Figure 22: Deep Power-Down (DP) Command Sequence

8.3 Release From Deep Power-Down (RDP)

The command sequence is shown in Figure 23. Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release-From-Deep-Power-Down (RDP) command. Executing this command takes the device out of the Deep Power-Down mode.

The RDP command is entered by driving Chip Select (CS#) Low, followed by the command code on serial data input SI.

The Release-From-Deep-Power-Down (RDP) command is terminated by driving Chip Select (CS#) High. Sending additional clock cycles on Serial Clock (CLK), while Chip Select (CS#) is driven Low, causes the command to be rejected, and not executed.

After Chip Select (CS#) has been driven High, followed by a delay, t_{RDP}, the device is put in the standby mode. Chip Select (CS#) must remain High at least until this period is over.

Any RDP command, while a write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

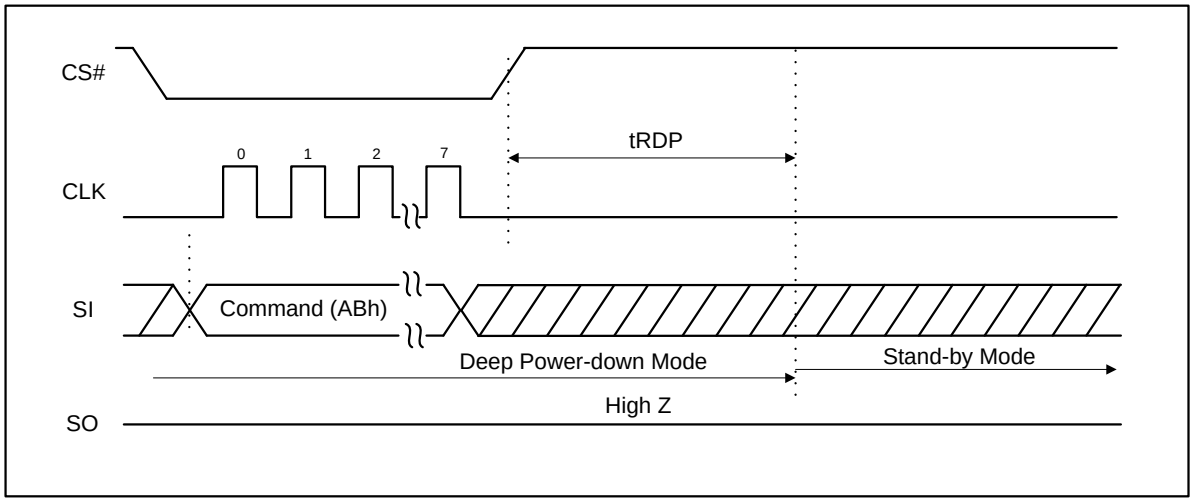


Figure 23: Release from Deep Power-Down (RDP) Command Sequence

9 Read Identification (RDID)

The command sequence is shown in Figure 24. The Read Identification (RDID) command provides the JEDEC assigned one-byte Manufacturer ID, the two-byte Device ID: the Memory Type, and the Memory Density.

The command is initiated by driving CS# pin low and shifting the command code 9Fh. After which, the Manufacturer ID for Avalanche E6h, the Memory Type, and the Memory Density are shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID values are listed in table of ID Definitions below. The command is completed by driving CS# High.

Table 5: ID Definitions

Command	Manufacturer ID	Device ID1 Memory Type (ID15 – ID08)	Device ID2 Memory Density (ID7 – ID0)	
			4Mb	8Mb
RDID	E6h	C1h	94h	96h

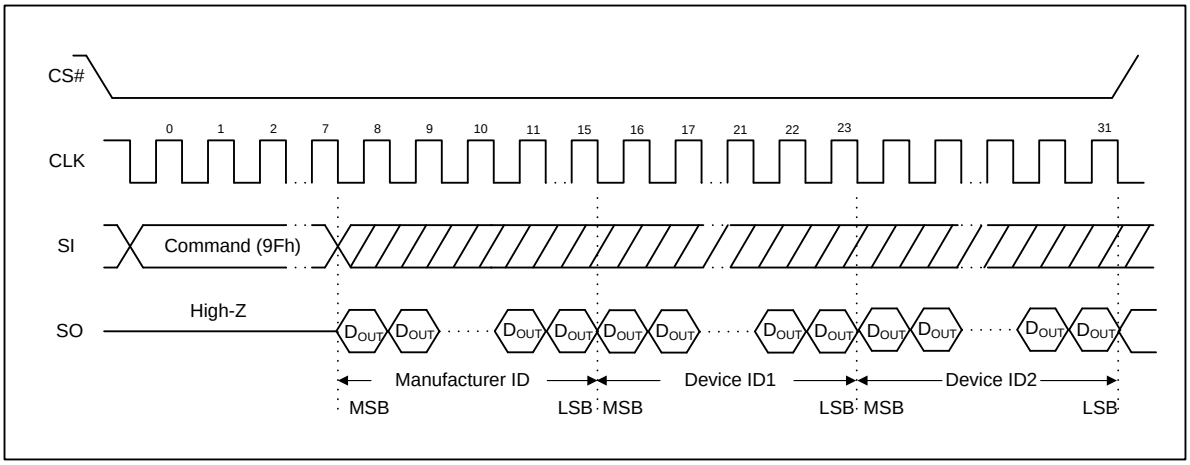


Figure 24: Read Identification (RDID) Command Sequence

10 Power Up and Power Down Requirements

The memory array must not be selected during power-up and power-down unless the following conditions are met:

- CS# must be at the final value of V_{CC}
- V_{CC} larger than V_{CC} min at power-up
- Ground must be within acceptable low value at power-down

Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor (typically 100nF) close to the package pins. At power-down, when V_{CC} drops below the power-on-reset threshold voltage as shown below, all operations are disabled and the device does not respond to any command. Adding a pull-up resistor on CS# may ensure a safe and proper power-up and power down level.

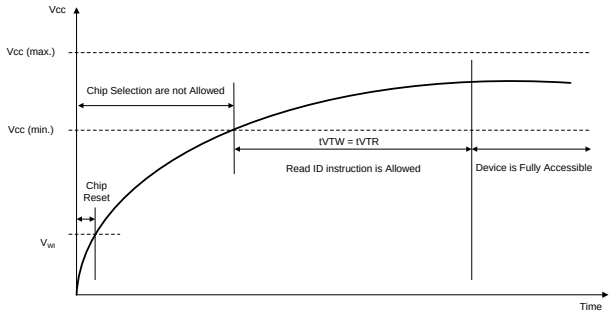


Figure 25: Power Up Timing

Table 6: Power Up Voltage & Timing

Symbol	Parameter	Min	Max	Unit
t_{VTR}	VCC (min) to Read	-	150	µs
T_{VTW}	VCC (min) to Device Fully Accessible	-	150	µs
V_{WI}	Write Inhibit Threshold Voltage	-	1.5	V

11 DC and AC Parameters

This section presents the DC and AC characteristics of the device. The values for the DC and AC parameters indicated in the following tables are derived from tests under the operating and measurement conditions also indicated in the relevant tables. Designers should be aware that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7: Operating Conditions

Symbol	Parameter		Min.	Max.	Unit
V_{CC} /V_{CCQ}	Single Supply Voltage		1.7	2.0	V
C	Operating Temperature	Commercial	0	85	°C
I		Industrial	-40	85	°C
E		Extended	-40	105	°C

Table 8: Endurance and Data Retention (T_A = 85ºC)

Parameter	Value	Unit
Read & Write	10^{14}	Times per Byte

Parameter	Value	Unit
Data Retention	>20	Years

Table 9: DC Characteristics (T_A = 85ºC)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		--	--	± 1	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$		--	--	± 1	µA
I_{SB}/I_{DPD}	Standby/Deep Power Down Current	CS# = V_{CC}, All Other Inputs = V_{CC} or V_{SS}		--	200	800	µA
I_{CC}	Active	CS# = V_{SS}, All Other Inputs = V_{CC} or V_{SS}, SO =Open, CLK Toggling		--	--	1,500	µA
I_{CC1}	V_{CC} Read		1MHz	--	--	2	mA
			40MHz	--	--	25	mA
I_{CC2}	V_{CC} Write		1MHz	--	--	3	mA
			40MHz	--	--	30	mA
V_{IL}	Input low voltage	--		-0.5	--	+0.2V_{CC}	V
V_{IH}	Input high voltage	--		0.8V_{CC}	--	V_{CC}+0.3	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		--	--	0.4	V
V_{OH}	Output high voltage	I_{OH} = -1.6 mA		V_{CC} - 0.5	--	--	V
I_{LTH}	Latch Up Protection	--		100+I_{CC1}	--	--	mA

Table 10: AC Measurement Conditions (T_A = 85ºC)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	--	8	pF
$C_{I/O}$	I/O capacitance	V_{OUT} = 0V	--	12	pF
C_{LOAD}	Load capacitance	-	--	30	pF

Table 11: AC Test Condition (T_A = 85ºC)

Parameter	Value	Unit
Power Supply Voltage	1.7 to 2.0	V
Input Pulse Levels	0 and Vcc	V
Input Rising and Falling time	3	ns
Input and Output Timing Reference Levels	0.5Vcc	V

Table 12: AC Timing Parameter (T_A = 85ºC)

Symbol	Parameter	Min.	Max.	Unit	Note
f_C	Clock Frequency for FR, DOFR, QOFR, WRITE, DIW, QIW, WREN, WRDI, and RDID	1	40	MHz	
f_R	Clock Frequency for READ	1	40	MHz	1
t_{CH}	Clock High Time	11	--	ns	2
t_{CL}	Clock Low Time	11	--	ns	2
t_{SLCH}	CS# Active Setup Time relative to CLK	8	--	ns	
t_{SHCH}	CS# Not Active Setup Time relative to CLK	8	--	ns	
t_{SHSL}	CS# Not Active after a Command	80	--	ns	
t_{SHSLW}	CS# High Time (End of Memory Array Write)	400	--	ns	
t_{CHSH}	CS# Active Hold Time relative to CLK	8	--	ns	
t_{CHSL}	CS# Not Active Hold Time relative to CLK	8	--	ns	
t_{DVCH}	Data In Setup Time	5	--	ns	
t_{CHDX}	Data In Hold Time	5	--	ns	
t_{SHQZ}	Output Disable Time	--	20	ns	
t_{CLQV}	CLK Low to Output Valid	--	10	ns	
t_{CLQX}	Output Hold Time relative to CLK Low	0	--	ns	
t_{WHSL}	WP# (I/O2) Setup Time before CS# Low	10	--	ns	
t_{SHWL}	WP# (I/O2) Hold Time before CS# Low	10	--	ns	
t_{HLCH}	HOLD# (I/O3) Setup Time relative to CLK High	6	--	ns	
t_{HLCL}	HOLD# (I/O3) Setup Time relative to CLK Low	2	--	ns	
t_{HHCH}	HOLD# (I/O3) Hold Time relative to CLK High	6	--	ns	

Symbol	Parameter	Min.	Max.	Unit	Note
t_{HHQX}	HOLD# (I/O3) to Output Low-Z	--	20	ns	
t_{HLQZ}	HOLD# (I/O3) to Output High-Z	--	20	ns	
t_{EDP}	CS# High to Deep Power Down Mode	--	3	µs	
t_{RDP}	Release DP Mode	--	3	µs	

Note:

1. Future design: $f_C > f_R$
2. Clock high + Clock Low must be less than or equal to $1/f_C$

12 Maximum Ratings

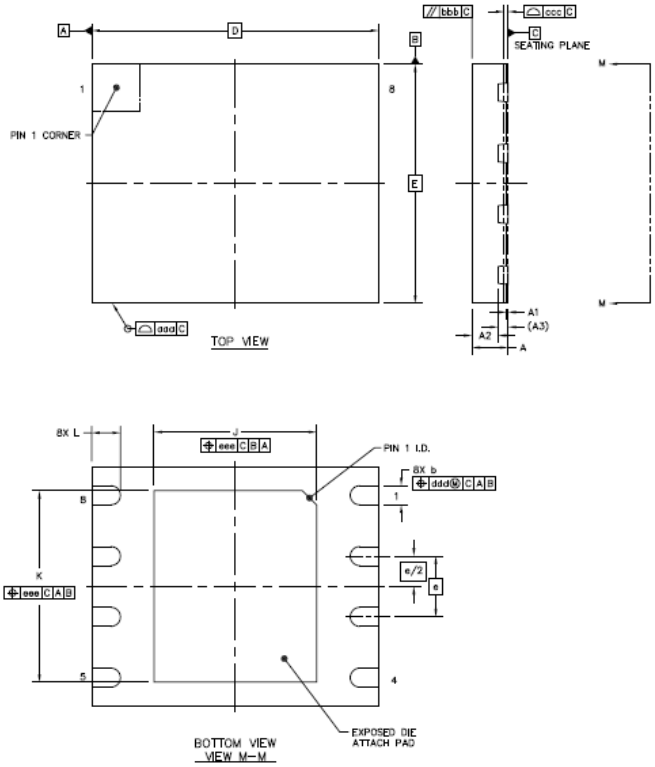
Stressing the device outside the ratings listed in Table 13 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	-55	125	°C
V_{IO}	Input/output voltage with reference to ground	-0.5	V_{CC} + 0.4	V
V_{CC}	Supply Voltage	-0.5	2.45	V

13 Package Diagram

13.1 8-Pin WSON Package Diagram



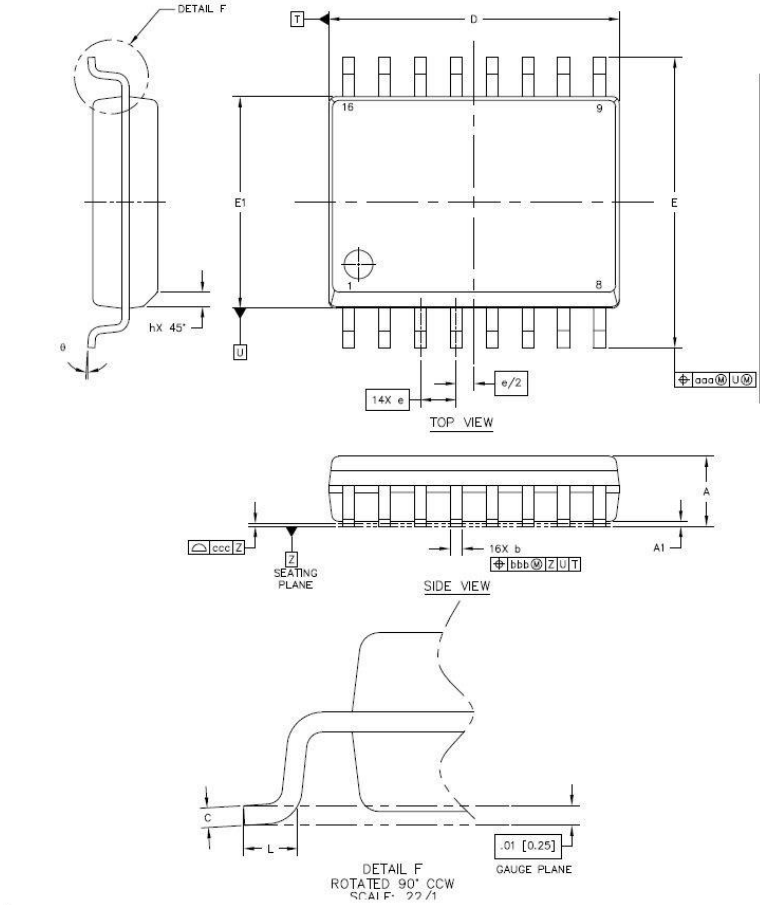
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.35	0.4	0.45
BODY SIZE	X	D		6 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		1.27 BSC	
EP SIZE	X	J	3.3	3.4	3.5
	Y	K	3.9	4	4.1
LEAD LENGTH		L	0.55	0.6	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 26: 8-Pin WSON Package Outline

13.2 16-Pin SOIC Package Diagram



	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.093	---	.104	2.35	---	2.65
STAND OFF	A1	.004	---	.010	0.10	---	0.25
LEAD WIDTH	b	.014	---	.019	0.35	---	0.49
L/F THICKNESS	c	.009	---	.013	0.23	---	0.32
BODY SIZE	D	.400	---	.411	10.15	---	10.45
	E1	.291	---	.299	7.40	---	7.60
	E	.396	---	.415	10.05	---	10.55
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016	---	.039	0.40	---	1.00
	h	.010	---	.030	0.25	---	0.75
	θ	0°	---	7°	0°	---	7°
LEAD EDGE OFFSET	aaa	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	ccc	.004			0.10		

Figure 27: 16-Pin SOIC Package Outline

14 Part Information Scheme

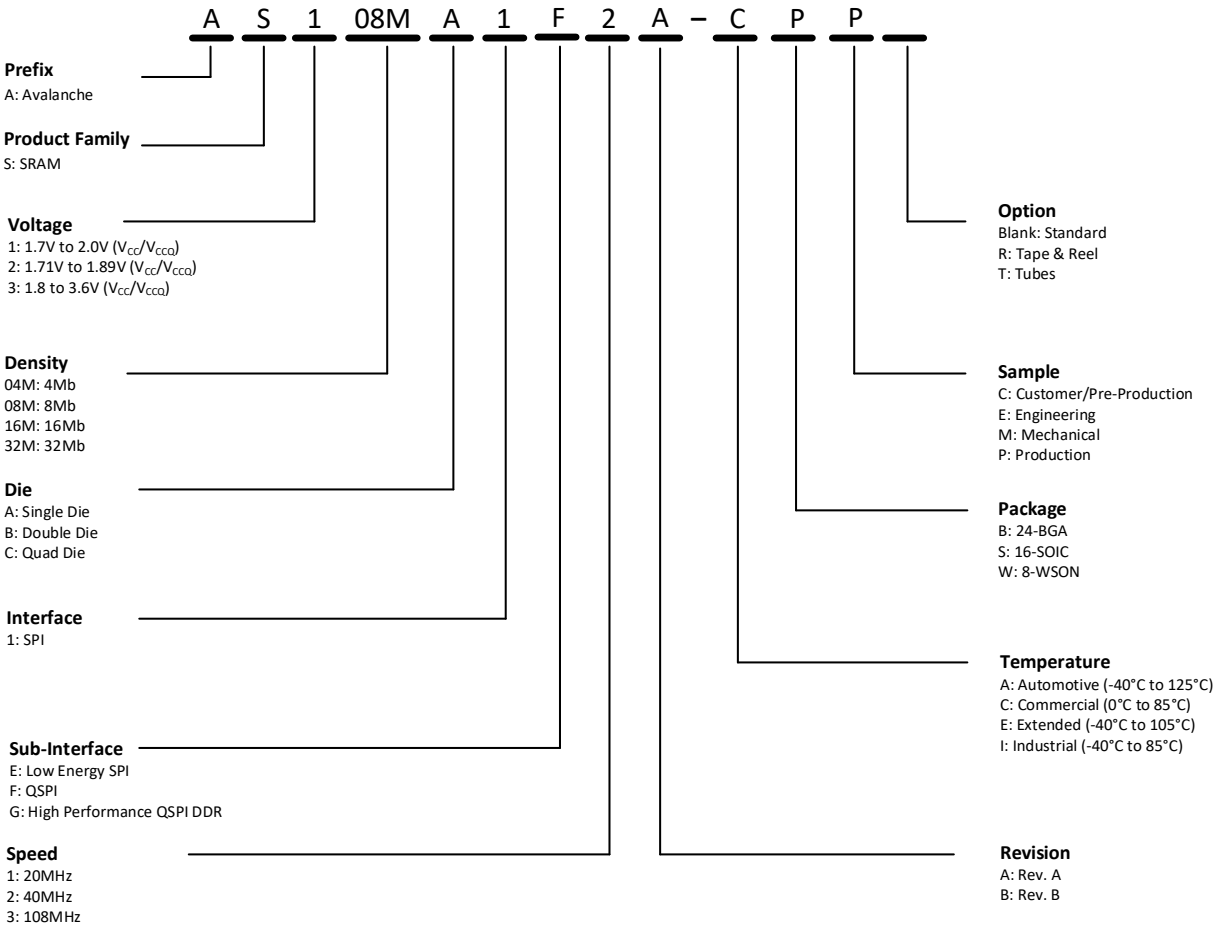


Figure 28: Part Information Scheme

15 Ordering Information

Table 14: Ordering Information

Part Number	Density	Clock Freq.	Operation (V_{CC}/V_{CCQ}) Voltage	Operating Temperature	Package
AS104MA1F2A-CWP	4Mb	40MHz	1.7V-2.0V	Commercial	8-WSON
AS104MA1F2A-IWP	4Mb	40MHz	1.7V-2.0V	Industrial	8-WSON
AS104MA1F2A-EWP	4Mb	40MHz	1.7V-2.0V	Extended	8-WSON
AS104MA1F2A-CSP	4Mb	40MHz	1.7V-2.0V	Commercial	16-SOIC
AS104MA1F2A-ISP	4Mb	40MHz	1.7V-2.0V	Industrial	16-SOIC
AS104MA1F2A-ESP	4Mb	40MHz	1.7V-2.0V	Extended	16-SOIC
AS108MA1F2A-CWP	8Mb	40MHz	1.7V-2.0V	Commercial	8-WSON
AS108MA1F2A-IWP	8Mb	40MHz	1.7V-2.0V	Industrial	8-WSON
AS108MA1F2A-EWP	8Mb	40MHz	1.7V-2.0V	Extended	8-WSON
AS108MA1F2A-CSP	8Mb	40MHz	1.7V-2.0V	Commercial	16-SOIC
AS108MA1F2A-ISP	8Mb	40MHz	1.7V-2.0V	Industrial	16-SOIC
AS108MA1F2A-ESP	8Mb	40MHz	1.7V-2.0V	Extended	16-SOIC

Revision History

Revision No.	Date	History
1.0	11/15/2017	Initial Release
1.1	02/12/2018	Added 4Mb Information
1.2	08/27/2018	Cosmetic Changes

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