

## 8Mb – 64Mb Embedded S-MRAM Macro (eSRAM)

Revision: A

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Page 1 | 17



## Purpose

The document describes the system level requirements for 8Mbit-64Mbit Embedded S-MRAM (eSRAM) macro. It includes the following:

- Executive Summary
- What' Available in the Market
- Application Space
- Market Positioning
- Signal Description & Assignment
- Bus Interface
- Electrical Specifications

## Background on Embedded MRAM (eSRAM)

Embedded S-MRAM (eSRAM) technology is analogous to embedded SRAM technology which is widely used in SoCs. However, eSRAM is more area and power efficient due to its 2T transistor design vs. SRAM's 6T transistor design. eSRAM requires standard CMOS manufacturing processes with two additional masks on top of any metal layer (preferably layers 1-4). As an added advantage, eSRAM is also non-volatile with infinite endurance (10<sup>16</sup> write cycles). eSRAM is a highly reliable and fast non-volatile memory, is rapidly becoming the embedded memory choice in SoCs replacing embedded SRAM with an embedded S-MRAM memory macro.

#### Table 1: Technology Comparison

	Embedded SRAM	eSRAM
Non-Volatility	N/A	V
Write Performance	٧	V
Read Performance	V	V
Endurance	V	V
Power	-	V
Cost per Memory Bit	-	V

## **Executive Summary**

eSRAM is a magneto-resistive random-access memory (MRAM) macro ranging in density from 8Mbit to 64Mbit organized in words (word: 32 bits). The eSRAM offers AMBA AHB-Lite compatible interface operating up to a maximum of 400MHz.

eSRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. The eSRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance, high performance and a scalable memory technology.

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#### eMRAM Use Model

Figure 1 shows a typical SoC with integrated eSRAM macro.





#### Features

- Interface: AMBA 3 AHB-Lite Protocol
- Technology: 28nm MRAM
- Density: 8Mbit 64Mbit
- Operating Voltage Range: VCC: 0.80V 1.05V, 1.65V 2.0V
- Operating Temperature Range (Junction Temperature): -40°C to 150°C
- Maximum Clock Speed: 400MHz (maximum)
- Read Latency: 4 Clock Cycles (maximum)
- Write latency: 8 Clock Cycles (maximum)

Revision: A

Avalanche Technology



- Low Power (hibernate Mode): Leakage 100nA (typical) •
- Endurance: 1x10<sup>16</sup> Write Cycles •
- Retention: 10 years •

#### Area

#### Table 2: Macro Area

Density	X Dimension (um)	Y Dimension (um)	Size (mm²)
64Mbit	2,116.08	3,282.16	2.64
32Mbit	2,298.08	1,703.63	1.98
16Mbit	2,296.08	914.36	1.45
8Mbit	1,328.04	914.36	1.10
4Mbit	857.52	914.36	0.89

## Performance

#### *Table 3: Performance Requirements*

Device Operation	Values	Units
Read (Word: 32 bits)	10.0	ns
Write (Word: 32 bits)	20.0	ns
Standby	25.0	μΑ
Hibernate Power Mode	100.0	nA
Read (Word: 32 bits)	2.0	mA
Write (Word: 32 bits)	10.0	mA



## What's Available in the Market

eSRAM, as mentioned above, will replace embedded SRAM in SoCs. Important parameters to compare are performance in terms of maximum frequency and how many wait states (extra clock cycles) the memory module requires at maximum frequency. Table 4 provides a comparison of eSRAM with widely available SRAM memories embedded in ARM based SoCs from ST Micro (ST), Texas Instruments (TI), Microchip, NXP and Freescale.

Company Name	Product Family (Series)	Main CPU	Operational Frequency (Max)	Embedded SRAM	Performance (States/MHz)
Microchip	SAM9	ARM Cortex M4	400MHz	16KB	No wait states up to 400MHz
ТІ	TMS320	32-bit Processor	200MHz	164KB	No wait states up to 120MHz
NXP	Kinetis K Series	ARM Cortex M4	150MHz	256KB	No wait states up to 150MHz
Avalanche	eSRAM	N/A	400MHz	8Mb-64Mb	4 wait states 400MHz

#### Table 4: High level Embedded Non-Volatile Memory Requirements



## **Application Space**

**Microcontrollers:** A microcontroller unit (MCU) is a small computer on a single integrated circuit that typically contains a central processing unit (CPU) core, static random-access memory (SRAM) modules, embedded flash memory modules, a system integration module and peripheral modules including a timer, an analog-to-digital converter (ADC), serial communication and networking. Microcontrollers with embedded SRAM memories are widely used as scratch pad memories in real-time control applications.

eSRAM is a scalable, high-performance and power-efficient embedded memory technology. eSRAM is intended to be part of a MCU's Memory sub-system where it can deliver data storage requirements. Although embedded SRAM is used for temporary storage (scratch pad), eSRAM can not only replace embedded SRAM to store temporary data but can also store code for an efficient small-system solution; eSRAM has very high data endurance and data retention limits.



## Marketing Positioning

The major advantages of eSRAM are as follows:

**High-performance:** eSRAM supports a 32-bit AMBA 3 AHB-Lite interface operating at 400MHz with 4 wait states. This translates into 32-bits of data every 10ns; 400MB/s sustained throughput is achieved.

**Low Power:** Low power mode is required in MCUs running real-time adaptive control applications. Most MCUs spend much of their time in lowered-power states where they are either running from a lowered frequency clock or are in a state where the CPU is suspended with peripherals operating or in a state where all operations are ceased awaiting a resume command based on certain user-selected input; typically, an interrupt or a timer event. eSRAM macro supports a low power mode (hibernate) where the macro's leakage current is 100nA or less. The wakeup time from hibernate mode is rapid; less than 300ns.



## Signal Description and Assignment



Table 5: Signal Description

Signal	Туре	Description
HSEL	Input	eSRAM SELECTOR: Enables or disables the eSRAM macro.
HCLK	Input	<b>eSRAM Clock Source:</b> The bus clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Input	<b>eSRAM Reset Controller:</b> The bus reset signal is active LOW and resets the eSRAM IP and brings it into Standby state.
HADDR[31:0]	Input	eSRAM Address Bus: The 32-bit address bus.
HWRITE	Input	<b>eSRAM Read / Write enable:</b> Indicates the transfer direction. When HIGH this signal indicates a write transfer and when LOW a read transfer. It has the same timing as the address signals, however, it must remain constant throughout a burst transfer.
HWDATA[31:0]	Input	<b>eSRAM Write Data Bus:</b> The write data bus transfers data from the master to the eSRAM during write operations. The data bus width is 32 bits.
HREADY	Output	<b>eSRAM Ready/Busy:</b> When HIGH, the HREADY signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRDATA[31:0]	Output	<b>eSRAM Read Data Bus:</b> During read operations, the read data bus transfers data from the eSRAM to the master. The data bus width is 32 bits.
Vcc	Supply	Vcc: eSRAM macro power supply.
Vss	Supply	Vss: eSRAM macro ground supply.



## Macro Architecture

The eSRAM macro's internal architecture is shown in Figure 3:





As can be seen, each eSRAM's memory array (irrespective of density) is organized in a group of 8 planes. The example shown depicts an 8Mbit implementation where each plane consists of 1Mbit MRAM cells. Having this architecture allows every access (reads/write) to generate 256 bits of data maximizing throughput. These 256 bits of data are then multiplexed to 32-bit outputs/inputs based on the address provided.

#### Read

The 8-plane architecture maximizes throughput for sequential reads. After providing the initial address followed by a 4-cycle latency, sequential data can be output at full clock frequency (400MHz) without incurring any further inter-address latencies. On the other hand, if random reads are required, each new address will incur a 4-cycles latency.

#### Write

Again, the 8-plane architecture maximizes throughput for sequential writes. The eSRAM macro accepts up to a maximum of 256 bits (8 sequential address) for each write followed by a 1-cycle latency. If less bits are provided (multiples of 32 bits), the latency varies (1-8 cycles). Table 6 provides the latencies for different data lengths.



### Table 6: Write Latency Table

#	# of Write Bits (Multiples of 32-bits)	Latency Incurred
1	32	8
2	64	7
3	96	6
4	128	5
5	160	4
6	192	3
7	224	2
8	256	1



## Bus Interface

As mentioned above, eSRAM supports the AMBA 3 AHB-Lite protocol for read and write operations. Each AHB-Lite transfer consists of two phases:

- 1. Address Phase: Address phase generally lasts for a single HCLK cycle unless extended by the previous bus transfer.
- 2. **Data Phase**: Data phase can require several HCLK cycles. eSRAM uses HREADY signal to control the number of clock cycles required to complete the transfer.

**HWRITE** controls the direction of data transfer to or from the master. It is based on the following:

- HWRITE HIGH (Logic '1') indicates a write transfer and the master transfers data on the write data bus, HWDATA[31:0]
- HWRITE LOW (Logic '0') indicates a read transfer and the eSRAM generates the data on the read data bus, HRDATA[31:0].

#### Write Transfer

During a Write transfer, the master drives the address and control signals onto the bus. eSRAM then samples the address and control information on the rising edge of HCLK. After eSRAM has sampled the address and control, the master can start to drive the data on the data bus HWDATA[31:0]. In response, eSRAM can drive the HREADY which the master samples on the rising edge of HCLK.



## Figure 4: Write Transfer



Avalanche Technology Page 12 | 17



#### Read Transfer

During a Read transfer, the master drives the address and control signals onto the bus. eSRAM then samples the address and control information on the rising edge of HCLK. After eSRAM has sampled the address and control, it can start to drive the data on the data bus HRDATA[31:0]. In response, eSRAM can drive the HREADY which the master samples on the rising edge of HCLK; HREADY is used during latency cycles.



# Don't Care Address C Dataout A Address B $\widehat{\wedge}$ ¥ Address A HWRITE HCLK HREADY HRDATA[31:0] HADDR[31:0] HWDATA[31:0]

## Figure 5: Read Transfer





Figure 6: Read Transfer – Sequential

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## **Electrical Specifications**

## Table 7: Recommended Operating Conditions

Parameter / Condition	Minimum	Maximum	Units
Operating Temperature	-40.0	150.0	°C
V <sub>cc</sub> Supply Voltage	0.8	1.05	V
V <sub>SS</sub> Supply Voltage	0.0	0.0	V

## Table 8: AC Timing Characteristics

#	Category	Parameter	Description	Minimum	Maximum	Units
1		fhclk	Frequency		400.00	MHz
2		thclk	Period	5.00		ns
3	Cleak	tнськн	Clock High	0.48	0.52	<b>t</b> HCLK
4	CIOCK	<b>t</b> HCLKL	Clock Low	0.48	0.52	<b>t</b> HCLK
5		<b>t</b> JITPER	Clock Period Jitter	-90.00	90.00	ps
6		tлтсс	Clock Cycle to Cycle Jitter		180.00	ps
7	Write Data (Innut)	<b>t</b> hwdatas	Data Setup Time	325.00		ps
8	White Data (Input)	<b>t</b> hwdatah	Data Hold Time	325.00		ps
9	Address	thaddrs	Address Setup Time	325.00		ps
10	Address	<b>t</b> haddrh	Address Hold Time	325.00		ps
11	Command	tcmds	Command Setup Time	325.00		ps
12	(HSEL, HWRITE, HBURST)	tсмdн	Command Hold Time	325.00		ps
13	Read Data (Output)	<b>t</b> hrdata	Data Output Access Time	2.50		ns
14	Ready / Busy	thready	Device Ready Signal		325.00	ps



## **Revision History**

Revision	Date	Change Summary
REV A	09/15/2018	Initial release Added latency for write Added eSRAM macro architecture