Migration from Fujitsu MB85RS4MT to Avalanche AS1004204 Application Note

AN000011 details the feature differences when migrating from the Fujitsu MB85RS4MT serial FRAM to Avalanche AS1004204 high-performance Persistent SRAM (P-SRAM).

1. Introduction

AS1004204 is a high-performance 4-Mbit serial spin-transfer torque magneto-resistive random-access memory (STT-MRAM). MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with unlimited endurance and greater than 20-year retention.

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

AS1004204 has a Serial Peripheral Interface (SPI) compatible bus interface supporting eXecute-In-Place (XIP) functionality, and hardware/software based data protection mechanisms.

This application note provides a comparison of features that need to be taken into consideration when migrating from the Fujitsu MB85RS4MT FRAM to the Avalanche AS1004204 MRAM.

2. Feature Comparison

The AS1004204 is a feature-rich memory device supporting x1, x2 and x4 SPI interface operating at up to 108MHz SDR or 54MHz DDR. In contrast, the Fujitsu MB85RS4MT only supports single I/O operation at a maximum frequency of 40 MHz SDR. As a result, the Avalanche AS1004204 offers higher performance, functionality, endurance and data retention compared with the Fujitsu device.

In addition to the 8-pin SOIC, the AS1004204 is also available in 8-pad WSON and 24-Ball FBGA packages. These packages are compatible with similar low-power volatile and non-volatile products.

Table 1 provides a feature comparison between the MB85RS4MT and the AS1004204.

Table 1: Feature Comparison

Feature		Fujitsu MB85RS4MT	Avalanche AS1004204
Family		Serial	High Performance
Technology		FRAM	STT-MRAM
Density		4Mbit	4Mbit
Voltage - V_{CC}		1.8V to 3.6V	1.71 to 2.00V[1]
Interface		SPI	SPI
Bus Width		x1	x1, x2, x4
Mode		0,3	0,3
Frequency (MHz max)		40 (SDR)	108 (SDR) 54 (DDR)
Endurance		10^{13}	10^{16}
Data Retention (yrs)		10	>20
Temperature Range	-40°C to +85°C	✓	✓
	-40°C to +105°C		✓
Package	8-SOIC		✓
	8-WSON	✓	✓
	24-BGA		✓

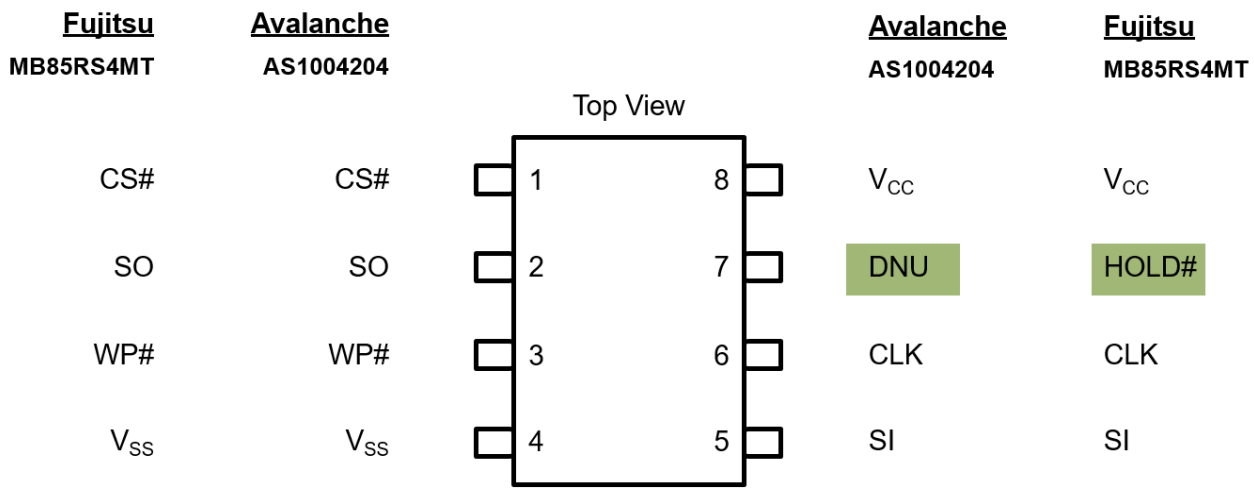
1. The Avalanche AS3004204 supports 2.70V to 3.60V.

3. 8-Pin SOIC Pinout Comparison

The Avalanche AS1004204 is offered in three industry-standard packages: 8-pin SOIC, 8-pad WSON and 24-Ball FBGA.

The 8-pin SOIC has the same footprint as the MB85RS4MT. Figure 1 compares the SOIC pinouts of the AS1004204 to the MB85RS4MT.

Figure 1: 8-pin SOIC Pinout Comparison



In the Avalanche default setting, x1 SPI Mode, the pinout of the AS1004204 is the same as the MB85RS4MT. Fujitsu supports the HOLD# pin which is a legacy feature not commonly used. For the AS1004204, it is recommended to tie Pin 7 to V_{CC} (do not leave pin floating).

Figure 2: SOIC Dimension Comparison

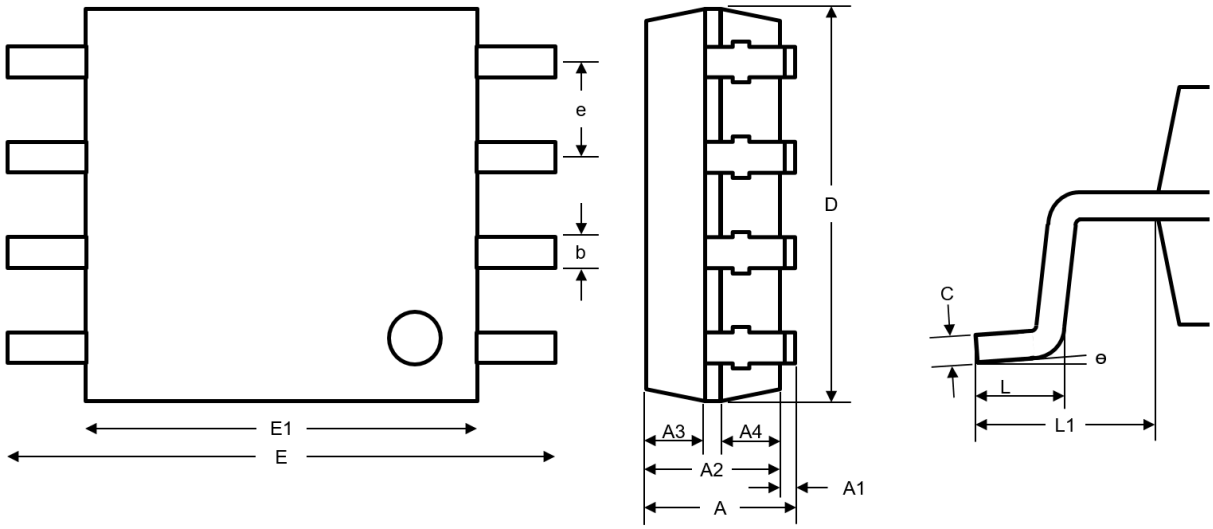


Table 2 lists the differences in dimensions of the SOIC packages.

Table 2: SOIC Package Dimensions (Typical Values)

Package	A	A1	A2	A3	A4	D	E	E1	b	e	L	L1	C	ɵ
Avalanche	2.16 (max)	0.15	1.80	0.798	0.798	5.23	7.90	5.28	0.41	1.27 BSC	0.65	1.37	0.20	5°
Fujitsu	2.10 (max)	0.10	NL	NL	NL	5.24	7.80	5.30	0.43	1.27 BSC	0.75	1.25	0.20	4°

NL = Not Listed

4. Command (Op Code) Comparison

The AS1004204 supports a superset of the commands supported by the MB85RS4MT. A comparison of the AS1004204 and the MB85RS4MT Op Codes is listed in Table 3.

Table 3: Op Code Comparison

Instruction Name	Op Code		MB85RS4MT	AS1004204	Comment
Write Status Register 1	WRSR1	01h	✓	✓	
Write Data Bytes	WRITE	02h	✓	✓	
Read Data Bytes	READ	03h	✓	✓	
Write Disable	WRDI	04h	✓	✓	
Read Status Register 1	RDSR1	05h	✓	✓	
Write Enable	WREN	06h	✓	✓	
Fast Read	FR	0Bh	✓	✓	
Read Device ID	RDID	9Fh	✓	✓	
Exit Deep-Power Down	EXSLP	ABh	-	✓	Avalanche provides options for user to exit DPD using either command opcode or driving CS# high
Enter Deep-Power Down	ENSLP	B9h	✓	✓	
Fast Write	FWR	DAh	-	✓	Fujitsu does not support this function

5. Read Device ID

Executing command op code 9Fh, Read Device ID, will return 4-bytes of information about the device. The first byte of information returns the Manufacturer's ID for both the AS1004204 (E6h) and the MB85RS4MT (04h). The remaining 3-bytes of information are defined differently for the two devices. The format of the Read Device ID output is listed in Table 4: MB85RS4MT Read ID Output and Table 5: AS1004204 Read ID Output.

Table 4: MB85RS4MT Read ID Output

Manufacturer ID ID[31:24]	Continuation Code ID[23:16]	Product ID (1st Byte)		Product ID (2nd Byte)
		Proprietary Use ID[15:13]	Density ID[12:8]	Proprietary Use ID[7:0]
0000 0100	0111 1111	010	01001 – 4Mb	0000 0011
04h	7Fh	49h		03h

Table 5: AS1004204 Read ID Output

Manufacturer ID ID[31:24]	Device Configuration				
	Interface ID[23:20]	Voltage ID[19:16]	Temp ID[15:12]	Density ID[11:8]	Frequency ID[7:0]
1110 0110	0000 – HP QSPI	0010 – 1.8V	0000 - -40ºC- 85ºC 0001 - -40ºC- 105ºC	0010 - 4Mb	0001 - 108MHz 0010 – 54MHz
E6h	00h	02h	00h or 01h	02h	01h or 02h

6. Registers

The AS1004204 provides a superset of registers to access features not supported by the MB85RS4MT. A comparison of the AS1004204 and the MB85RS4MT registers is listed in Table 6

Table 6: Register Comparison

Register Name	MB85RS4MT	AS1004204[1]	Comment
Status Register	✓	✓	
Configuration Register 1	-	✓	Fujitsu does not support this register
Configuration Register 2	-	✓	Fujitsu does not support this register
Configuration Register 3	-	✓	Fujitsu does not support this register
Configuration Register 4	-	✓	Fujitsu does not support this register
Augmented Storage Protection Register	-	✓	Fujitsu does not support this register
Device Identification Register	-	✓	Fujitsu does not support this register
Serial Number Register	-	✓	Fujitsu does not support this register
Unique Identification Register	-	✓	Fujitsu does not support this register

1. All registers need to be re-initialized after a solder reflow process. Refer to application note AN000008 for the detailed description.

The Status Register functions for the AS1004204 and the MB85RS4MT are the same for bits SR[0], SR[1], SR[2], SR[3] and SR[7]. The AS1004204 uses SR[4]-SR[6] to provide additional features not supported by the MB85RS4MT. Table 7 lists the Status Register bit definition for the AS1004204 and MB85RS4MT.

Note: The AS1004204 additional features are set after the device has boot-up. The default state of the status registers are same for both the AS1004204 and MB85RS4MT. See *Table 8: Status Register – Default State Comparison*.

Table 7: Status Register – Bit Definition Comparison

Bits	MB85RS4MT	AS1004204	Comment
SR[7]	WPEN	WP#EN	Hardware based WP# Protection Enable/Disable. 1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low **Functionally the same**.
SR[6]	-	SNPEN	Serial Number Protection Enable/Disable 1: S/N Write protected - protection enabled 0: S/N Writable - protection disabled **Note: Not supported by Fujitsu**
SR[5]	-	TBSEL	Software Top/Bottom Memory Array Protection Selection. 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range) **Note: Fujitsu only supports Top Block.**
SR[4]	-	BPSEL[2]	High order Block Protection Bit provides additional memory array protection areas. **Note: Not supported by Fujitsu. Refer to 6. Block Protection Configuration for more detail.**
SR[3]	BP1	BPSEL[1]	Block Protection Bits
SR[2]	BP0	BPSEL[0]	Block Protection Bits
SR[1]	WEL	WREN	Write Operation Protection Enable/Disable. 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled **Functionally the same.**
SR[0]	0	RSVD	'Reserved for future use' on Avalanche**.** **Functionally the same.**

The Status Register default setting on boot is 00H for the AS1004204. The default setting is not listed in the MB85RS4MT datasheet, but is assumed that the device is shipped unprotected. This means that both parts are initiated in the same state with Top Protection selected and write protection disabled for the Status Register and the memory array. The Serial Number write protection feature SR[6] is not a concern as the Serial Number feature is not supported on the MB85RS4MT (e.g. do not care).

Table 8: Status Register – Default State Comparison

Bits	MB85RS4MT	AS1004204	Comment
SR[7]	0[1]	0	Fujitsu: Protection Disabled – Doesn't write protect when WP# is Low Avalanche: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	-	0	Fujitsu: Function not supported Avalanche: S/N Writable - protection disabled
SR[5]	-	0	Fujitsu: Only Supports Top Protection Avalanche: Top Protection Enabled (Higher Address Range)
SR[4]	-	0	Fujitsu: All Blocks Unprotected Avalanche: All Blocks Unprotected
SR[3]	0[1]	0	
SR[2]	0[1]	0	
SR[1]	0[1]	0	Fujitsu: Write Operation Protection Enabled Avalanche: Write Operation Protection Enabled
SR[0]	0	0	Fujitsu: N/A Avalanche: N/A

1. Value not listed in Fujitsu datasheet, but assumed to be '0' or in the unprotected state.

7. Block Protection Configuration

The AS1004204 provides four additional sizes for protecting the memory array in comparison to the MB85RS4MT. To support this, the AS1004204 uses an extra bit in the Status Register SR[4] as BLSEL[2] as the high-order Block Protection Bit. BPSEL[2] on the Avalanche device must be set appropriately to match the Fujitsu configuration. Table 9 compares the Block Protection for the AS1004204 and the MB85RS4MT.

Table 9: Block Protection Comparison

Block	MB85RS4MT		AS1004204		
Protected	BP1	BP0	BPSEL[2]	BPSEL[1]	BPSEL[0]
None	0	0	0	0	0
Upper 1/64	Not Supported		0	0	1
Upper 1/32	Not Supported		0	1	0
Upper 1/16	Not Supported		0	1	1
Upper 1/8	Not Supported		1	0	0
Upper 1/4	0	1	1	0	1
Upper 1/2	1	0	1	1	0
All	1	1	1	1	1

8. DC Parameters

Table 10 compares the DC Parameters for the MB85RS4MT and AS1004204. For most parameters the Avalanche AS1004204 provides an advantage over the MB85RS4MT.

Table 10: DC Parameter Comparison

Parameter	Symbol	MB85RS4MT	AS1004204	Comments
Supply Voltage	V_{CC}	1.8V to 3.6V	1.71V to 2.00V[1]	
Read Current (1-1-1) SDR[1]	I_{READ1}	1.8 mA @40MHz	7 mA @54MHz	Avalanche has higher read current operating at a faster clock rate
Write Current (1-1-1) SDR[1]	I_{WRITE1}	1.8 mA @40MHz	10 mA @54MHz	Avalanche has higher write current operating at a faster clock rate
Standby Current[1]	I_{SB}	10 µA	120 µA	Avalanche has higher standby current
Deep Power Down[1]	I_{DPD}	5 µA	1 µA	Avalanche has lower current consumption
Input High Voltage	V_{IH}	0.7xV_{CC} to V_{CC}+0.5	0.7xV_{CC} to V_{CC}+0.3	
Input Low Voltage	V_{IL}	-0.5V to 0.3xV_{CC}	-0.3V to 0.3xV_{CC}	Voltage swings cannot go below V_{IL} (min) of -0.3V for Avalanche
Output High Voltage Level	V_{OH}	V_{CC}-0.5V (min) I_{OH}= -2 mA	V_{CC}-0.2V (min) I_{OH}=-100 µA 1.5V (min) I_{OH} = -1 mA	No change required. Note: V_{OH} must remain within logic levels for inputs on heavily loaded system buses
Output Low Voltage Level	V_{OL}	0.4V (max) I_{OL} = 2 mA;	0.2V (max), I_{OL}=150 µA 0.4V (max) I_{OL} = 2 mA;	No change required. Note: V_{OL} must remain within logic levels for inputs on heavily loaded system buses

1. The Avalanche AS3004204 supports 2.70V to 3.60V.

9. AC Parameters

Table 11 compares selected AC Parameters for the MB85RS4MT and AS1004204. The Avalanche AS1004204 provides equivalent or better timing than the MB85RS4MT.

Table 11: AC Parameter Comparison

Parameter	Symbol	MB85RS4MT	AS1004204	Comments
Deep Power Down Entry Time	t_{EDPD}	Not Listed	3 µs (min)	
Deep Power Down Exit Time	t_{EXDPD}	400 µs (max)	400 µs (min)	Fujitsu device is available within 400 µs while the Avalanche device is available after 400 µs.
Output Disable Time (w.r.t. CS#)	t_{HZCS}	12 ns (max)	7.0 ns (max)	Avalanche device ensures the bus is available after 7ns while the Fujitsu device releases the output after 12ns.

9. Power-Up and Power-Down Behavior

Figure 3 and Figure 4 depict the Power-Up and Power-Down behavior.

Figure 3: Power-Up Behavior

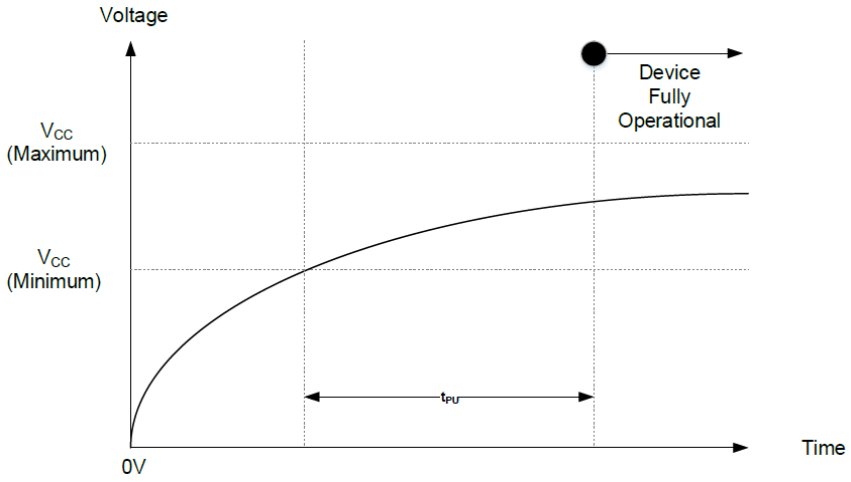


Figure 4: Power-Down Behavior

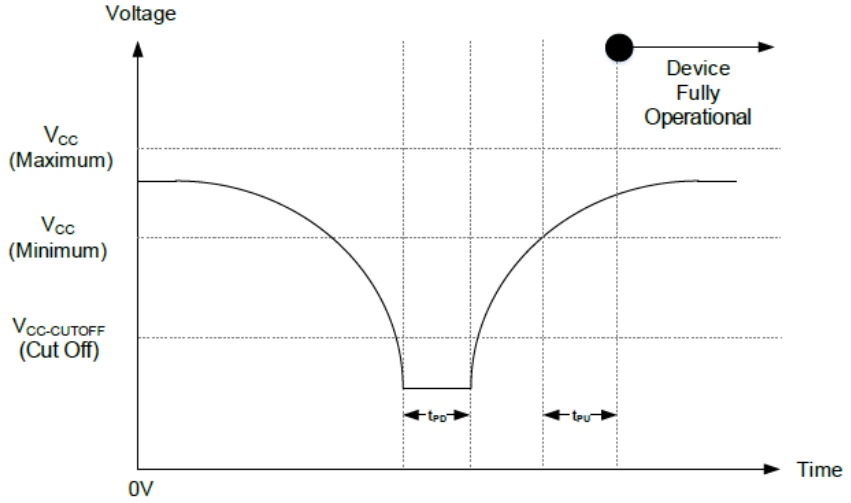


Table 12: Power-Up and Power-Down Comparison

Parameter	Symbol	MB85RS4MT	AS1004204	Comment
V_{CC} Power Up to First Instruction	t_{PU}	250 µs (min)	250 µs (min)	
V_{CC} Ramp Up Time	R_{VR}	50 µs/V (min)	30 µs/V (min)	Avalanche device permits a slower ramp-up time
V_{CC} Ramp Down Time	R_{VF}	100 µs/V (min)	20 µs/V (min)	Avalanche device permits a slower ramp-down

10. Summary

The features of the AS1004204 provide system designers a straightforward migration path from the MB85RS4MT while also providing higher in-system performance for read and write operations with lower power consumption.

11. Revision History

Revision	Date	Change Summary
REV A	11/22/2019	Initial release