Space-Grade Dual QSPI Persistent SRAM Memory

(AS3064204, AS3128208)

Features

- Interface
  - Dual Quad SPI – support 8-bit wide transfer
    - Dual QPI (4-4-4) – up to 100MHz SDR
    - Dual QPI (4-4-4) – up to 50MHz DDR
- Density
  - 64Mb, 128Mb
- Voltage Range
  - V_{CC}: 2.50V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.3V
- Temperature Range
  - Operating: -40°C to 125°C
- Technology
  - 22 nm pMTJ STT-MRAM
    - Data Endurance: 10^{16} write cycles
    - Data Retention: 20 years @ 85°C
- Packages
  - 56-ball FBGA (10mm x 10mm)
- Data Protection
  - Hardware Based
    - Dedicated Hardware Signals (HBP0, HBP1, HBP2) in conjunction with Top/Bottom Select Signal (HTBSEL)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Qualification
  - JESD47H.01
  - 48-hour burn-in at 125°C
- RoHS & REACH Compliant *

* Leaded Balls available

Please contact sales for information about the Safe Operating Area of these devices under radiation

Table of Contents

General Description

AS3xxxx204/8 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 64Mbit to 128Mbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

Table 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually infinite endurance and retention, and scalable non-volatile memory technology.

AS3xxxx204 has a Single QSPI Interface, while AS3xxxx208 has a Dual QSPI Interface. SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

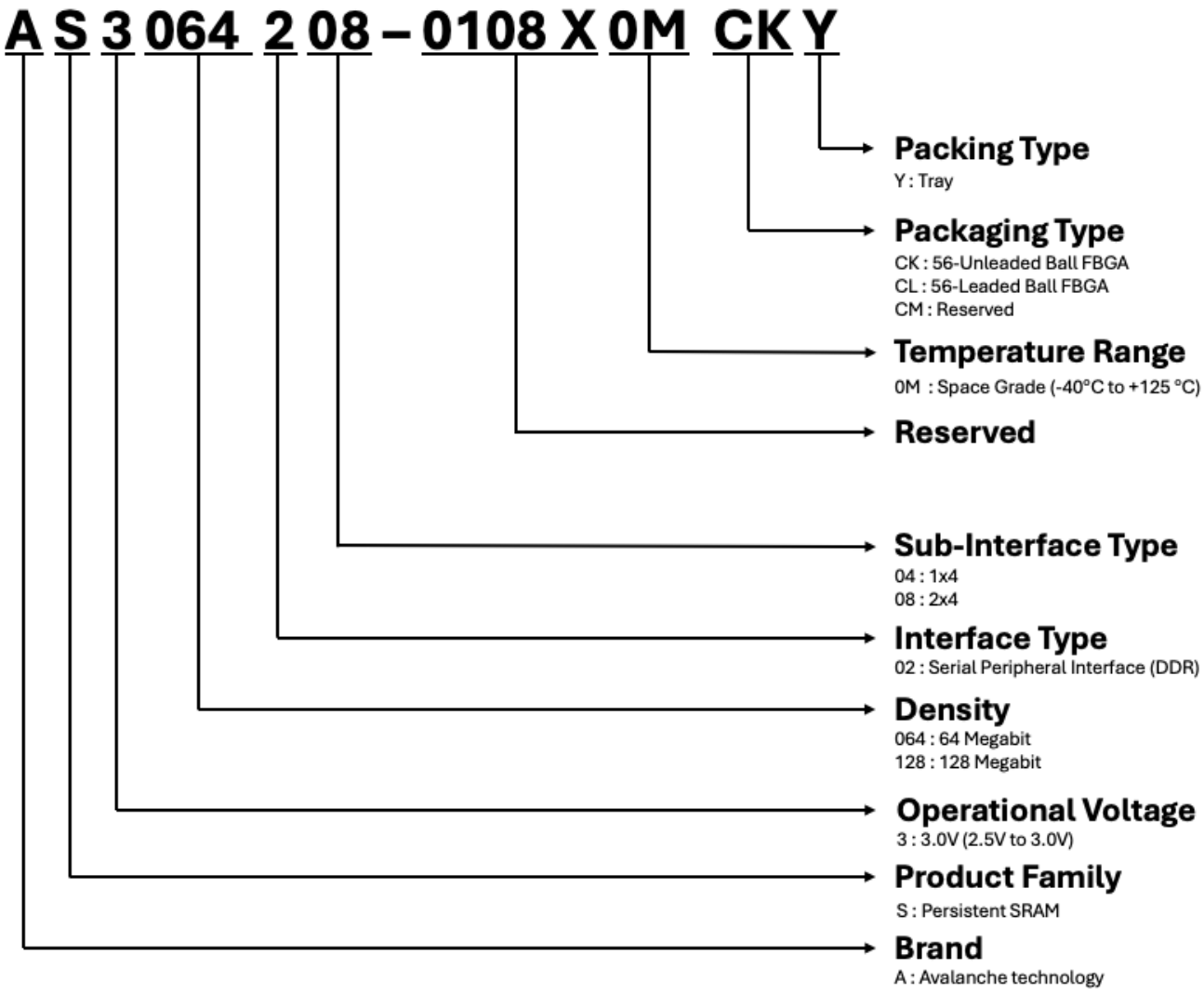
AS3xxxx204/8 is available in small footprint 56-Ball FBGA package. The ball assignment is compatible with our 96/224-Ball FBGA packages and allows an upgrade path to higher densities. Board designers are encouraged to allow a keep out zone if they wish to allow an upgrade to our higher density family of Dual QSPI devices.

AS3xxxx204/8 is offered with industrial (-40°C to 85°C) and in Space Grade (-40°C to 125°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Ordering Options



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2: Valid Combinations List

Valid Combinations				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS3064204-0108X	0M	CK	Y	AS3064204-0108X0MCKY
AS3128208-0108X	0M	CK	Y	AS3128208-0108X0MCKY
AS3064204-0108X	0M	CL	Y	AS3064204-0108X0MCLY
AS3128208-0108X	0M	CL	Y	AS3128208-0108X0MCLY

Marking Specification — Standard

The device will be marked according to the following specification:

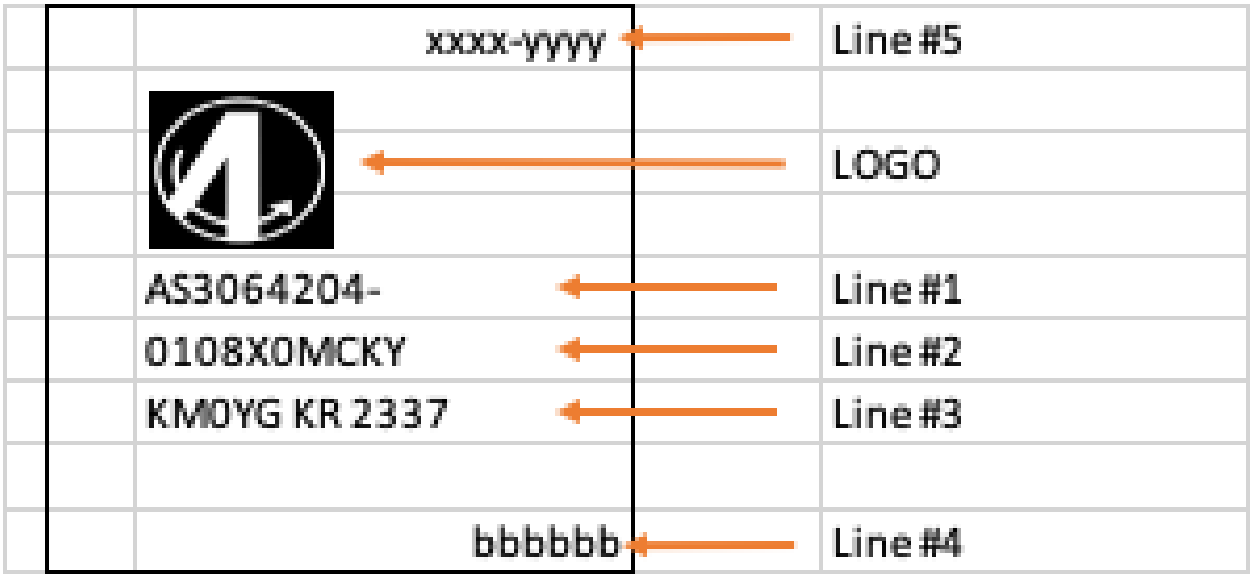
Line #1 & Line #2 will match the part number in Table 2

Line #3 Will show: 5 digit Alphanumeric Code + Country of Origin + Date Code

Line #4 May or May not be marked. This field is reserved for Avalanche Technology

Line #5 May or May not be marked. This field is reserved for Avalanche Technology

Figure 2: Device Marking



Signal Description and Assignment

Figure 3: Device Pinout

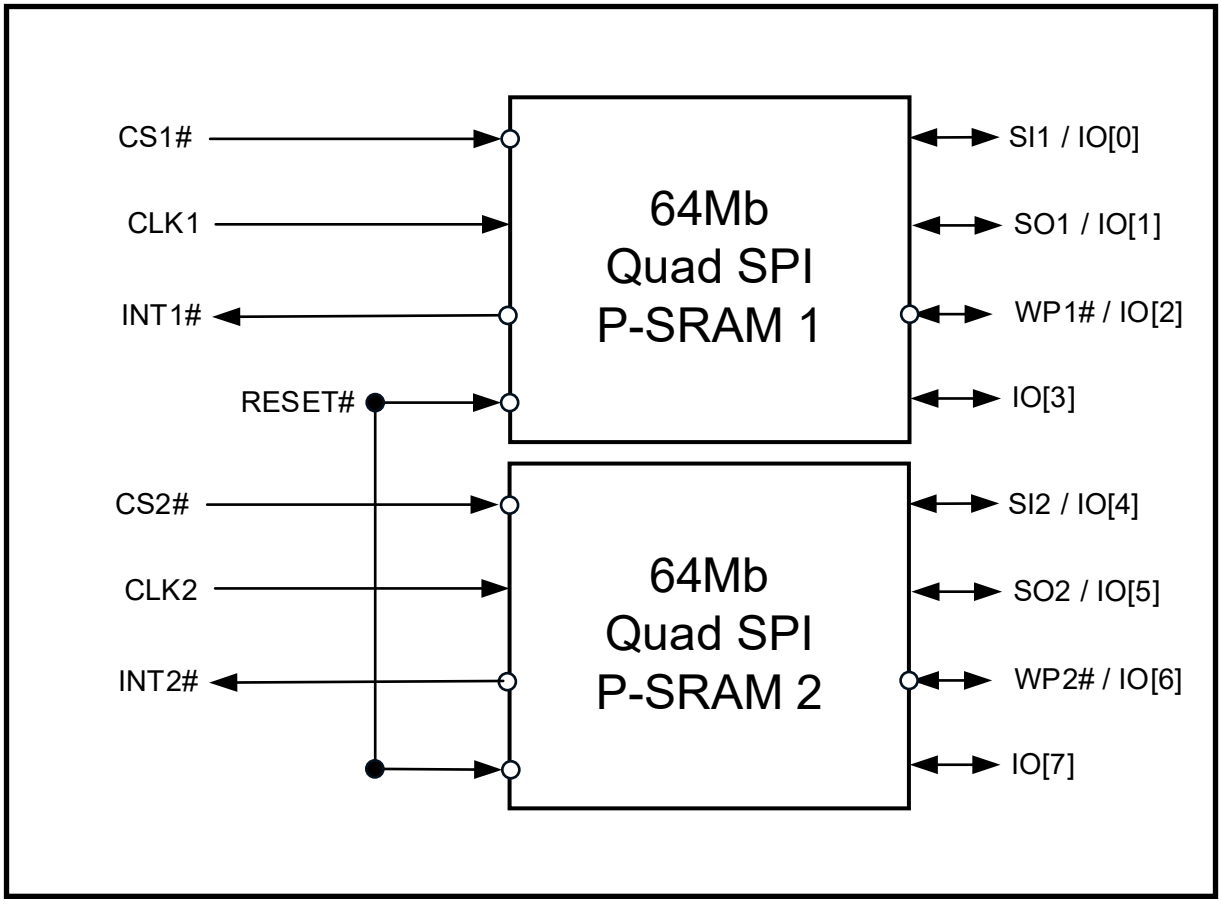


Figure 4: Single QSPI System Block Diagram

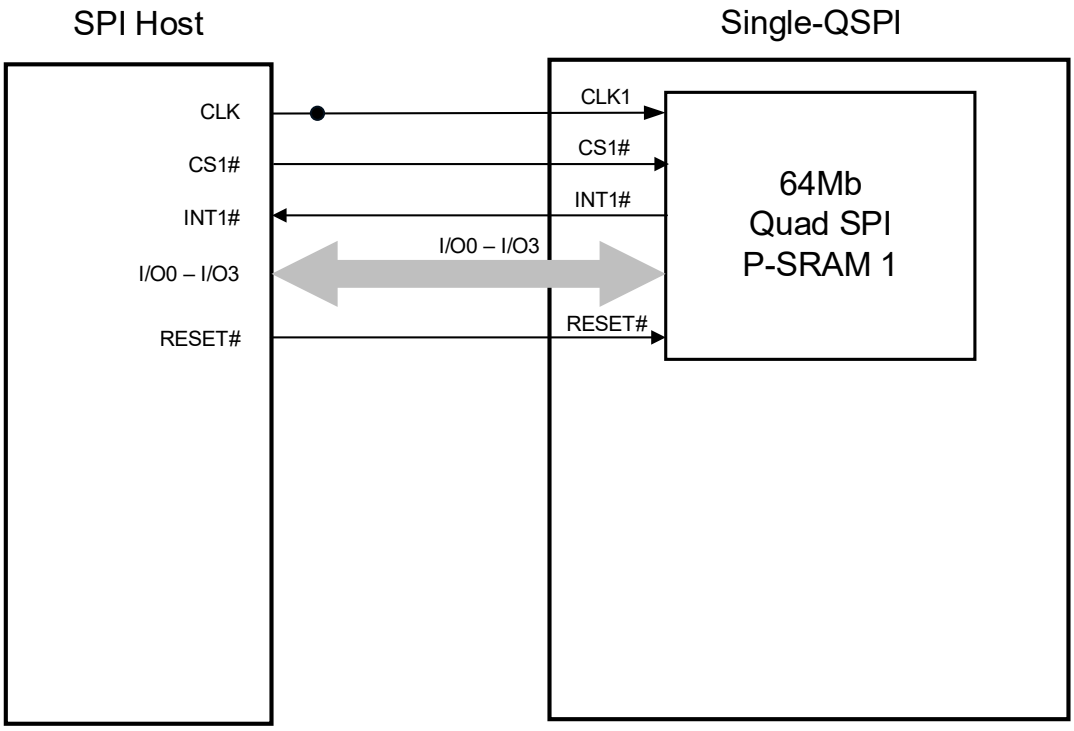


Figure 5: Dual QSPI System Block Diagram

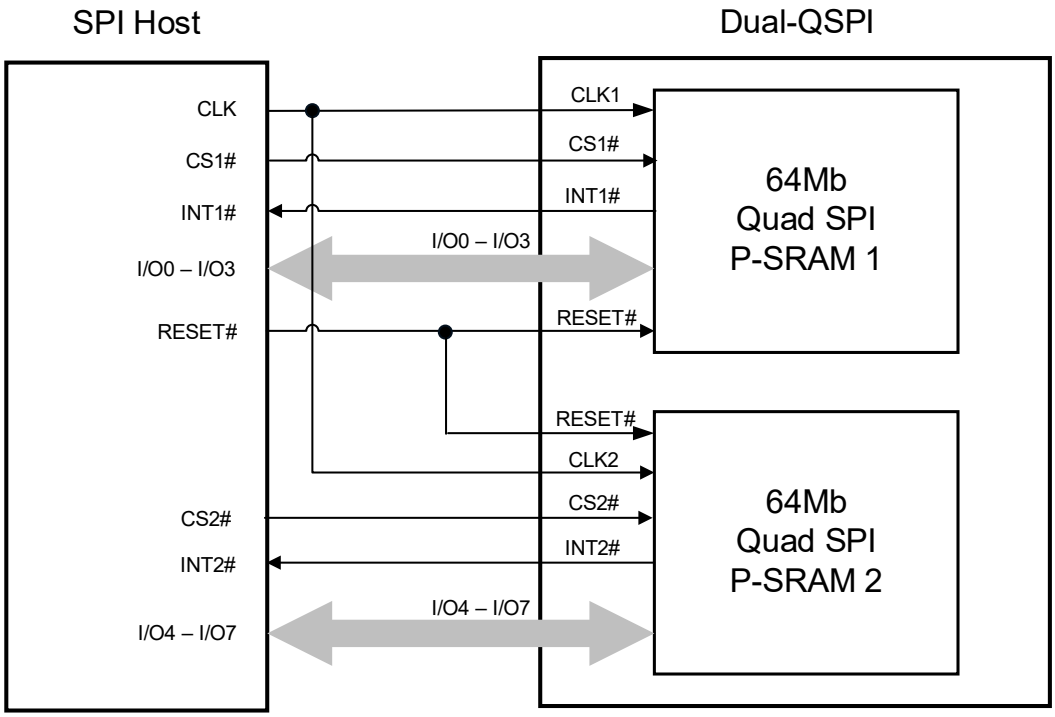


Table 3: 64Mb QSPI AS3064204 Signal Description

Signal		Type	Description
CS1#	E2	Input	**Chip Select 1:** When CS1# is driven High, device 1 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
SI1 / IO[0]	F3	Input / Bidirectional	**Serial Data Input 1 (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode. **Bidirectional Data 0 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
SO1 / IO[1]	F2	Output / Bidirectional	**Serial Data Ooutput 1 (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode. **Bidirectional Data 1 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
WP1# / IO[2]	E4	Input / Bidirectional	**Write Protect 1 (SPI):** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used. **Bidirectional Data 2 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
IO[3]	F4	Bidirectional	**Bidirectional Data 3 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
CLK1	D2	Input	**Clock 1:** Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • ***SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR*** • ***SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only***
INT1#	C5	Output	**Interrupt 1**: Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
RESET#	C4	Input	**RESET**: When this signal is driven high, device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z. This signal resets both devices.
HBP[0:2]	A5, A6, B7	Input	**HPB0, HBP1, HBP2**: these Hardware Block Protect signals, when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions: These balls have a Pull down to Vss. If left disconnected they will be seen by device as “Low”.
HTBSEL	C7	Input	**HTBSEL**: This signal when driven High or Low, is used in conjunction with the Hardware Block Protect Pins (HBP0, HBP1, and HBP2) determines if the write-protected memory area defined by the state of the HBP pins, starts from

Signal		Type	Description
			the top or the bottom of the memory array: This ball have a Pull down to Vss. If left disconnected it will be seen by device as “Low”.
V_{CC}	A2, A4, D4, D6, D7, F7	Supply	Core power supply
V_{CCIO}	A7, B2, B4, C6, F1, F6, G4	Supply	I/O power supply
V_{SS}	A1, A3, A8, B3, E5, E6, E7, G7	Supply	Core ground supply.
V_{SSIO}	B1, B5, B6, E1, G5, G6	Supply	I/O ground supply.
DNU	B8, C1, C2, C3, C8, D1, D3, D5, D8, E3, E8, F5, F8, G1, G2, G3, G8	-	Do Not Use: DNUs must be left unconnected, floating.

Table 4: 128Mb QSPI AS30128208 Signal Description

Signal		Type	Description
CS1#	E2	Input	**Chip Select 1:** When CS1# is driven High, device 1 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
CS2#	C3	Input	**Chip Select 2:** When CS2# is driven High, device 2 will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS2# Low enables device 2, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
SI1 / IO[0]	F3	Input / Bidirectional	**Serial Data Input 1 (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode. **Bidirectional Data 0 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
SI2 / IO[4]	F5	Input / Bidirectional	**Serial Data Input 2 (SPI):** The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode. **Bidirectional Data 4 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad mode.
SO1 / IO[1]	F2	Output / Bidirectional	**Serial Data Ooutput 1 (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode. **Bidirectional Data 1 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
SO2 / IO[5]	G3	Output / Bidirectional	**Serial Data Ooutput 2 (SPI):** The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode. **Bidirectional Data 5 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad mode.
WP1# / IO[2]	E4	Input / Bidirectional	**Write Protect 1 (SPI):** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used. **Bidirectional Data 2 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
WP2# / IO[6]	G2	Input / Bidirectional	**Write Protect 2 (SPI):** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used. **Bidirectional Data 6 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad mode.
IO[3]	F4	Bidirectional	**Bidirectional Data 3 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad mode.
IO[7]	G1	Bidirectional	**Bidirectional Data 7 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad mode.
CLK1	D2	Input	**Clock 1:** Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer.

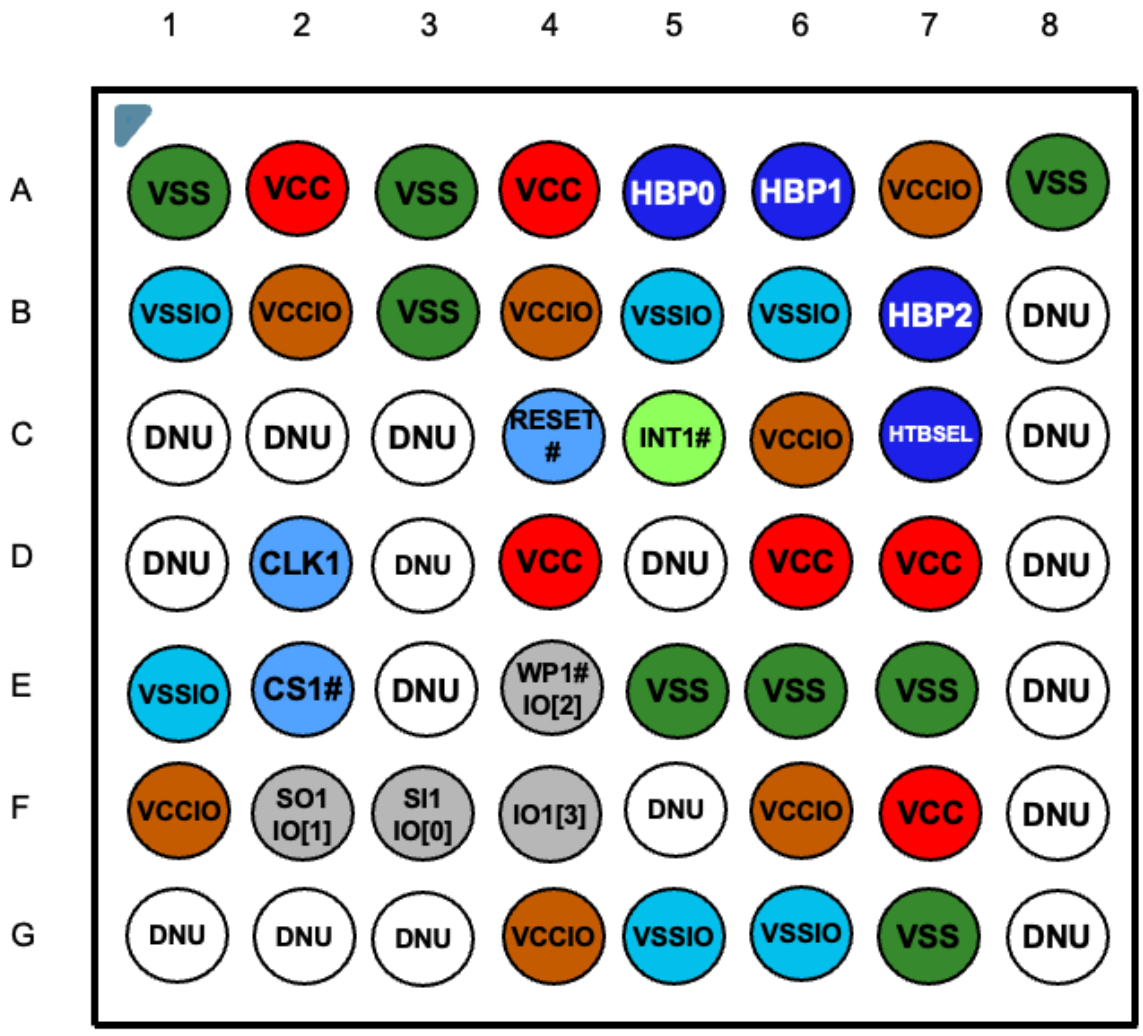
Signal		Type	Description
			In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • ***SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR*** • ***SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only***
CLK2	D1	Input	**Clock 2:** Provides the timing for device 2 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • ***SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR*** • ***SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only***
INT1#	C5	Output	**Interrupt 1**: Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
INT2#	D3	Output	**Interrupt 2**: Output generated by device 2 when an unrecoverable ECC error is detected during read operation (output goes low on error).
RESET#	C4	Input	**RESET**: When this signal is driven high, device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z. This signal resets both devices.
HBP[0:2]	A5, A6, B7	Input	**HPB0, HBP1, HBP2**: these Hardware Block Protect signals, when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions: These balls have a Pull down to Vss. If left disconnected they will be seen by device as “Low”.
HTBSEL	C7	Input	**HTBSEL**: This signal when driven High or Low, is used in conjunction with the Hardware Block Protect Pins (HBP0, HBP1, and HBP2) determines if the write-protected memory area defined by the state of the HBP pins, starts from the top or the bottom of the memory array: This ball have a Pull down to Vss. If left disconnected it will be seen by device as “Low”.
V_{CC}	A2, A4, D4, D6, D7, F7	Supply	Core power supply
V_{CCIO}	A7, B2, B4, C6, F1, F6, G4	Supply	I/O power supply
V_{SS}	A1, A3, A8, B3, E5, E6, E7, G7	Supply	Core ground supply.
V_{SSIO}	B1, B5, B6, E1, G5, G6	Supply	I/O ground supply.
DNU	B8, C1, C2, C8, D5, D8,	-	Do Not Use: DNUs must be left unconnected, floating.

Signal		Type	Description
	E3, E8, F8, G8		

Package Options

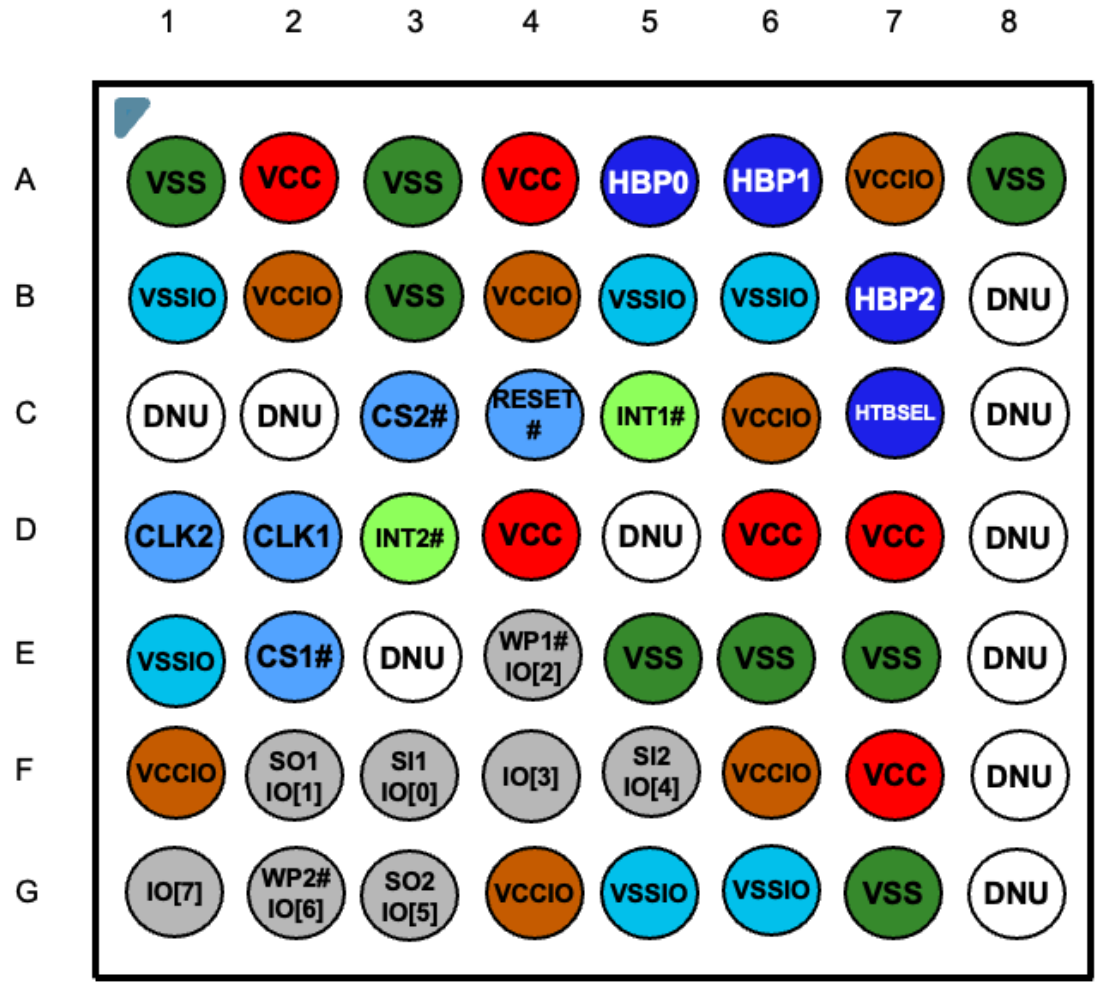
64Mb QSPI, SPI (56-Ball FBGA – Balls Down, Top View)

Figure 6: 56-Ball FBGA



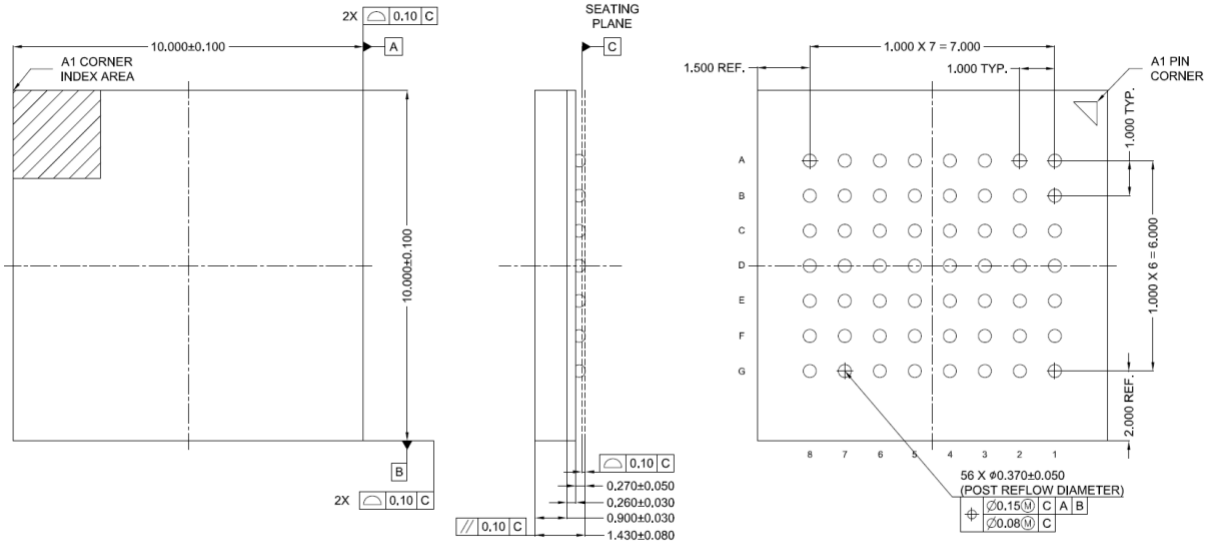
128Mb D-QSPI, SPI (56-Ball FBGA – Balls Down, Top View)

Figure 7: 56-Ball FBGA



Package Drawings

56-Ball FBGA



TOP VIEW SIDE VIEW BOTTOM VIEW

[NOTES]

1a. ROHS SOLDER BALL DIAMETER IS

Diameter: 0.35 mm before reflow; 0.37 (+/-0.05) mm post reflow

Height: 0.27 (+/-0.05) mm

1a. LEADED SOLDER BALL DIAMETER IS

Diameter: 0.37 mm before reflow; 0.385 (+/-0.05) mm post reflow

Height: 0.285 (+/-0.05) mm

2. SOLDER RESIST OPENING IS

0.300 mm

3. Package Height can increase after reballing to Leaded by .015mm

Architecture

AS3xxxx204/8 is a high performance serial STT-MRAM device. It features a SPI-compatible bus interface running in SDR or DDR nodes, eXecute-In-Place (XIP) functionality, and hardware/software-based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

AS3xxxx204/8 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. In Single SPI mode, the device is accessed via the SI / IO[0] pin. In Quad SPI modes, IO[7:0] is used to access the device respectively. ***Table 5 & 6*** summarize all the different interface modes supported and their respective I/O usage. ***Table 7*** shows the clock edge used for each instruction component.

Nomenclature adoption: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O (SI / IO[0] or SO / IO[1]). On the other hand, 4-4-4 represents all command address and data are being sent on four I/Os (IO[3:0]).

Table 5: Interface Modes of Operations – Device 1

Instruction Component	Single SPI (1-1-1)	Quad Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[0]	SI / IO[0]	SI / IO[0]	IO[3:0]
Address	SI / IO[0]	IO[0]	IO[3:0]	IO[3:0]
Data Input	SI / IO[0]	IO[3:0]	IO[3:0]	IO[3:0]
Data Output	SO / IO[1]	IO[3:0]	IO[3:0]	IO[3:0]

Table 6: Interface Modes of Operations – Device 2

Instruction Component	Single SPI (1-1-1)	Quad Output SPI (1-1-4)	Quad I/O SPI (1-4-4)	QPI (4-4-4)
Command	SI / IO[4]	SI / IO[4]	SI / IO[4]	IO[7:4]
Address	SI / IO[4]	IO[4]	IO[7:4]	IO[7:4]
Data Input	SI / IO[4]	IO[7:4]	IO[7:4]	IO[7:4]
Data Output	SO / IO[5]	IO[7:4]	IO[7:4]	IO[7:4]

Table 7: Clock Edge Used for instructions

Instruction Type	Command	Address	Data Input	Data Output
(1-1-1) SDR				1
(1-1-1) DDR				1
(1-4-4) SDR				1
(1-4-4) DDR				1
(4-4-4) SDR				1
(4-4-4) DDR				1

Notes:
R: Rising Clock Edge
F: Falling Clock Edge
1: Data output from AS3xxxx204/8 always begins on the falling edge of the clock

AS3xxxx204/8 supports eXecute-In-Place (XIP) which allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. Thus, XIP mode saves command overhead and reduces random read & write access time. A special XIP byte must be entered after the address bits to enable/disable (Axh/Fxh) XIP.

AS3xxxx204/8 offers both hardware and software-based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the registers and memory array.

AS3xxxx204/8 supports Deep Power Down. Data is not lost while the device is in this low power state. Moreover, the device maintains all its configurations.

Figure 8: Functional Block Diagram – Dual QSPI Device 1

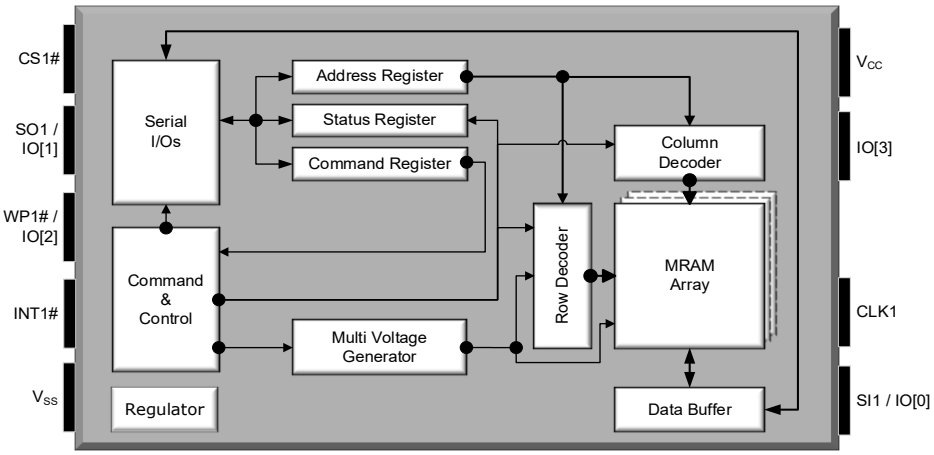


Figure 9: Functional Block Diagram – Dual QSPI Device 2

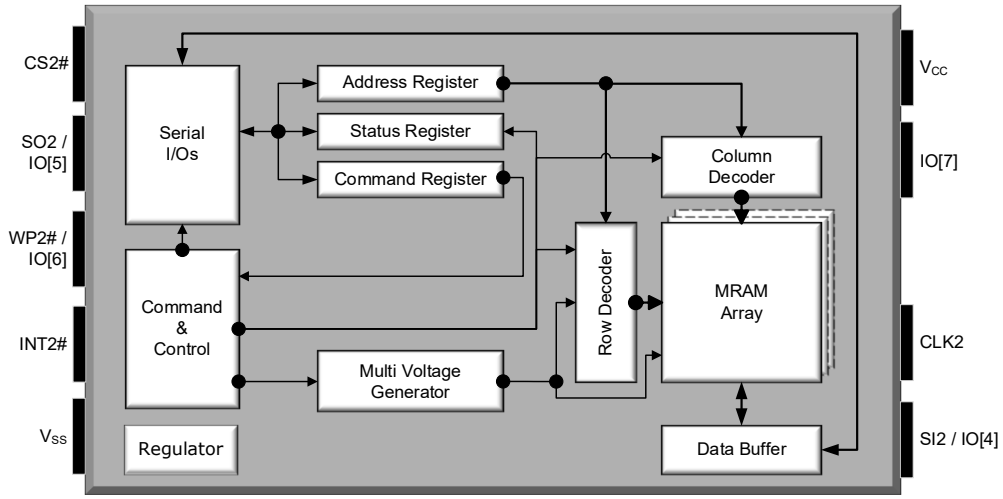


Table 8: Modes of Operation – Device 1

Mode	Current	CS1#	CLK1	SI1 / IO[3:0]	SO1 / IO[3:0]
Standby	I_{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I_{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I_{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z

Notes:
H: High (Logic '1')
L: Low (Logic '0')
Hi-Z: High Impedance

Table 9: Modes of Operation – Device 2

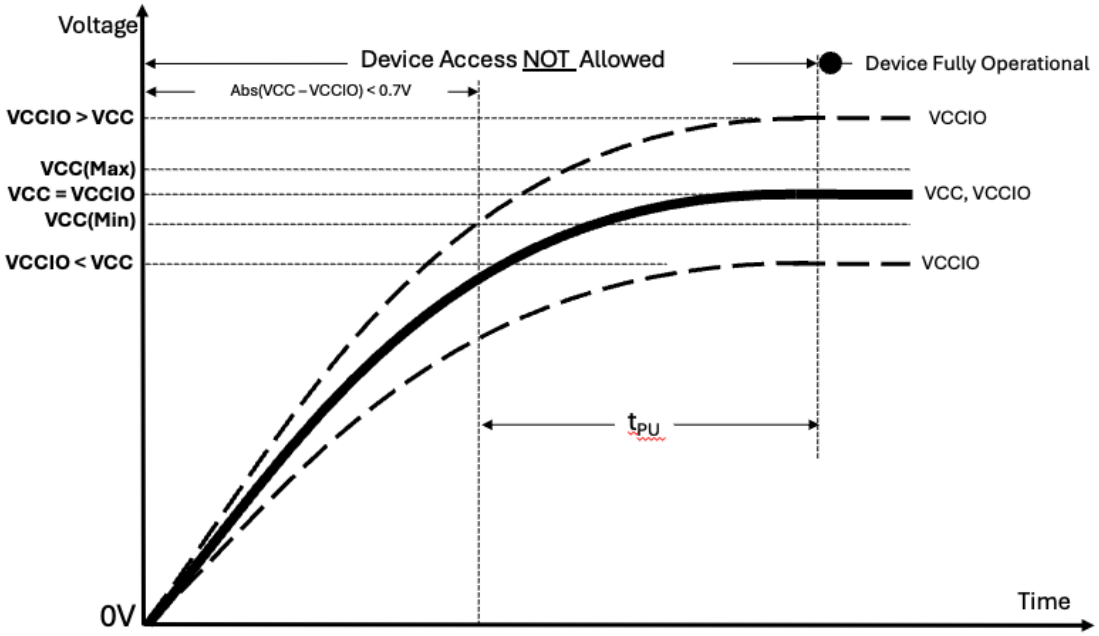
Mode	Current	CS2#	CLK2	SI2 / IO[7:4]	SO2 / IO[7:4]
Standby	I_{SB}	H	Gated	Gated / Hi-Z	Hi-Z / Hi-Z
Active - Read	I_{READ}	L	Toggle	Command, Address	Data Output
Active - Write	I_{WRITE}	L	Toggle	Command, Address, Data Input	Hi-Z

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- V_{CC} and V_{CCIO} can ramp up together (R_{VR}), if not possible then V_{CC} first followed by V_{CCIO}. The maximum difference between the two voltages should not exceed 0.7V before reaching the final value of V_{CCIO}.
- The device must not be selected at power-up (a 10KΩ pull-up Resistor to V_{CCIO} on CS# is recommended). Then a further delay of t_{PU} (Figure 10) until V_{CC} reaches V_{CC}(minimum).
- During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences (Figure 10).

Figure 10: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- V_{CC} and V_{CCIO} can ramp down together (R_{VF}), if not possible then V_{CC} first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V after V_{CC} reaches V_{CC_CUTOFF}.
- The device must not be selected at power-down (a 10KΩ pull-up Resistor to V_{CCIO} on CS# is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, when V_{CC} goes below $V_{CC\text{-}CUTOFF}$. The voltage must be dropped below V_{CC}(Reset) for a period of t_{PD}. The power-up timing needs to be observed after V_{CC} goes above V_{CC} (minimum).

Figure 11: Power-Down and Brown-out Behavior

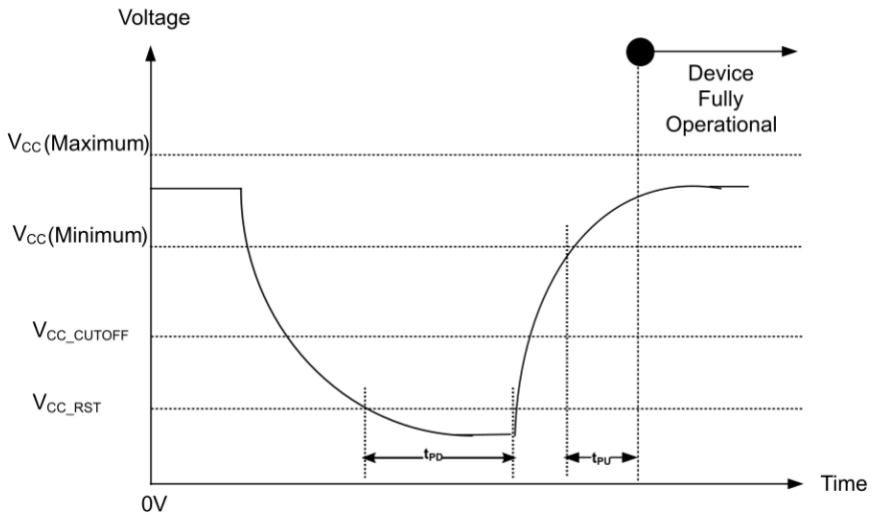


Table 10: Power Up/Down Timing – 3.0V

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.5	-	3.0	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up/RESET to First Instruction	t_{PU}		250	-	-	µs
V_{CC} (low) time	t_{PD}		1			ms
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} (Reset)	V_{CC_RST}		0		0.3	V

The following procedure is required to power down the device correctly:

- It is recommended to power down all supplies together. If not possible then the following sequence must be followed 1-V_{CC}, 2-V_{CCIO}.
- Timing for Ramp down rate should follow ramp down time (R_{VF}).
- CS# cannot be active during power-down (a 10KΩ pull-up Resistor to V_{CCIO} is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, if V_{CC} goes below $V_{CC\text{-}CUTOFF}$. All supply voltages V_{CC} and V_{CCIO} must be dropped below their respective (RESET) values V_{CC_RST} for a period of t_{PD}. Figure-11 timing needs to be observed for the subsequence power-up.

Memory Map

Table 11: Memory Map

Density	Address Range	24-bit Address [23:0]	
64Mb	000000h – 07FFFFFh	[23] – Logic '0'	[22:0] - Addressable
128Mb	000000h – 0FFFFFFh	[23] – Logic '0'	[23:0] - Addressable

Register Addresses

Table 12: Register Addresses

Register Name	Address
Status Register	0x000000h
Configuration Register 1	0x000002h
Configuration Register 2	0x000003h
Interrupt Configuration Register	0x000004h
ECC Test – Data Input Register	0x000005h
ECC Test – Error Injection Register	0x000006h
ECC Test – Data Output Register	0x000007h
ECC Test – Error Count Register	0x000008h
Flag Status Register	0x00000Ah
Device Identification Register	0x000030h

Notes: 1: The Status and Configuration registers need to be re-initialized after a solder reflow process.

Hardware Block Protection

The Hardware Block Protect signals (HBP0, HBP1, and HBP2), when driven High or Low, define the size of the memory array to be hardware protected against all Write memory array instructions. When one or more HBP signals are driven High, the relevant memory area, as defined in Table 13 and Table 14 below, becomes protected against all Write memory array instructions. When all three signals, HBP0, HBP1, and HBP2 are driven Low, the memory array is in normal operation without being write-protected.

The Hardware Top/Bottom Select signal (HTBSEL), when driven High or Low, is used in conjunction with the Hardware Block Protect signals (HBP0, HBP1, and HBP2) to determine if the write-protected memory area defined by the state of the HBP signals, starts from the top or the bottom of the memory array:

- When the HTBSEL signal is driven Low, the memory area, protected by the HBP signals, starts from the top of the memory array.
- When the HTBSEL signal is driven High, the memory area, protected by the HBP signals, starts from the bottom of the memory array.

These pins have an internal pull down to Vss. If the pins are left unconnected, the device will have no hardware protection and all regions of the device can be written to (unless the Software Block Protection is activated through the Status Register).

Table 13: Hardware Top Block Protection Address Range Selection (HTBSEL Signal = L)

HBP [2]	HBP [1]	HBP [0]	Protected Portion	64Mb	128Mb
L	**L**	**L**	None	None	None
L	**L**	**H**	Upper 1/64	7E0000h – 7FFFFFh	FC0000h - FFFFFFh
L	**H**	**L**	Upper 1/32	7C0000h – 7FFFFFh	F80000h - FFFFFFh
L	**H**	**H**	Upper 1/16	780000h – 7FFFFFh	F00000h - FFFFFFh
H	**L**	**L**	Upper 1/8	700000h – 7FFFFFh	E00000h - FFFFFFh
H	**L**	**H**	Upper 1/4	600000h – 7FFFFFh	C00000h - FFFFFFh
H	**H**	**L**	Upper 1/2	400000h – 7FFFFFh	800000h - FFFFFFh
H	**H**	**H**	All	000000h – 7FFFFFh	All

Table 14: Hardware Bottom Block Protection Address Range Selection (HTBSEL Signal = H)

HBP [2]	HBP [1]	HBP [0]	Protected Portion	64Mb	128Mb
L	**L**	**L**	None	None	None
L	**L**	**H**	Lower 1/64	000000h – 01FFFFh	000000h - 03FFFFh
L	**H**	**L**	Lower 1/32	000000h – 03FFFFh	000000h - 07FFFFh
L	**H**	**H**	Lower 1/16	000000h – 07FFFFh	000000h – 0FFFFFh
H	**L**	**L**	Lower 1/8	000000h – FFFFFh	000000h – 1FFFFFh
H	**L**	**H**	Lower 1/4	000000h – 1FFFFFh	000000h – 3FFFFFh
H	**H**	**L**	Lower 1/2	000000h – 3FFFFFh	000000h – 7FFFFFh
H	**H**	**H**	All	000000h – 7FFFFFh	000000h – FFFFFFh

Notes:
High (H): Logic '1'
Low (L): Logic '0'

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

Table 15: Status Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	RSVD	Reserved	R/W	0	Reserved
SR[5]	TBSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits (Table 16, Table 17)
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Protection Enable/Disable	R	0	1: Write Operation Protection Disabled 0: Write Operation Protection Enabled
SR[0]	RSVD	Reserved	R/W	0	Reserved

Software Block Protection

These 3 bits are OR'ed with the Hardware Protection Bits and can be used to dynamically protect regions of memory.

Table 16: Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	64Mb	128Mb
L	L	L	None	None	None
L	L	H	Upper 1/64	7E0000h – 7FFFFFh	FC0000h - FFFFFFh
L	H	L	Upper 1/32	7C0000h – 7FFFFFh	F80000h - FFFFFFh
L	H	H	Upper 1/16	780000h – 7FFFFFh	F00000h - FFFFFFh
H	L	L	Upper 1/8	700000h – 7FFFFFh	E00000h - FFFFFFh
H	L	H	Upper 1/4	600000h – 7FFFFFh	C00000h - FFFFFFh
H	H	L	Upper 1/2	400000h – 7FFFFFh	800000h - FFFFFFh
H	H	H	All	000000h – 7FFFFFh	All

Table 17: Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	64Mb	128Mb
L	L	L	None	None	None
L	L	H	Lower 1/64	000000h – 01FFFFh	000000h - 03FFFFh
L	H	L	Lower 1/32	000000h – 03FFFFh	000000h - 07FFFFh
L	H	H	Lower 1/16	000000h – 07FFFFh	000000h – 0FFFFFh
H	L	L	Lower 1/8	000000h – FFFFFh	000000h – 1FFFFFh
H	L	H	Lower 1/4	000000h – 1FFFFFh	000000h – 3FFFFFh
H	H	L	Lower 1/2	000000h – 3FFFFFh	000000h – 7FFFFFh
H	H	H	All	000000h – 7FFFFFh	000000h – FFFFFFh

Table 18: Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status & Configuration Registers	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	**X**	**X**	Protected	Protected	Protected
1	**0**	**X**	Unprotected	Protected	Unprotected
1	**1**	**Low**	Protected	Protected	Unprotected
1	**1**	**High**	Unprotected	Protected	Unprotected

Notes:
High: Logic '1'
Low: Logic '0'
X: Don't Care – Can be Logic '0' or '1'
Protected: Write protected
Unprotected: Writable
1: Memory address range protection based on Block Protection Bits

Flag Status Register (Read Only)

Flag status register contains device's access status and addressing information.

Table 19: Flag Status Register (Read Only)

Bits	Name	Description	Read / Write	Default State	Selection Options
FSR1[7]	ST	Device Access Status	R	1	1: Ready 0: Busy
FSR1[6:1]	RSVD	Reserved	R	0	Reserved for future use
FSR1[0]	RSVD	Reserved	R	0	Reserved for future use

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 20: Device Identification Register – Read Only

Bits	Avalanche Manufacturer's ID	Device Configuration				
ID[31:0]	ID[31:24]	Interface	Voltage	Temp	Density	Freq
		ID[23:20]	ID[19:16]	ID[15:12]	ID[11:8]	ID[7:0]

Manufacturer ID	Interface	Voltage	Temperature	Density	Frequency
31-24	23-20	19-16	15-12	11-8	7-0
1110 0110	0010-HP Dual QSPI	0001 - 3V	0000 - -40ºC- 85ºC	0001 – 64Mb	00000001 – 100MHz
			0001 - -40ºC-105ºC	0010 – 128Mb	00000010 – Reserved
			0010 - -40ºC-125ºC	0011 – Reserved	00000011 – Reserved
				0100 – Reserved	00000100 – Reserved
				1000 – Reserved	00000101 – Reserved
				1001 – Reserved	00000110 – Reserved
				1010 – Reserved	00000111 – Reserved
				1100 – Reserved	00001000 – Reserved

Configuration Register 1 (Read/Write)

Configuration Register 1 controls locking/unlocking data protection options set in the Status register. Once locked, the protection options cannot be changed in the Status register.

Table 21: Configuration Register 1 – Read and Write

Bits	Name	Description	Read / Write	Default	Selection Options (Ohm)			
					VCCIO			
						1.8V	2.5V	3.0V
CR1[7]	ODSEL[2]	Output Driver Strength Selector	R/W	1	**000**	40	25	22
					001	40	25	22
					010	40	25	22
CR1[6]	ODSEL[1]			1	**011**	40	25	22
					100	150	110	90
CR1[5]	ODSEL[0]			0	**101**	80	50	45
					110	50	35	30
					111	40	25	22
CR1[4]	RSVD	Reserved	R	0	Reserved for future use			
CR1[3]	RSVD	Reserved	R	0	Reserved for future use			
CR1[2]	MAPLK	Status Register Lock Enable/Disable (TBSEL, BPSEL[2:0]	R/W	0	1: Lock TBSEL and BPSEL[2:0] 0: Unlock TBSEL and BPSEL[2:0]			
CR1[1]	WRENS[1]	WREN Reset Selector (Memory Array Write Functionality)	R/W	0	00: Normal: WREN is prerequisite to all Memory Array Write instruction. (WREN is reset after CS# goes High) 01: SRAM: WREN is not a prerequisite to Memory Array Write instruction (WREN is ignored) 10: Back-to-Back: WREN is prerequisite to only the first Memory Array Write instruction. WREN disable instruction must be executed to reset WREN. (WREN does not reset once CS# goes High) 11: Illegal - Reserved for future use			
CR1[0]	WRENS[0]			0				

Notes:
1: Write Enable protection (WREN – Status Register) for Registers is maintained irrespective of the Configuration Register 1 settings. In other words, all register write instructions require WREN to be set and WREN resets once CS# goes High for the write instruction.

Configuration Register 2 (Read/Write)

Configuration Register 2 controls the interface type along with memory array access latency.

Table 22: Configuration Register 2 (CR2) – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
CR2[7]	RSVD	Reserved	R	0	Reserved for future use
CR2[6]	RSVD	Reserved	R	0	Reserved for future use
CR2[5]	RSVD	Reserved	R	0	Reserved for future use
CR2[4]	XIPWR	XIP Write	R/W	0	0: Enable XIP Write – Default 1: Disable XIP Write
CR2[3]	MLATS[3]	Memory Array Read/Read Any Register Latency Selection [1]	R/W	1	0000: 0 Cycles 0001: 1 Cycle 0010: 2 Cycles 0011: 3 Cycles 0100: 4 Cycles 0101: 5 Cycles 0110: 6 Cycles 0111: 7 Cycles 1000: 8 Cycles - Default 1001: 9 Cycles 1010: 10 Cycles 1011: 11 Cycles 1100: 12 Cycles 1101: 13 Cycles 1110: 14 Cycles 1111: 15 Cycles
CR2[2]	MLATS[2]			0	
CR2[1]	MLATS[1]			0	
CR2[0]	MLATS[0]			0	

Notes:
1: Latency is frequency dependent. Please consult Table 23, 24 and 25

Table 23: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

Read Type	Latency	AS3xxx204/8-0108
(1-1-1) SDR	12-15	100MHz
(1-1-1) DDR	8-15	50MHz
(1-1-4) SDR	12-15	100MHz
(1-1-4) DDR	8-15	50MHz
(1-4-4) SDR	12-15	100MHz
(1-4-4) DDR	8-15	50MHz
(4-4-4) SDR	12-15	100MHz
(4-4-4) DDR	8-15	50MHz

Table 24: Memory Read Latency Cycles vs. Maximum Clock Frequency (without XIP)

Read Type	Latency	Max Frequency
		AS3xxx204/8-0108
(1-1-1)	0	50MHz

Table 25: Read Any Register Command Latency Cycles vs. Maximum Clock Frequency

Read Type	Latency Cycles	Max Frequency
(1-1-1) SDR	12-15	100MHz
(4-4-4) SDR	12-15	100MHz

Interrupt Configuration Register (Read/Write)

The Interrupt Configuration Register controls different events that trigger INT# pin transitioning from High to Low state. INT# pin can be configured in the INT# configuration register to transition to the active Low state when either ECC error is detected and corrected or transitioning from the busy to the ready state.

Table 26: Interrupt Configuration Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Selection Options
INTCR[7]	INTRF	Shows status of ECC error detection	R	0	Selection Options: 1: Unrecoverable ECC error detected 0: No unrecoverable ECC error detected
INTCR[6]	INTR	Clear Interrupt Status	W	0	Selection Options: 1 = Resets Interrupt caused by unrecoverable ECC 0 = No Action
INTCR[5]	ECC_CR	Reset the ECC Error Count Register	W	0	Selection Options: 1 = Resets ECC count register to 0 0 = No Action
INTCR[4]	----	Reserved	-	-	Reserved for future use
INTCR[3:2]	----	Reserved	-	-	Reserved for future use
INTCR[1]	ECCTE	ECC Test Enable	W	0	ECC Test Engine Test mode: 1 = Enable 0 = Disable
INTCR[0]	ECCEDS	ECC Error Detection Selection	W	0	Selection Options: 1 = ECC detection will transition a High to Low state on the INT# pin 0 = ECC detection will not transition the INT# pin

Error Correction Code (ECC) Test – Data Input Register

The contents of this register are entered into the ECC engine data buffer i.e. used as data input to test the ECC engine.

Table 27: ECC Test Data Input Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_In	Data Input	R/W	00000000	Any value from 00000000 to FFFFFFFF

Error Correction Code (ECC) Test – Error Injection

The contents of this register are used as an error mask to inject error to test the ECC engine.

Table 28: ECC Test Error Injection Register – Read and Write

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Error_Injection	Error Mask	R/W	00000000	1 in any position injects an error into ECC engine. For example, 00000003 will inject a two-bit error in two LSB bits i.e. the Data in the ECC engine buffer is Exclusive or'd with the error mask.

Error Correction Code (ECC) Test – Data Output Register

The contents of this register are the output of the ECC engine when testing the ECC engine.

Table 29: ECC Test Data Output Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	ECC_Data_Out	Output of ECC engine	R	00000000	None – read only.

Error Correction Code (ECC) – Error Count Register

This register must only be used during TEST MODE for testing the ECC engine. The Error Count Register is incremented when uncorrectable ECC errors are induced during the test mode. During normal operation of the device, the content of this register is not reflective of corrected or uncorrected errors. An interrupt is generated on device pin INT# and the interrupt flag is set when an unrecoverable error is detected in test mode.

Table 30: ECC Count Register – Read Only

Bits	Name	Description	Read / Write	Default State	Select Options
[31:0]	Error_Count	Number of induced uncorrectable Errors detected during TEST mode	R	32'b0	None – read only

Instruction Set

Table 31: Instruction Set

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-0-4)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite	Note
1	**No Operation**	NOOP 00h	•					•				•				100 MHz		
2	**Write Enable**	WREN 06h	•					•				•				100 MHz		
3	**Write Disable**	WRDI 04h	•					•				•				100 MHz		
4	**Enable QPI**	QPIE 38h	•									•				100 MHz		
5	**Enable SPI**	SPIE FFh	•					•				•				100 MHz		
6	**Read Status Register**	RDSR 05h		•					•			•			1	50 MHz		
7	**Read Flag Status Register**	RDFSR 70h		•					•			•			1	50 MHz		
8	**Read Device ID**	RDID 9Fh		•					•			•			4	50 MHz		
9	**Read Any Register - Address Based**	RDAR 65h			•					•		•		•	1	100 MHz		
10	**Write Status Register**	WRSR 01h		•					•			•			1	100 MHz	WREN	
11	**Write Any Register - Address Based**	WRAR 71h			•					•		•			1	100 MHz	WREN	
12	**Read Memory Array - SDR**	READ 03h			•							•			1 to ∞	50 MHz		1,2
13	**Read Memory Array - SDR**	READ 13h			•							•			1 to ∞	50 MHz		1,2,5

#	Instruction Name	Command (Opcode)	(1-0-0)	(1-0-1)	(1-1-1)	(1-1-4)	(1-4-4)	(4-0-0)	(4-0-4)	(4-4-4)	XIP	SDR	DDR	Latency Cycles	Data Bytes	Max. Frequency	Prerequisite	Note
14	**Fast Read Memory Array - SDR**	RDFT 0Bh			•					•		•		•	1 to ∞	100 MHz		1,2,3,5
15	**Fast Read Memory Array - SDR**	READ 0Ch			•					•		•		•	1 to ∞	100 MHz		1,2,3,5
16	**Fast Read Memory Array - DDR**	RDFT 0Dh			•					•	•		•	•	1 to ∞	50 MHz		1,2,3
17	**Read Quad Output Memory Array - SDR**	RDQO 6Bh				•						•		•	1 to ∞	100 MHz		1,2,3,5
18	**Read Quad Output Memory Array - SDR**	RDQO 6Ch				•						•		•	1 to ∞	100 MHz		1,2,3,5
19	**Read Quad I/O Memory Read - SDR**	RDQI EBh					•				•	•		•	1 to ∞	100 MHz		1,2,3
20	**Read Quad I/O Memory Read - DDR**	DRQI EDh					•				•		•	•	1 to ∞	50 MHz		1,2,3
21	**Write Memory Array - SDR**	WRTE 02h			•					•		•			1 to ∞	100 MHz	WREN	1,4
22	**Fast Write Memory Array - SDR**	WRFT DAh			•					•	•	•			1 to ∞	100 MHz	WREN	1,2,4
23	**Fast Write Memory Array - DDR**	4DRFW DEh			•					•	•		•		1 to ∞	50 MHz	WREN	1,2,4
24	**Write Quad I/O Memory Array - SDR**	WQIO D2h					•				•	•			1 to ∞	100 MHz	WREN	1,2,4
25	**Write Quad I/O Memory Array - DDR**	4DWQO D1h					•				•		•		1 to ∞	50 MHz	WREN	1,2,4

Notes:
1: A typical SPI instruction consists of command, address and data components. The bus width to transmit these three components varies based on the SPI interface mode selected. To accurately represent the number of I/Os used to transmit these three components, a nomenclature (command-address-data) is adopted and used throughout this document. Integers placed in the (command-address-data) fields represent the number of I/Os used to transmit the particular component. As an example, 1-1-1 means command, address and data are transmitted on a single I/O Dual-Quad SPI device 1 (SI / IO[0] or SO / IO[1]) and Dual-Quad SPI device 2 (SI / IO[04 or SO / IO[7]). On the other hand, 1-4-4 represents command being

sent on a single I/O Dual-Quad SPI device 1 (SI / IO[0]) and Dual-Quad SPI device 2 (SI / IO[4]) - address/data being sent on four I/Os of Dual-Quad SPI device 1 (IO[3:0]) and Dual-Quad SPI device 2 (IO[7:4])
2: XIP allows completing a series of read and write instructions without having to individually load the read or write command for each instruction. A special mode byte must be entered after the address bits to enable/disable XIP – Axh / Fxh.
3: Fast Read instruction must include Latency cycles to meet higher frequency. They are configurable (Configuration Register 2 – CR2[3:0]) and frequency dependent.
4: WREN prerequisite for array writing is configurable (Configuration Register 1– CR1[1:0])
5. Support legacy device boot on Xilinx platforms

Instruction Description and Structures

All communication between a host and AS3xxxx204/8 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from AS3xxxx204/8. All command, address and data information are transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic'1').
- CLK marks the transfer of each bit.
- Each instruction starts out with an 8-bit command. The command selects the type of operation AS3xxxx204/8 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location or register. The address is 24-bit wide and is transferred on the rising edges of CLK.
- The address bits are followed by data bits. For Write instructions, write data bits to AS3xxxx204/8 are transferred on the rising edges of CLK.
- In normal operational mode, Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every Write instruction. WREN bit can also be reset by executing the WRDI instruction. AS3xxxx204/8 offers two other modes, namely SRAM and Back-to-Back Write where WREN does not get reset after a write instruction to the memory array. These modes are set in Configuration Register 1. For XIP supported Write instructions, XIP can be enabled or disabled through Configuration Register 2, bit 4 (CR2[4]).
- Similar to write instructions, the address bits are followed by data bits for read instructions:
    - Read data bits from AS3xxxx204/8 are transferred on the falling edges of CLK.
- AS3xxxx204/8 is a high-performance serial memory and at higher frequencies, read instructions require latency cycles to compensate for the memory array access time. The number of latency cycles required depends on the operational frequency and is configurable – Configuration Register 2. The latency cycles are inserted after the address bits before the data comes out of AS3xxxx204/8.
- For Read and Write instructions, AS3xxxx204/8 offers XIP mode. XIP allows similar instructions to be executed sequentially without incurring the command cycles overhead.
    - For XIP supported Read instructions, XIP is enabled by entering byte Axh and disabled by entering byte Fxh. These respective bytes must be entered following the address bits.
    - For XIP supported Write instructions, XIP can be enabled or disabled through Configuration Register 2, bit 4 (CR2[4]).
- The entire memory array can be read from or written to using a single read or write instruction. After the staring address is entered, subsequent addresses are internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bits.

Figure 12 to Figure 20 show the description of SDR instruction types supported.

Figure 12: Description of (1-0-0) Instruction Type

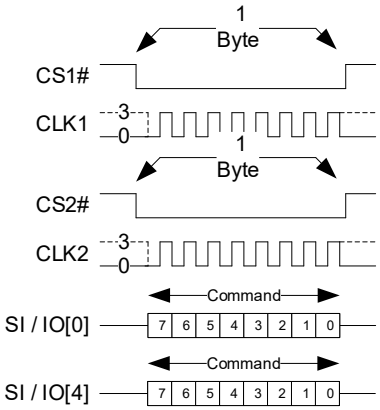


Figure 13: Description of (1-0-1) Instruction Type

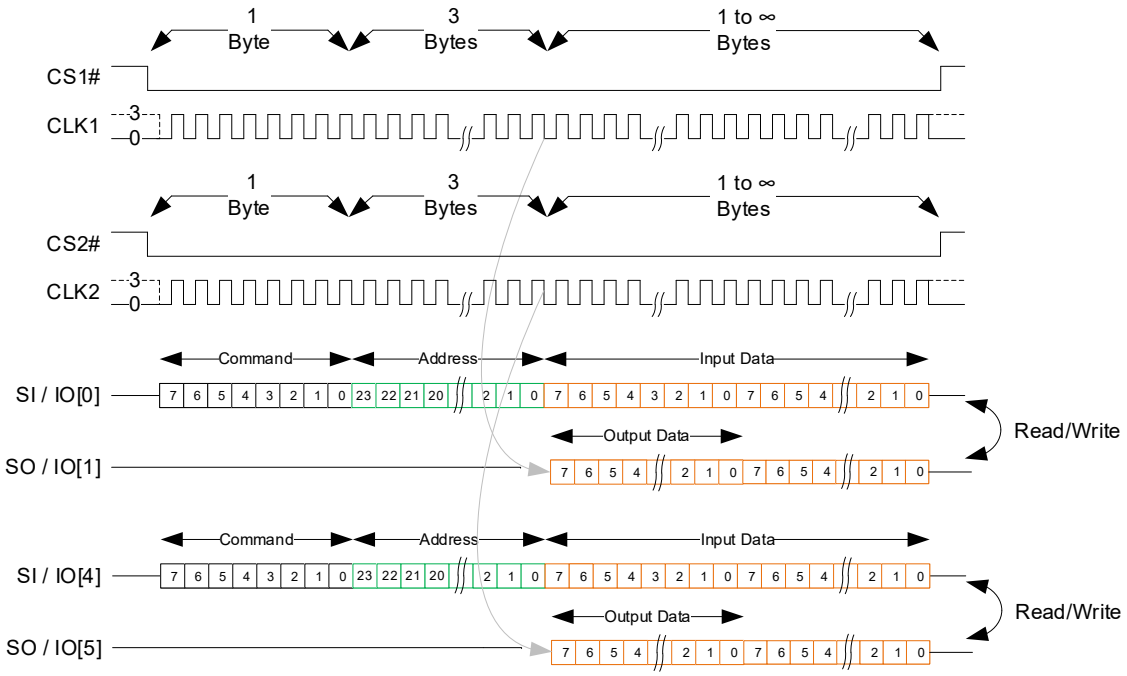


Figure 14: Description of (1-1-1) Instruction Type (Without XIP)

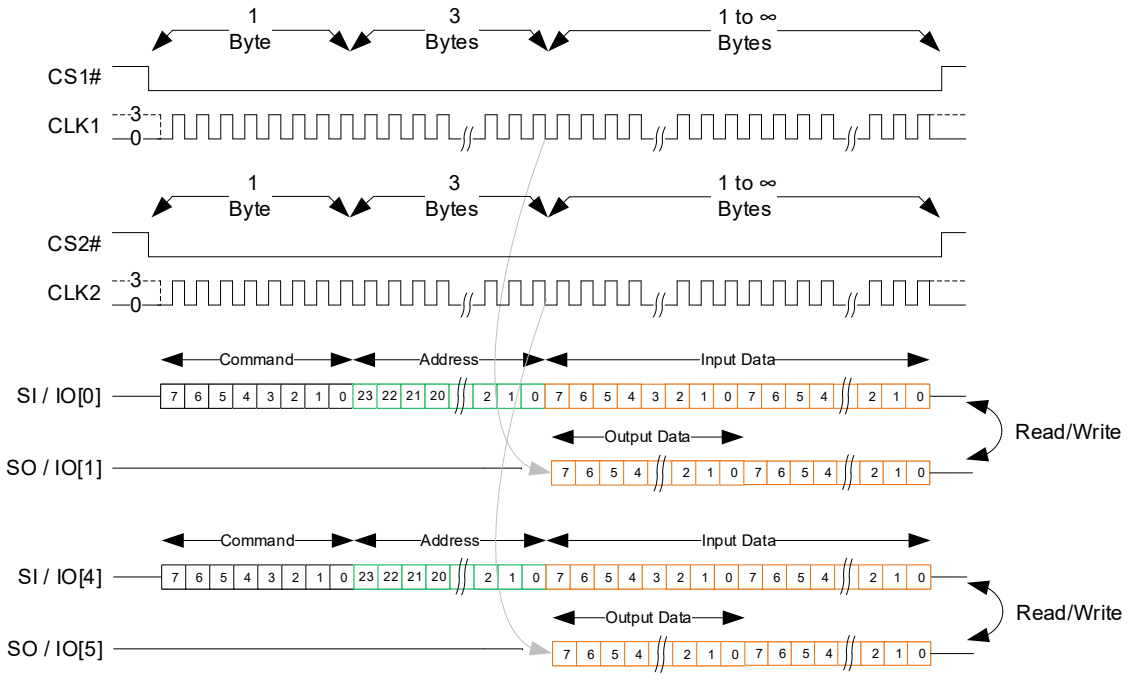


Figure 15: Description of (1-1-1) Instruction Type (With XIP)

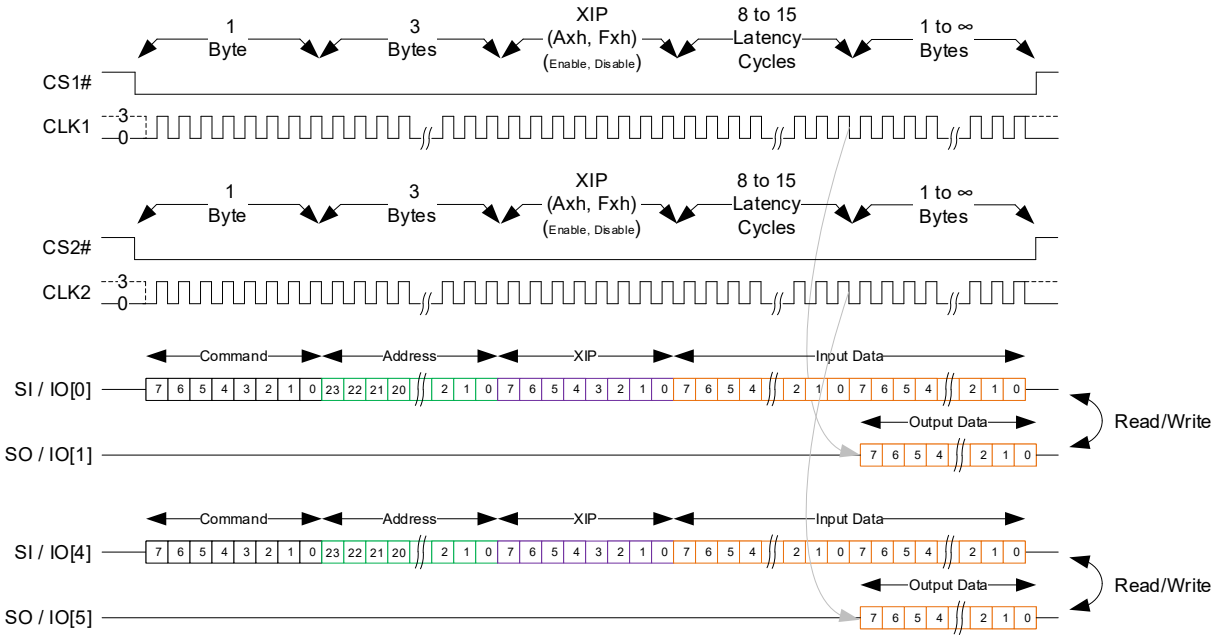


Figure 16: Description of (1-1-1) Instruction Type (Without XIP)

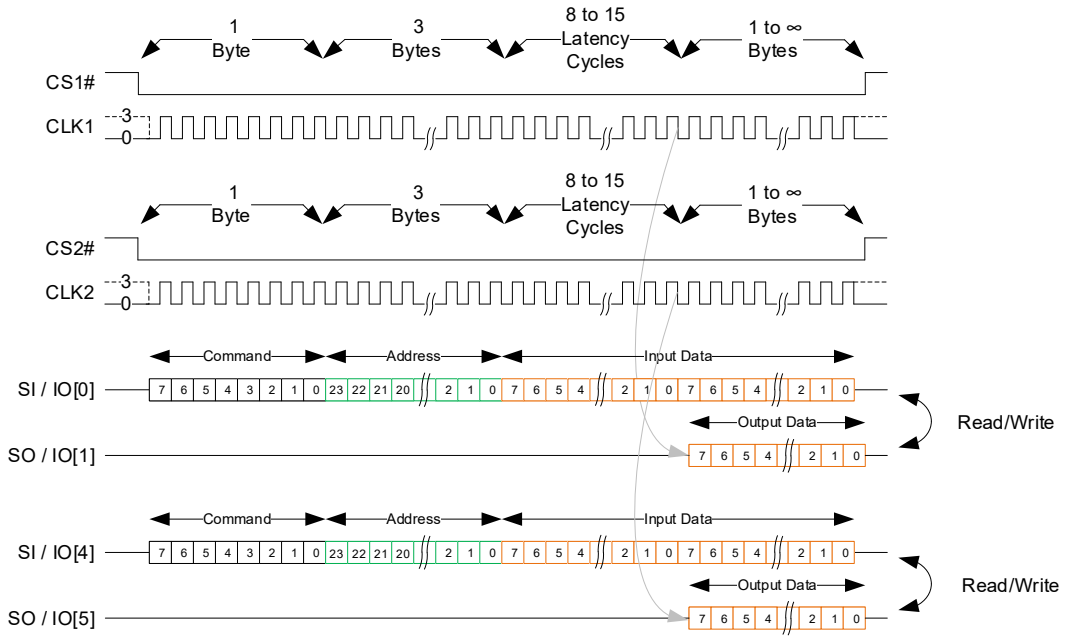


Figure 17: Description of (1-1-4) Instruction Type (Without XIP)

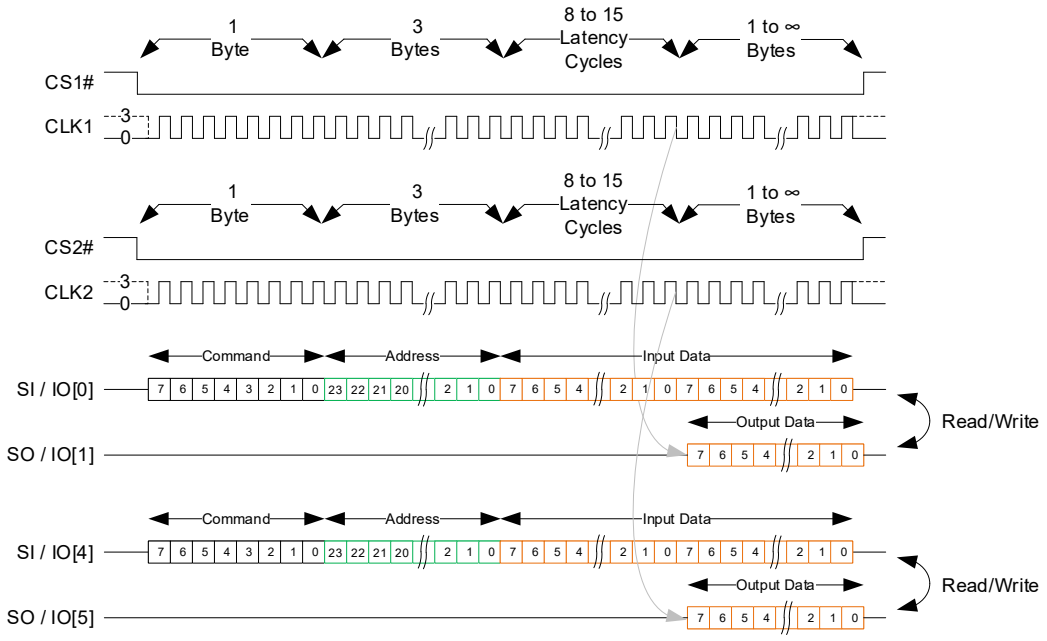


Figure 18: Description of (1-4-4) Instruction Type with XIP

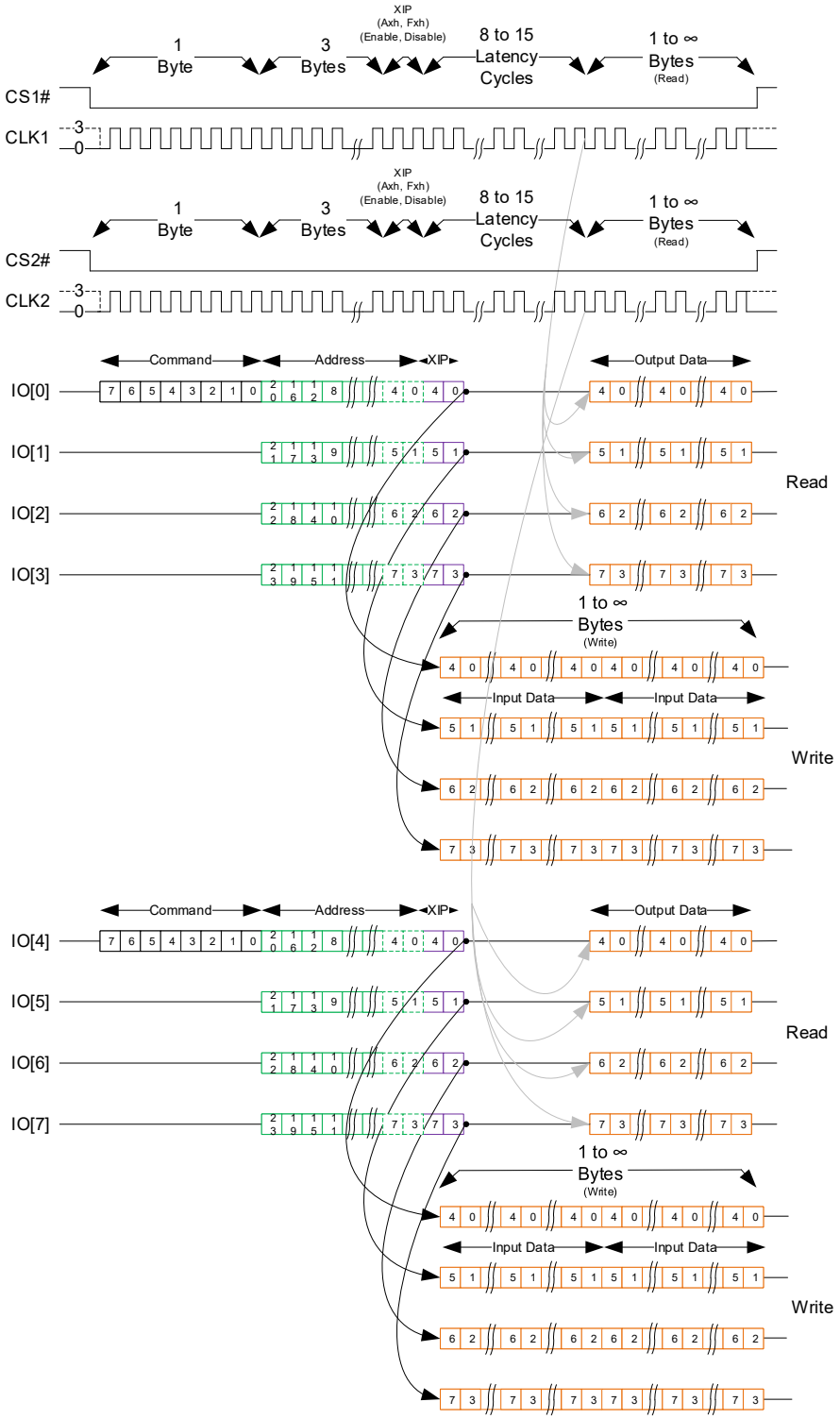


Figure 19: Description of (4-4-4) Instruction Type (Without XIP)

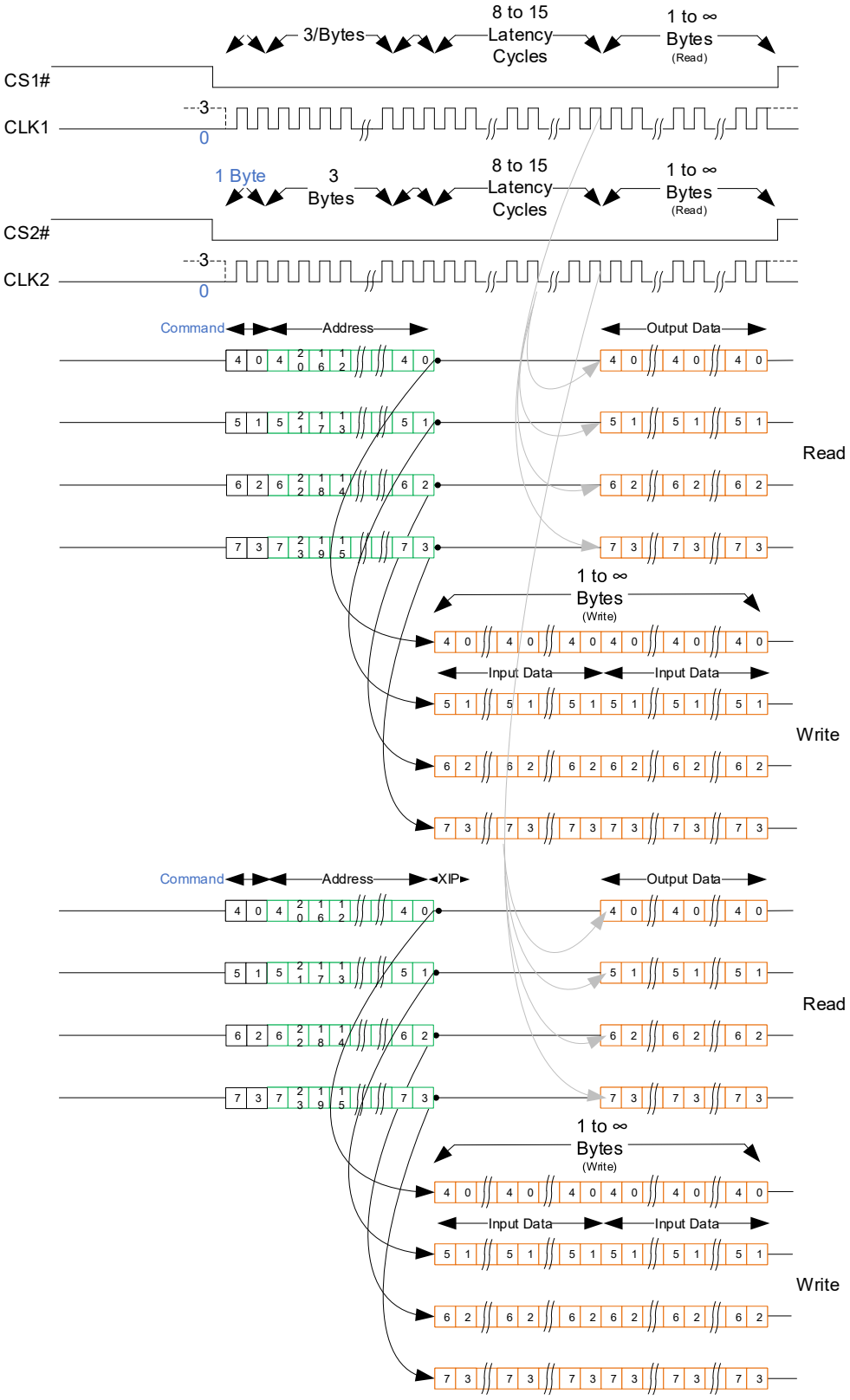


Figure 20: Description of (4-4-4) Instruction Type with XIP

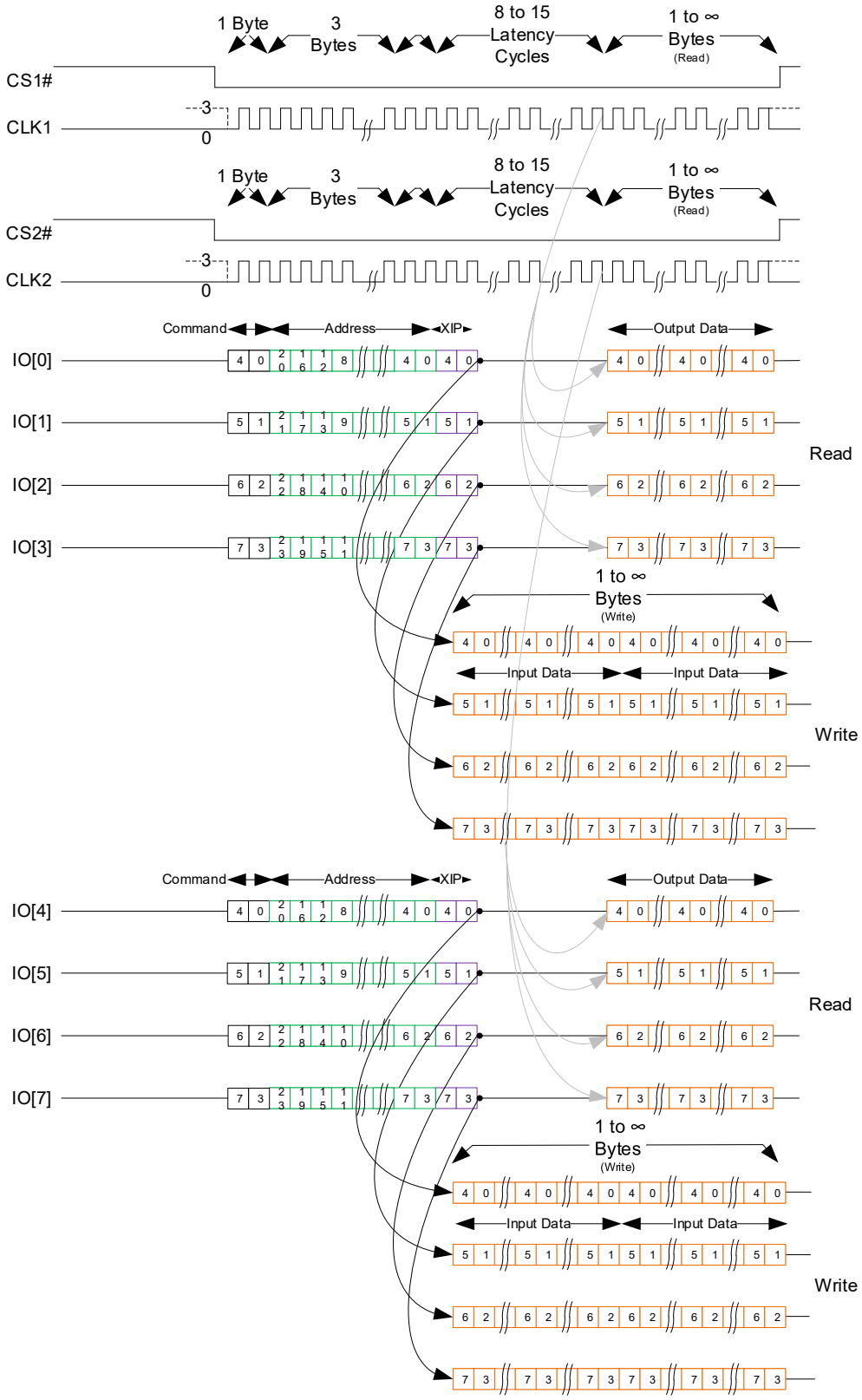


Figure 21 to **Figure 22** show the description of DDR instruction types supported.

Figure 21: Description of (1-1-1) DDR Instruction Type (With XIP)

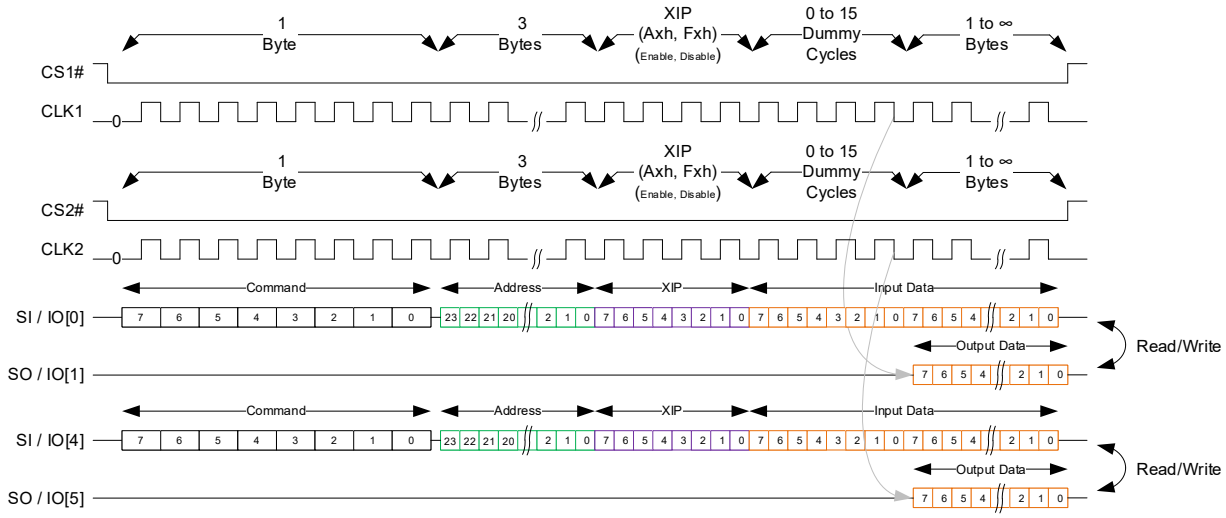
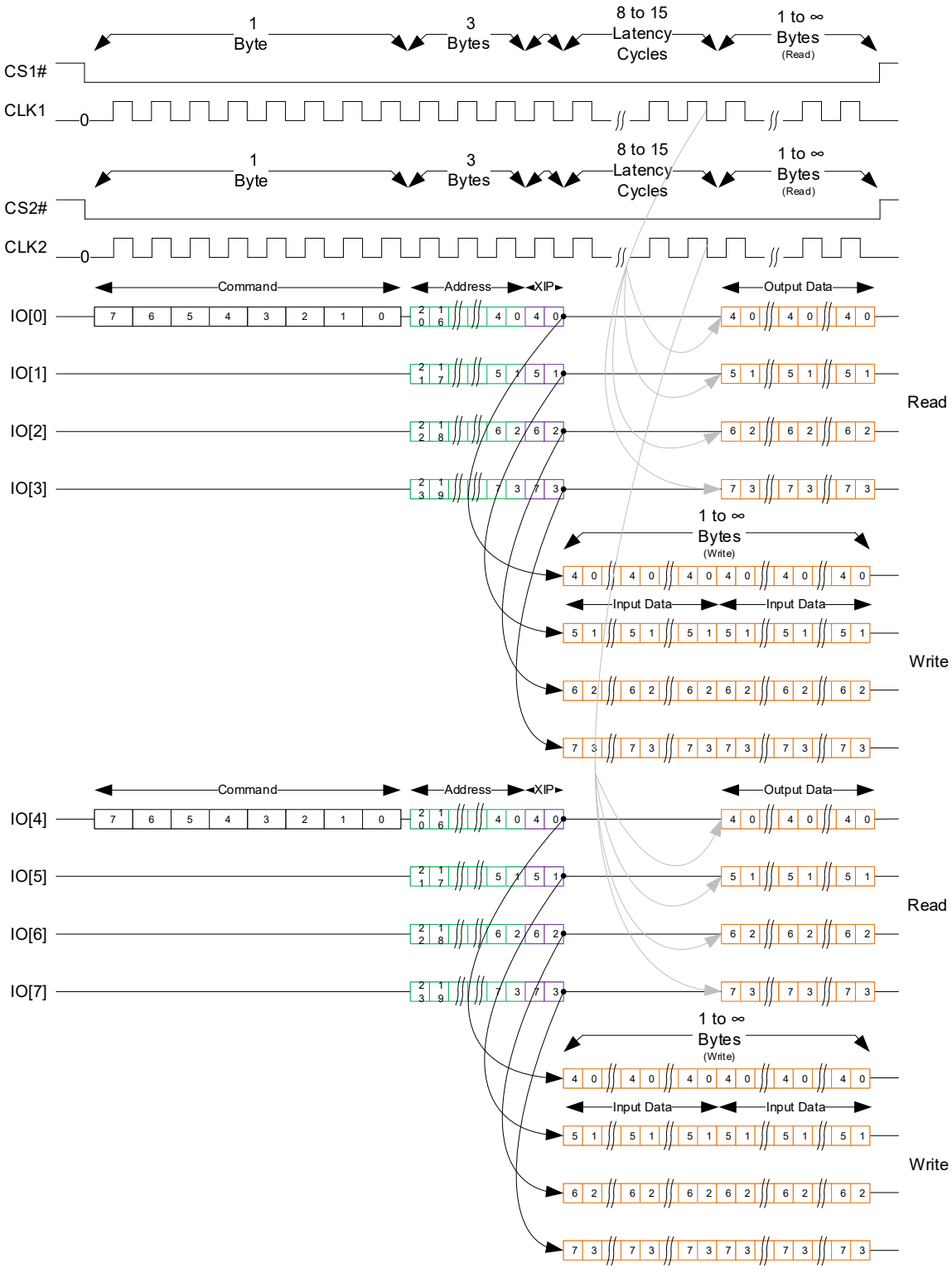


Figure 22: Description of (1-4-4) DDR Instruction Type (With XIP)



Electrical Specifications

Table 32: Recommended Operating Conditions

Parameter / Condition	Minimum	Typical	Maximum	Units
Operating Temperature (T_A)	-40.0	-	125.0	°C
V_{CC} Supply Voltage	2.45	-	3.60	V
V_{CCIO} Supply Voltage	1.8 – 2.5 – 3.3			V
V_{SS} Supply Voltage	0.0	0.0	0.0	V
V_{SSIO} Supply Voltage	0.0	0.0	0.0	V

Table 33: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{IN}	5.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{INOUT}	6.0	pF

Table 34: Endurance & Data Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	85°C	20	years

Table 35: 3.0V DC Characteristics

Parameter	Symbol	Test Conditions	Density	3.0V Device (2.5V-3.6V)				
				Min	Typical[1]	85°C[2]	Max[3]	Units
Active Read Current	I_{READ}	V_{CC} = 3.0V, CLK=100MHz	64Mb		10	11	18	mA
			128Mb		20	22	35	mA
Active Write Current	I_{WRITE}	V_{CC} = 3.0V, CLK=100MHz	64Mb		10	14	23	mA
			128Mb		20	28	45	mA
Standby Current	I_{SB}	V_{CC} = 3.0V, CLK=V_{CCIO}, CS#=V_{CCIO}, SI=WP#=V_{CCIO}	64Mb		7	10	13	mA
			128Mb		13	16	25	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CCIO} (max)		-	-		±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CCIO} (max)		-	-		±1.0	µA
Input High Voltage (V_{CCIO}=1.71-2.2)	V_{IH}			0.65* V_{CCIO}	-		V_{CCIO}+0.2	V
Input High Voltage (V_{CCIO}=2.2-2.7)				1.8				
Input High Voltage (V_{CCIO}=2.5-3.6)				2.2				
Input Low Voltage (V_{CCIO}=1.71-2.2)	V_{IL}			-0.2	-		0.35* V_{CCIO}	V
Input Low Voltage (V_{CCIO}=2.2-2.7)							0.7	
Input Low Voltage (V_{CCIO}=2.5-3.6)							0.8	
Output Low Voltage (V_{CCIO}=1.71-2.2)	V_{OL}	I_{OL} = 0.1mA		-			0.2	V
Output Low Voltage (V_{CCIO}=2.2-2.7)		I_{OL} = 0.1mA					0.4	
Output Low Voltage (V_{CCIO}=2.5-3.6)		I_{OL} = 2.0mA					0.4	
Output High Voltage (V_{CCIO}=1.71-2.2)	V_{OH}	I_{OH} = -0.1mA		1.4			-	V
Output High Voltage (V_{CCIO}=2.2-2.7)		I_{OH} = -0.1mA		2.0				
Output High Voltage (V_{CCIO}=2.5-3.6)		I_{OH} = -1.0mA		2.4				

Notes:

[1] Typical values are measured at 25°C

[2] 85°C values are guaranteed by characterization; not tested in production

[3] Max values are measured at 125°C

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table 36: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Junction Temperature	---	150	°C
Storage Temperature	-55 to 150		°C
Supply Voltage Vcc	-0.5	4.0	V
Supply Voltage Vccio	-0.5	3.8	V
Voltage on any pin	-0.5	Vccio + 0.2	V
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥ |2000 V|		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥ |500 V|		V
Latch-Up (I-test) JESD78	≥ |100 mA|		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

Table 37: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	3.0ns
Input and output measurement timing levels	$V_{CC}/2$
Output Load	CL = 30.0pF

CS# Operation & Timing

Figure 23: CS# Operation & Timing

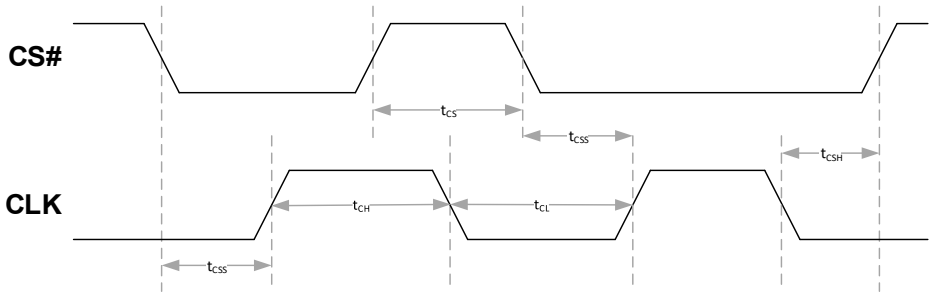


Table 38: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	100	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Register Write Cycle	t_{CS2}	5	-	µs
Chip Deselect Time after Write Cycle (SPI)	t_{CS3}	280	-	ns
Chip Deselect Time after Write Cycle (QPI)	t_{CS5}	490[1]	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:
Power supplies must be stable

[1] For single byte operations, t_{CS5} is 280ns

Command, Address, XIP and Data Input Operation & Timing

Figure 24: Command, Address and Data Input Operation & Timing

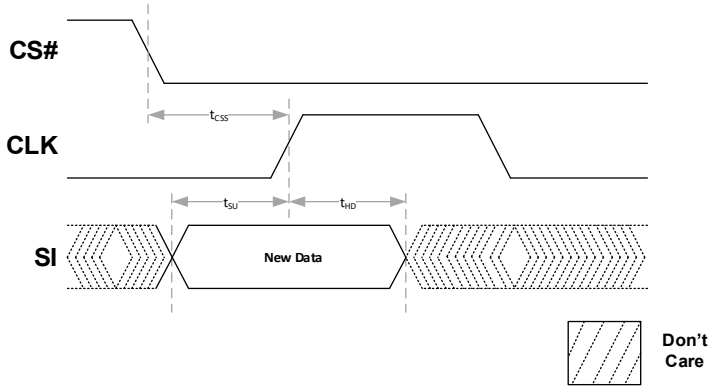


Table 39: Command, Address, XIP, and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	2.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	3.0	-	ns

Notes:
Power supplies must be stable

Data Output Operation & Timing

Figure 25: Data Output Operation & Timing

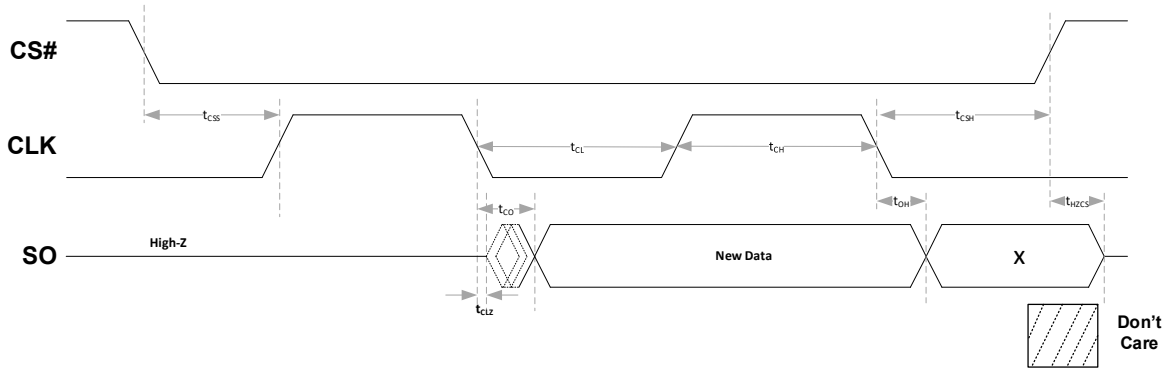


Table 40: Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	7.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	7.0	ns

Notes:
Power supplies must be stable

WP# Operation & Timing

Figure 26: WP# Operation & Timing

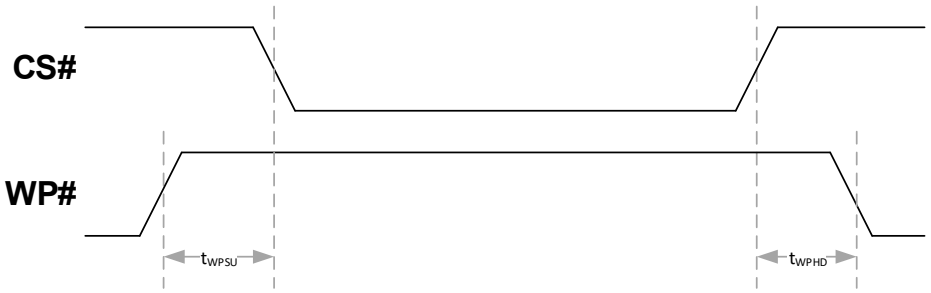


Table 41: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:
Power supplies must be stable

Thermal Resistance

Table 42: Thermal Resistance

Parameter	Description	Test Conditions	56 Ball FBGA		Unit
			64Mb	128Mb	
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	17.89	TBD	°C/W
θ_{JC}	Thermal resistance (junction to case)		2.10	TBD	

Notes:
1: These parameters are guaranteed by characterization; not tested in production.
2: Ambient temperature, T_A 25 ℃
3: Worst case Junction temp specified for Top die (θ_{JA}) and Bottom die (θ_{JC})

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Revision History

Revision	Date	Change Summary
REV A.1	07/28/2023	Initial Release
REV A.2	09/25/2023	Still Preliminary
	10/03/2023	Removed Jedec reset Removed Deep power down Updated DC Characteristics Table
	10/10/2023	Changed Package from 49 to 56 Ball BGA
	10/13/2023	Changed Package from 55 to 56 ball BGA
	10/23/2023	Corrected package drawing
	10/30/2023	Updated Package Drawing from SFA
	10/31/2023	Updated Maximum rating table 35
	12/13/2023	Updated SRO on package drawing
REV A.3	01/17/2024	Removed Unique ID Register. CR1 default for WREN was incorrectly stated as 10. It is 00. CR2 default for latency was incorrectly stated as 0000. It is 8 cycles: 1000
REV B	03/18/2023	Updated to reflect the latest product roadmap: 64M is Single QSPI, and 128M is Dual QSPI Maximum Freq. set to 108MHz SDR/54MHz DDR Opcodes now fully match the 1-8Gb Family Device specification only given under radiation Added Marking Specification.
REV B.1	05/01/2024	Updated t_{PU} Specification: V_{CC} Power Up to First Instruction Updated latency timing for 108MHz (8 to 12 cycles).
REV C	07/12/2024	Maximum Freq. set to 100MHz SDR/50MHz DDR to be consistent with the High desnity Family.
	07/15/2024	Updated Power UP Behavior to allow for Vcc and Vccio mismatch.
	08/15/2024	Cosmetic fixes
	08/21/2024	WP2# IO[6] was mislabelled as E4. in the ball assignment table. Correct ball assignment is G2. The ball diagram was always correct.
	10/28/2024	Corrected performance table references to say: “See Tables” .
C.1	12/19/2024	Changed the radiation perofmance based on latest radiation test report ▪ ***From:*** **LET ≤ 37 MeV cm2/mg** ▪ ***To:*** **LET ≤ 55 MeV cm2/mg**
C.2	04/08/2025	Removed Radiation exposure limit from the datasheet. Updated Max Vcc
C.3	05/20/2025	Cleaned up definition of 2nd die IO[3:0] to [7:4]
C.4	06/10/2025	Added Clock edge use for DDR Updated Power Up Ramp for VCC and VCCIO Updated Table showing HBP [2:0 H-H-H] Output drive strength default value changed to C0 Added package height impact due to reballing to Lead
C.5		Reserved
C.6		Reserved
C.7	11/13/2025	Updated Instruction Set table to include Latency Cycles for Read Any Register Updated Output Drive Strength Options Corrected Part number on Table 4