

Data Endurance, Retention and Field Immunity in STT-MRAM.

AN000002 details the Endurance, Retention and Field Immunity characteristics of Avalanche's STT-MRAM devices and highlights its capabilities.

1. Introduction

Spin Torque Magneto-Resistive Random Access Memory (STT-MRAM) based on perpendicular magnetic tunnel junction (pMTJ) is by far the most promising emerging non-volatile memory (NVM) technology with a unique combination of low power, fast read/write speeds and practically unlimited endurance. This application note presents studies on time-dependent dielectric breakdown (TDDB), data retention and field immunity properties of STT-MRAM based on Avalanche's proprietary pMTJ technology. The results of the studies show projected endurance of $>10^{14}$ write cycle, 10 years data retention at 125°C, the operation immunity field of up to 700 Oe and standby immunity field of up to 1000 Oe. This suggests that STT-MRAM meets and exceeds the requirements of most memory use cases for data storage, code storage, and scratchpad memories for embedded and high-performance computing applications, such as last-level caches (LLC).

2. Endurance

Endurance specifies the cumulative number of program/erase cycles of memory devices without unrecoverable errors. Endurance is a ubiquitous issue in Flash memories and relates to the product's end-of-life. Each program/erase operation introduces defects in the flash memory cell structure (oxide) that accumulate over time. At some point, defect-induced errors prevent the flash cell from normal operation, rendering it unusable. STT-MRAM, on the other hand, does not store charge and uses magnetic states instead for storage. Programming is achieved by pulsing a current through an MTJ element, causing the magnetization direction of the storage layer to switch (up/down) by Spin Transfer Torque (STT) effect. Reading is done by sensing different MTJ resistance states (low/high depending on the storage layer magnetization directions) owing to Tunneling Magneto-Resistance (TMR) effect. Two different MTJ resistance states represent data "1" and "0," respectively. Since MTJ has a thin tunnel barrier which can degrade owing to voltage stress, the endurance of STT-MRAM is limited by Time-dependent Dielectric Breakdown (TDDB). This is analogous to CMOS gate oxide lifetime limitation owing to TDDB.

3. Retention

Retention is the ability of an NVM device to maintain and provide on-demand the programmed state of any memory cell for a minimum period of time. In general, the capability of any NVM cell to return correct data is influenced by many factors, such as temperature, voltage and cumulative program/erase cycles, etc.

As mentioned in the Endurance section, STT-MRAM does not have charge cycling based wear-out mechanisms. However, STT-MRAM has decreasing data retention at elevated temperatures owing to temperature-dependence of magnetic anisotropy. In order to compensate for the loss of thermal stability at high temperatures, magnetic anisotropy of the devices must be increased. This in turn leads to larger write currents at lower temperatures, thus reducing the efficiency of the memory. Avalanche's proprietary pMTJ design maintains low write current/voltage without compromising data retention.

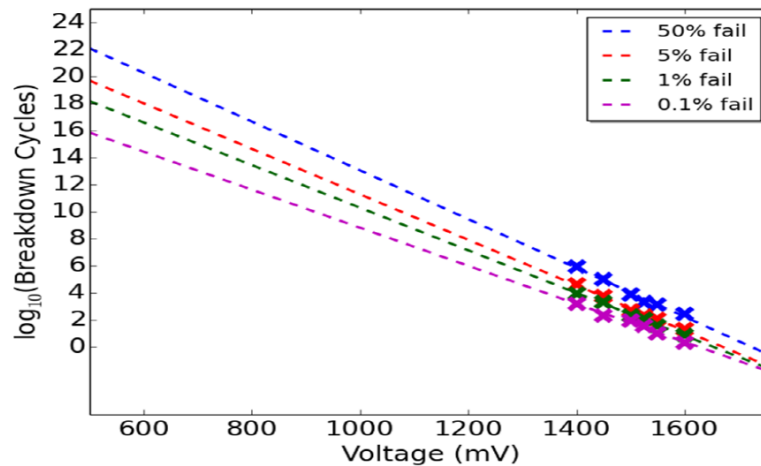
4. Field immunity

In certain applications, the memory device may potentially be exposed to stray or external magnetic field. Since MRAM stores data using magnetic moment, it is more sensitive to the magnetic field than charge based devices. Field immunity is a parameter that describes how well the MRAM works when exposed to external magnetic field. There are two types of immunity field we need to consider for MRAM. Firstly, when MRAM is exposed to the external magnetic field, the energy barrier of MRAM will be altered, which will impact the electrical switching performance of the MRAM. The maximum magnetic field under which the MRAM is still functional is called operation immunity field. Secondly, when MRAM is exposed to very high magnetic field, the magnetic field will flip the magnetic moment of the storage layer in pMTJ, which leads to loss of data in the memory. The maximum magnetic field under which the data in MRAM can be maintained without corruption is called standby immunity field. Avalanche takes into account the potential external magnetic field impact on STT-MRAM with advanced pMTJ design and circuit design. Avalanche STT-MRAM achieves the operation immunity field of up to 700 Oe and standby immunity field of up to 1000 Oe with less than sub-ppm raw error rate impact.

5. Avalanche’s STT-MRAM – Endurance, Retention, Field immunity

The **cycling endurance** of a STT-MRAM product depends on the write voltage and must be set far above the mean switching voltage to ensure a low write error rate. Figure 1 shows empirical data of Avalanche’s 64Mbit device.

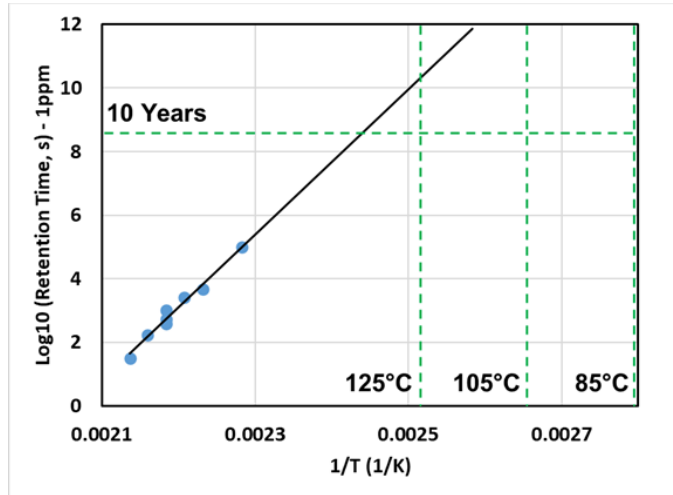
Figure 1: Typical Endurance Data for pMJT in 64Mbit device



As can be seen, with a 500mv write pulse, 1×10^{14} write cycles are achieved.

Retention is the other important characteristic in STT-MRAM, which is the length of time the data can be retained after it is written. 10 years is the industry norm for non-volatile memories. Figure 2 shows empirical data of Avalanche's 64Mbit device.

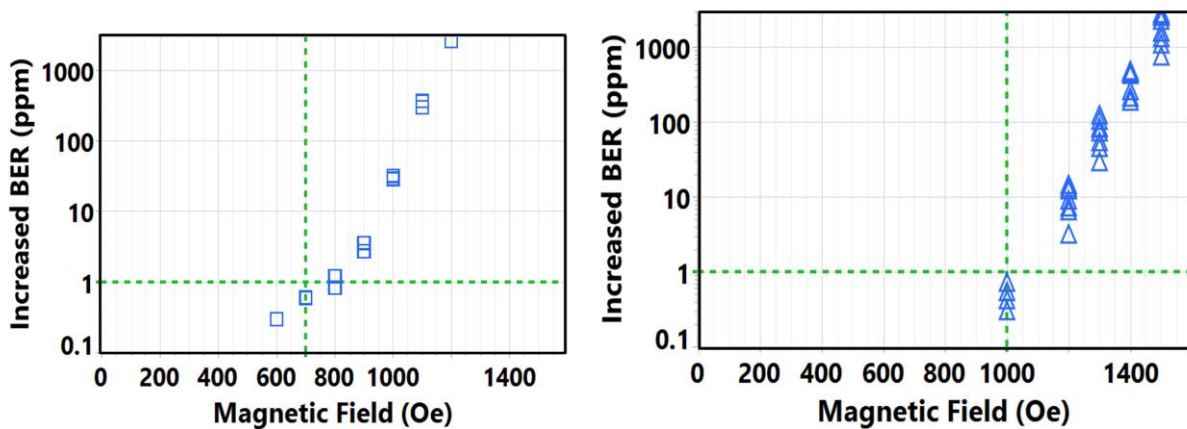
Figure 2: Typical Retention Data for pMJT in 64Mbit device



As can be seen, >10 years data retention is achieved at 125°C.

Field immunity can be characterized by testing MRAM in the presence of external magnetic field. Figure 3 shows Avalanche STT-MRAM achieves the operation immunity field of up to 700 Oe and standby immunity field of up to 1000 Oe with less than sub-ppm raw error rate impact. Duration of applied field is 1 hour in standby mode. Figure 3: Field immunity results for chip in operation (left chart) and standby (right chart) mode

Figure 3: Field immunity results for chip in operation (left chart) and standby (right chart) mode



6. Avalanche's STT-MRAM products

Avalanche offers five STT-MRAM product families which address the different use cases discussed in the following section. The product families are:

E-SRAM: E-SRAM products are embedded non-volatile true random-access memories; allowing both reads and writes to occur randomly in memory. The E-SRAM is a scratch pad memory ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance, high performance and a scalable memory technology. E-SRAM offers the industry standard AMBA 3 AHB-Lite interface.

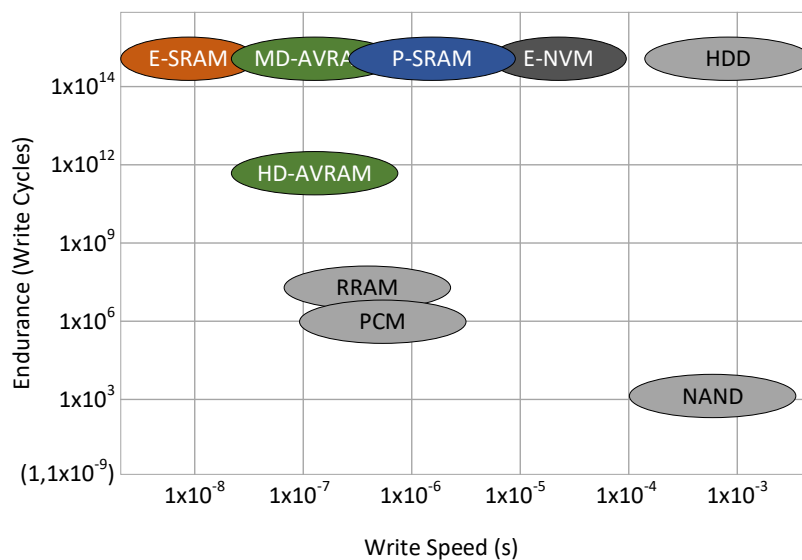
E-NVM: E-NVM products are also embedded non-volatile true random-access memories similar to E-SRAM and have a much higher temperature profile (solder reflow). The E-NVM is ideal for program and data storage. E-NVM offers the industry standard AMBA 3 AHB-Lite interface.

P-SRAM: P-SRAM products are standalone and are ideal for scratch pad applications. They offer random access, low latency, low power, infinite endurance and high performance. P-SRAMs have a SPI or Parallel interface and offer small packages.

MD-AVRAM: MD-AVRAMs are standalone, mid-density persistent RAM products build around industry leading DDR3/4 interface. MD-AVRAM are extremely high performance, provide low latency and are ideal for replacing low density DRAMs.

HD-AVRAM: HD-AVRAM products are similar to MD-AVRAM products and are currently in development built around the industry DDR4/5 standard will offer much higher densities. HD-AVRAMs have lower endurance of 1×10^{12} write cycles due to a highly scalable next generation switching mechanism.

Figure 4: Avalanche Products Overview



7. Use Models

a. Data Logging Memory (P-SRAM)

A data logger is an electronic device that records data over time via external instruments and sensors. Its primary benefit is the ability to automatically collect data. Upon activation, data loggers measure and record information for the duration of the monitoring period. A few of their critical properties are as follows:

- Data loggers have relatively slower sample rates (~1MHz).
- Data loggers are standalone devices. Memory requirements are non-volatile, large (~megabits) to accommodate several days/months of uninterrupted data acquisition.
- Data loggers are battery backed devices with solar power to supplement the power source. Power consumption must be low.
- Data loggers are extremely reliable. In other words, as long as they have power, they will not fail to log data for any reason.

Table 1: Data Logging Memory Requirements

Requirements	Read Access Time (ns)	Write Time (ns)	Frequency of Operation (MHz)	Data Endurance (Cycles)	Data Retention (Years)
Data Logging Memory	30	30	10-100	1×10^{14}	20

Avalanche's SP-NVSRAM family meets these requirements and can be used as data logger memory of choice.

Table 2: Avalanche's P-SRAM characteristics

Device Operation	Values	Units
Density range	8 – 64	Megabits
Read (Word: 32 bits)	10.0	ns
Write (Word: 32 bits)	20.0	ns
Frequency of Operation	100	MHz
Endurance	1×10^{14}	cycles
Retention	20	years
Standby	50.0	μ A
Hibernate Power Mode	1.0	μ A
Read (Word: 32 bits)	2.0	mA
Write (Word: 32 bits)	10.0	mA

b. IoT Memory (E-SRAM, E-NVM)

IoT devices are computing gadgets that connect wirelessly to a network and have the ability to transmit data. Their rapid development has created a number of exciting new opportunities and challenges for designers with one consideration that cannot be overlooked: the need for the device to have memory that can store boot code and data. Some of the must have requirements are as follows:

- **Cost.** Cost is a concern in any project; the more expensive the memory selection, the more expensive the final device.
- **Size.** Most IoT devices are small, and thus the embedded technology must also be small. The amount of space required for memory processing must also be kept to a minimum, as the more silicon wafer space required, the more costs go up.
- **Power Consumption.** Most IoT devices either run on small batteries or rely on energy harvesting for recharging. For this reason, it's important to choose an option that uses the least amount of power and voltage, both in use and during standby.
- **Startup time.** Users want excellent device performance, so memory needs to be sufficient to allow for a quick startup. Implementing a code-in-place option reduces the time required to boot up, as well as the cost of the chip since there is less need for RAM with substantial on-chip storage.

Table 3: IoT Memory Requirements

Requirements	Read Access Time (ns)	Write Time (ns)	Frequency of Operation (MHz)	Data Endurance (Cycles)	Data Retention (Years)
IoT Memory (Boot Code & Data Storage)	10	20	100	1x10 ¹⁴	10

Avalanche's E-SRAM and E-NVM families meet these requirements and can be used as IoT memory(ies) of choice.

Table 4: Avalanche's E-SRAM, E-NVM characteristics

Device Operation	E-SRAM Values	E-NVM Values	Units
Density range	8 – 64	8 – 64	Megabits
Read (Word: 32 bits)	10.0	10.0	ns
Write (Word: 32 bits)	20.0	200.0	ns
Frequency of Operation	100	100	MHz
Endurance	1x10 ¹⁴	1x10 ¹⁴	cycles
Retention	10	10	years
Standby	50.0	50.0	µA
Hibernate Power Mode	1.0	1.0	µA
Read (Word: 32 bits)	2.0	2.0	mA
Write (Word: 32 bits)	10.0	10.0	mA

c. Persistent Memory (MD-AVRAM, HD-AVRAM)

Persistent memory (PM) is simply data storage memory that does not lose data if the power fails in the system. PM storage is in the system (outside the main processor) and has worse performance than conventional DRAM. It sits in the system DIMM slots and as mentioned before, doesn't lose data upon power loss.

In the data storage hierarchy, PM is placed between DRAM and disk storage. Its performance is either similar to or slower than DRAM; it can have higher latency. PM's capacity can be larger than DRAM.

Avalanche's MD-AVRAM and HD-AVRAM families meet these requirements and can be used as persistent memory(ies) of choice.

Table 5: Avalanche's E-SRAM, E-NVM characteristics

Device Operation	MD-AVRAM Values	HD-AVRAM Values	Units
Density range	1-16	8 – 64	Gigabits
Read (Word: 32 bits)	10.0	10.0	ns
Write (Word: 32 bits)	25.0	25.0	ns
Frequency of Operation	1.60	1.60	GHz
Endurance	1x10 ¹⁴	1x10 ¹²	cycles
Retention	10	10	years
Standby	100.0	100.0	μA
Hibernate Power Mode	15.0	15.0	μA
Read (Word: 32 bits)	250.0	250.0	mA
Write (Word: 32 bits)	300.0	300.0	mA

8. Summary

Avalanche's STT-MRAM technologies exceed the requirements of most memory use cases and can be used in low power as well as high performance applications.

9. Revision History

Revision	Date	Change Summary
REV A	01/03/2019	Initial release
REV B	01/01/2020	Added Field immunity
REV C	06/01/2021	Updated with latest results