Migration from Everspin MR2xH40 to Avalanche AS3004101 Application Note

AN000013 details the feature differences when migrating from the Everspin MR2xH40 serial MRAM to Avalanche AS3004101 Serial Persistent SRAM (P-SRAM).

1. Introduction

AS3004101 is a 4Mb serial (SPI) spin-transfer torque magneto-resistive random-access memory (STT-MRAM). MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually infinite endurance and scalable non-volatile memory technology.

AS3004101 has a Serial Peripheral Interface (SPI) compatible bus interface supporting hardware/software based data protection mechanisms.

This application note provides a comparison of features that need to be taken into consideration when migrating from the Everspin MR2xH40 MRAM to the Avalanche AS3004101 MRAM.

2. Feature Comparison

The AS3004101 is a magneto resistive random access memory supporting SPI interface operating at up to 50MHz SDR. The Everspin MR2xH40 also supports single I/O SPI operation at a maximum frequency of 50 MHz SDR.

In addition to the 8-pad WSON, the AS3004204 is also available in 8-pin SOIC package. These packages are compatible with similar low-power volatile and non-volatile products. For non-automotive applications, the AS3004204 is offered over the same industrial (-40°C to 85°C), and industrial plus (-40°C to 105°C) temperature ranges as the MR2xH40.

Table 1 provides a feature comparison between the MR2xH40 and the AS3004204.

Table 1: Feature Comparison

Feature		Everspin MR2xH40	Avalanche AS3004101
Family		Serial	Serial
Technology		Toggle MRAM	STT-MRAM
Density		4Mbit, 1Mbit	4Mbit, 1Mbit
Voltage - V_{CC}		3.0 to 3.6V	2.7 to 3.6V
Interface		SPI	SPI
Bus Width		x1	x1
Mode		0,3	0,3
Frequency (MHz max)		50 (SDR)	50 (SDR)
Endurance[1]		Unlimited	10^{14}
Data Retention (yrs)		>20	>20
Temperature Range	0°C to +70°C		✓
	-40°C to +85°C	✓	✓
	-40°C to +105°C	✓	✓
	-40°C to +125°C (AEC-Q100 Grade 1)	✓	
Package	8-WSON / 8-DFN / 8-DFN Small Flag	✓	✓
	8-SOIC		✓

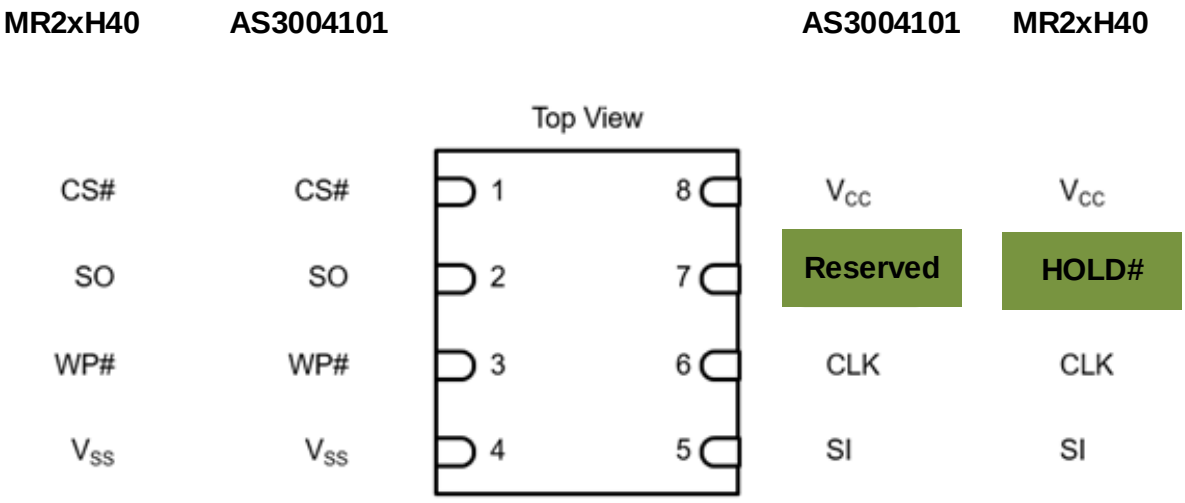
Note 1: Everspin does not list actual endurance number. MRAM devices have a finite number of write cycles. "Unlimited" is typically in reference to other non-volatile memories such as NOR or NAND with endurances of 10^5 to10^6 cycles.

3. 8-Pad WSON Pinout Comparison

The Avalanche AS3004101 is offered in two industry-standard packages: 8-pad WSON and 8-pin SOIC.

The 8-pad WSON has the same footprint as the 8-pad DFN and 8-pad DFN Small Flag the MR2xH40 is offered in. Figure 1 compares the WSON pinouts of the AS3004101 to the MR2xH40.

Figure 1: 8-WSON vs DFN/DFN Small Flag Pinout Comparison



The pinout of the AS3004101 is the same as the MR2xH40. Everspin supports the HOLD# pin which is a legacy feature not commonly used. Pin 7 is not used in AS3004101 and pulling it high or low will have no effect on the operation of this device. System designers are allowed to tie Pin 7 to Vcc.

Figure 2: WSON vs DFN/DFN Small Flag Dimension Comparison

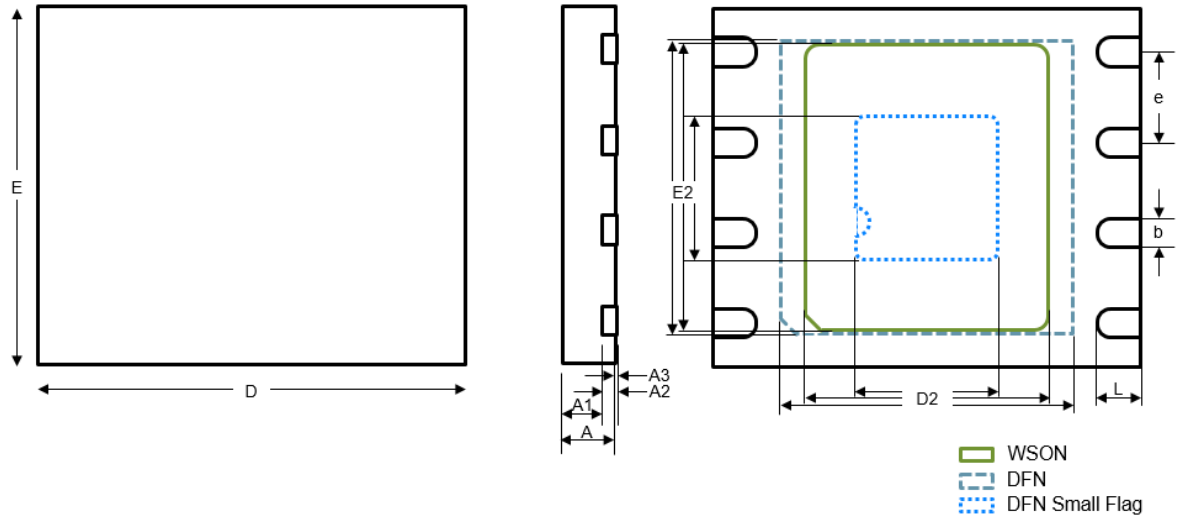


Table 2 lists the differences in dimensions of the three packages.

Table 2: Package Dimensions

Package	A	A1	A2	A3	D	E	b	D2	E2	e	L
	Thickness	Standoff	Mold Thick.	Lead Thick.	Body Width	Body Len.	Lead Width	Pad Width	Pad Len.	Lead Pitch	Lead Len.
WSON	0.75	0.02	0.55	0.2 Ref	6.00	5.00	0.40	3.40	4.00	1.27 BSC	0.60
DFN	0.95	0.025	0.747	0.203	6.00	5.00	0.40	4.10	4.10	1.27 BSC	0.60
DFN Small Flag	0.95	0.025	0.747	0.203	6.00	5.00	0.40	2.00	2.00	1.27 BSC	0.60

With a package thickness of 0.75 mm, the 8-WSON is thinner than the either DFN or DFN small Flag with a thickness of 0.95 mm. The thinner package offered by the AS3004101 is an advantage for systems with height restrictions.

The exposed pad on the bottom of the package is different for the three packages. PCB's designed for either DFN or DFN small flag will accommodate the Avalanche WSON exposed metal pad.

4. Command (Op Code) Comparison

The AS3004101 supports a superset of the commands supported by the MR2xH40. A comparison of the Op Codes is listed in Table 3.

Table 3: Op Code Comparison

Instruction Name	Op Code		MR2xH40	AS3004101	Comment
Write Enable	WREN	06h	✓	✓	
Write Disable	WRDI	04h	✓	✓	
Read Status Register	RDSR	05h	✓	✓	
Write Status Register	WRSR	01h	✓	✓	
Read Memory	READ	03h	✓	✓	
Write Memory	WRTE	02h	✓	✓	
Enter Sleep Mode	DPDE	B9h	✓	✓	
Exit Sleep Mode	DPDX	ABh	✓	✓	
Read Device ID	RDID	9Fh	-	✓	Everspin does not support this function

5. Registers

The AS3004101 provides a superset of registers to access features not supported by the MR2xH40. A comparison of the AS3004101 and the MR2xH40 registers is listed in Table 4

Table 4: Register Comparison

Register Name	MR2xH40	AS3004101	Comment
Status Register	✓	✓	
Device Identification Register	-	✓	Everspin does not support this register

The Status Register functions for the AS3004101 and the MR2xH40 are the same for bits SR[0], SR[1], SR[2], SR[3] and SR7. The AS3004101 uses SR[4]-SR[5] to provide additional features not supported by the MR2xH40. Table 5 lists the Status Register bit definition for the AS3004101 and MR2xH40.

Note: The AS3004101 additional features are set after the device has boot-up. The default state of the status registers are same for both the AS3004101 and MR2xH40. See *Table 6: Status Register – Default State Comparison*.

Table 5: Status Register – Bit Definition Comparison

Bits	MR2xH40	AS3004101	Comment
SR[7]	SRWD	WP#EN	Hardware based WP# Protection Enable/Disable. 1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low **Functionally the same**.
SR[6]	Do Not Care	Reserved	
SR[5]	Do Not Care	TBSEL	Software Top/Bottom Memory Array Protection Selection. 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range) **Note: Everspin only supports Top Block.**
SR[4]	Do Not Care	BPSEL[2]	High order Block Protection Bit provides additional memory array protection areas. **Note: Not supported by Everspin. Refer to 6. Block Protection Configuration for more detail.**
SR[3]	BP1	BPSEL[1]	Block Protection Bits
SR[2]	BP0	BPSEL[0]	Block Protection Bits
SR[1]	WEL	WREN	Write Operation Protection Enable/Disable. 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled **Functionally the same.**
SR[0]	Do Not Care	RSVD	'Reserved for future use' on Avalanche**.** **Functionally the same.**

The Status Register default setting on boot up for both the AS3004101 and the MR2xH40 is 00h. This means that both parts are initiated in the same state with regard to write protection which is disabled for the Status Register and the memory array and Top Protection selected. The Serial Number write protection feature SR[6] is not a concern as the Serial Number feature is not supported on the MR2xH40 (e.g. do not care).

Table 6: Status Register – Default State Comparison

Bits	MR2xH40	AS3004101	Comment
SR[7]	0	0	Everspin: Protection Disabled – Doesn't write protect when WP# is Low Avalanche: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	0	0	Everspin: Function not supported Avalanche: Reserved
SR[5]	0	0	Everspin: Only Supports Top Protection Avalanche: Top Protection Enabled (Higher Address Range)
SR[4]	0	0	Everspin: All Blocks Unprotected Avalanche: All Blocks Unprotected
SR[3]	0	0	
SR[2]	0	0	
SR[1]	0	0	Everspin: Write Operation Protection Enabled Avalanche: Write Operation Protection Enabled
SR[0]	0	0	Everspin: N/A Avalanche: N/A

6. Block Protection Configuration

The AS3004101 provides four additional sizes for protecting the memory array in comparison to the MR2xH40. To support this, the AS3004101 uses an extra bit in the Status Register SR[4] as BLSEL[2] as the high-order Block Protection Bit. BPSEL[2] on Avalanche device must be set appropriately to match Everspin configuration. Table 7 compares the Block Protection for the AS3004101 and the MR2xH40.

Table 7: Block Protection Comparison

Block	**MR2xH40**		**AS3004101**		
Protected	BP1	BP0	BPSEL[2]	BPSEL[1]	BPSEL[0]
None	0	0	0	0	0
Upper 1/64	Not Supported		0	0	1
Upper 1/32	Not Supported		0	1	0
Upper 1/16	Not Supported		0	1	1
Upper 1/8	Not Supported		1	0	0
Upper 1/4	0	1	1	0	1
Upper 1/2	1	0	1	1	0
All	1	1	1	1	1

7. DC Parameters

Table 8 compares the DC Parameters for the MR2xH40 and AS3004204. For most parameters the Avalanche AS3004204 provides an advantage over the MR2xH40.

Table 8: DC Parameter Comparison

Parameter	Symbol	MR2xH40	AS3004101	Comments
Supply Voltage	V_{CC}	3.0V to 3.6V	2.7V to 3.6V	
Read Current (1-1-1)	I_{READ1}	13.8 mA @50MHz	8 mA @50MHz	
Write Current (1-1-1)	I_{WRITE1}	33 mA @50MHz	14 mA @50MHz	
Standby Current[1]	I_{SB}	90 µA	160 µA	
Deep Power Down[1]	I_{DPD}	15 µA	5 µA	
Input High Voltage	V_{IH}	2.2V to V_{CC}+0.3	0.7xV_{CC} to V_{CC}+0.3	Avalanche supports lower V_{IH} (min) of 2.1V @ 3.0V V_{CC}
Input Low Voltage	V_{IL}	-0.5V to 0.8V	-0.3V to 0.3xV_{CC}	Avalanche supports higher V_{IL} (max) of 0.9V @ 3.0V V_{CC}. Voltage swings cannot go below V_{IL} (min) of -0.3V for Avalanche
Output High Voltage Level	V_{OH}	V_{CC}-0.2V (min) I_{OH}=-100 µA 2.4V (min) I_{OH} = -4 mA	V_{CC}-0.2V (min) I_{OH}=-100 µA 2.4V (min) I_{OH} = -1 mA	No change required. Note: V_{OH} must remain within logic levels for inputs on heavily loaded system buses
Output Low Voltage Level	V_{OL}	V_{SS}+0.2V (max), I_{OL}=100 µA 0.4V (max) I_{OL} = 4 mA;	0.2V (max), I_{OL}=150 µA 0.4V (max) I_{OL} = 2 mA;	No change required. Note: V_{OL} must remain within logic levels for inputs on heavily loaded system buses
Magnetic Field During Write	H_{max_write}	12,000 A/m	24,000 A/m	Avalanche has a higher magnetic immunity
Magnetic Field During Read	H_{max_read}	12,000 A/m	24,000 A/m	Avalanche has a higher magnetic immunity

8. AC Parameters

Table 9 compares selected AC Parameters for the MR2xH40 and AS3004204. The Avalanche AS3004204 provides equivalent or better timing than the MR2xH40.

Table 9: AC Parameter Comparison

Parameter	Symbol	MR2xH40	AS3004204	Comments
Deep Power Down Entry Time	t_{EDPD}	3 µs (min)	3 µs (min)	
Deep Power Down Exit Time	t_{EXDPD}	400 µs (min)	400 µs (min)	
Output Disable Time (w.r.t. CS#)	t_{HZCS}	12 ns (min)	7.0 ns (max)	Avalanche specifies this parameter as a Maximum while Everspin specifies a Minimum. Avalanche device ensures the bus is available after 7ns while the Everspin device releases the output sometime after 12ns.

9. Power-Up and Power-Down Behavior

Figure 3 and Figure 4 depict the Power-Up and Power-Down behavior. The AS3004204 provides a shorter Power-Up to first instruction time than the MR2xH40.

Figure 3: Power-Up Behavior

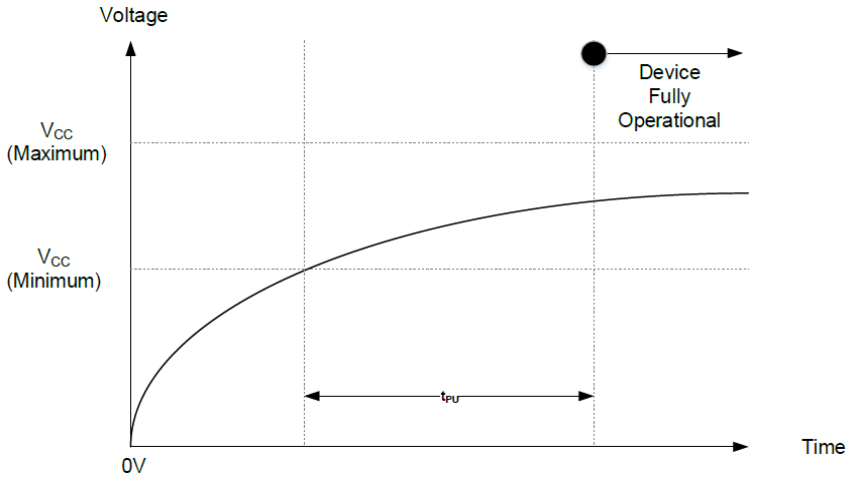


Figure 4: Power-Down Behavior

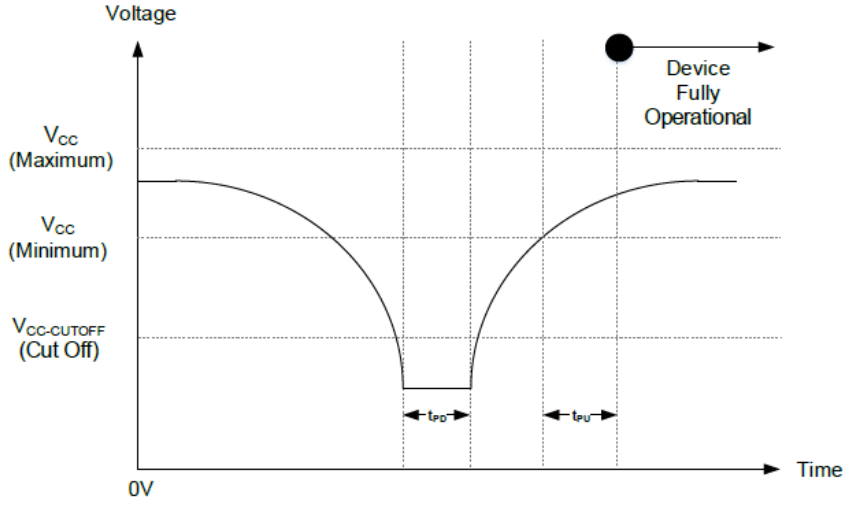


Table 10: Power-Up and Power-Down Comparison

Parameter	Symbol	MR2xH40	AS3004204	Comment
V_{CC} Power Up to First Instruction	t_{PU}	400 µs (min)	250 µs (min)	Avalanche power-up time is shorter
V_{CC} Ramp Up Time	R_{VR}	Not Listed	30 µs/V (min)	
V_{CC} Ramp Down Time	R_{VF}	Not Listed	20 µs/V (min)	

10. Summary

The features of the AS3004204 provide system designers a straightforward migration path from the MR2xH420 at the same system performance for read and write operations with lower power consumption.

11. Revision History

Revision	Date	Change Summary
REV A	09/22/2020	Initial release
REV B	06/10/2021	Updated information allowing customers to tie Pin 7: (HOLD) to Vcc or Vss