Migration from Cypress CY15B104Q to Avalanche AS3004101 Application Note

AN000015 details the feature differences when migrating from the Cypress CY15B104Q serial FRAM to Avalanche AS3004101 Serial (SPI) Persistent SRAM (P-SRAM).

1. Introduction

AS3004101 is a 4-Mbit serial spin-transfer torque magneto-resistive random-access memory (STT-MRAM). MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile.

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

AS3004101 has a Serial Peripheral Interface (SPI) compatible bus interface supporting hardware/software based data protection mechanisms.

This application note provides a comparison of features that need to be taken into consideration when migrating from the Cypress CY15B104Q FRAM to the Avalanche AS3004101 MRAM.

2. Feature Comparison

The AS3004101 is a serial interface memory device supporting x1 SPI interface operating at up to 50MHz SDR. In contrast, the Cypress CY15B104Q only supports single I/O operation at a maximum frequency of 40 MHz SDR. As a result, the Avalanche AS3004101 offers higher performance, functionality, endurance and data retention compared with the Cypress device.

The AS3004101 is available in 8-pin SOIC and 8-pad WSON. These packages are compatible with similar low-power volatile and non-volatile products.

Table 1 provides a feature comparison between the CY15B104Q and the AS1004204.

Table 1: Feature Comparison

Feature		Cypress CY15B104Q	Avalanche AS3004101
Family		Serial	Serial
Technology		FRAM	STT-MRAM
Density		4Mbit	4Mbit
Voltage - V_{CC}		2.0V to 3.6V	2.70 to 3.6V[1]
Interface		SPI	SPI
Bus Width		x1	x1
Mode		0,3	0,3
Frequency (MHz max)		40 (SDR)	50 (SDR)
Endurance		10^{14} (read-write endurance, F-RAM technology suffers from destructive read where read instructions are followed by write instructions – transparent to the system -- to maintain data integrity)	10^{14} (write endurance)
Data Retention (yrs)		10	>20
F	-40°C to +85°C	✓	✓
	-40°C to +105°C		✓
Package	8-SOIC	✓	✓
	8-WSON, 8-Pad DFN	✓	✓
	24-BGA		✓

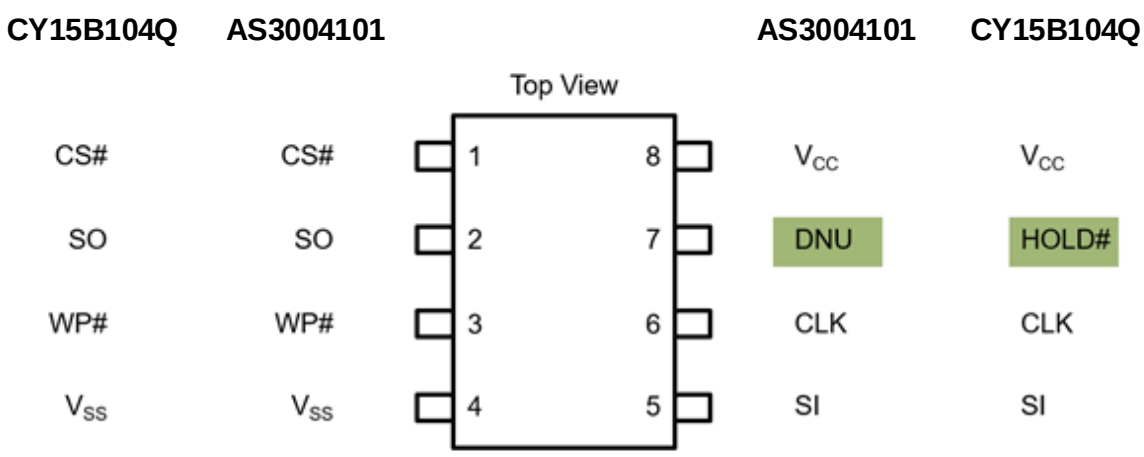
1. The Avalanche AS3004101 supports 1.8V operation and can be configured to operate in x1 SPI mode upon boot up.

3. 8-Pin SOIC Pinout Comparison

The Avalanche AS3004101 is offered in two industry-standard packages: 8-pin SOIC and 8-pad WSON.

The 8-pin SOIC and 8-pad WSON have the same footprint as the CY15B104Q. Figure 1 compares the WSON pinouts of the AS3004101 to the CY15B104Q.

Figure 1: 8-pin SOIC Pinout Comparison



In the Avalanche AS3004101, the pinout of the AS3004101 is the same as the CY15B104Q. Cypress supports the HOLD# pin which is a legacy feature not commonly used.

Figure 2: SOIC Dimension Comparison

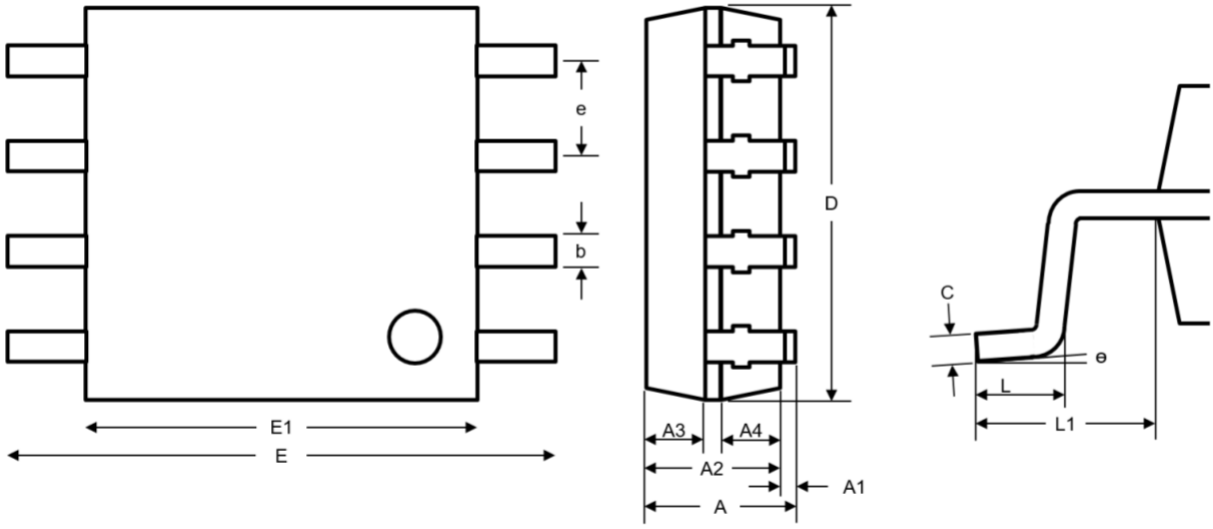


Table 2 lists the differences in dimensions of the SOIC packages.

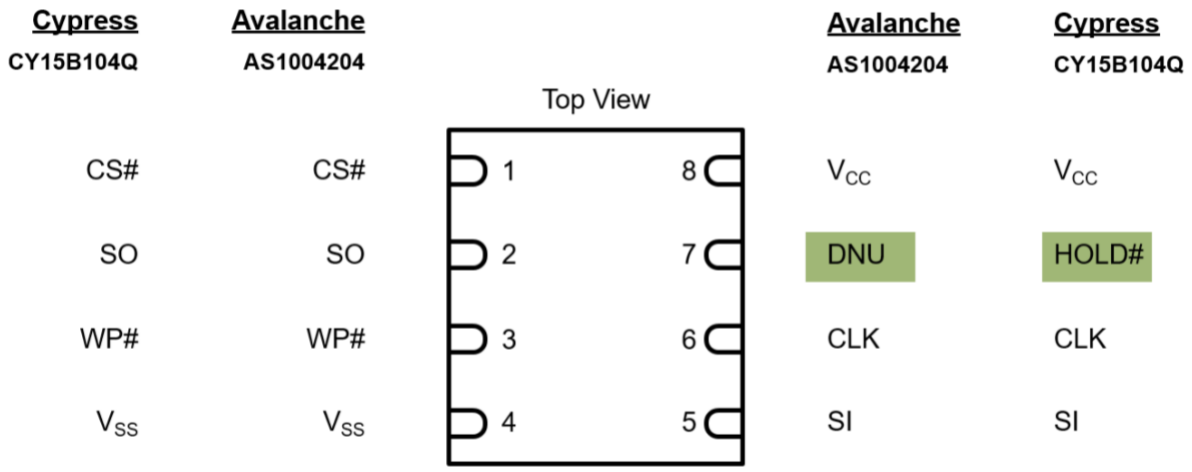
Table 2: SOIC Package Dimensions (Typical Values)

Package	A	A1	A2	A3	A4	D	E	E1	b	e	L	L1	C	ɵ
Avalanche	2.16 (max)	0.15	1.80	0.798	0.798	5.23	7.90	5.28	0.41	1.27 BSC	0.65	1.37	0.20	5°
Cypress	2.03 (max)	0.15	1.84	0.810	0.810	5.23	8.01	5.28	0.42	1.27 BSC	0.635	1.363	0.25	4°

NL = Not Listed

The 8-pad WSON has the same footprint as the 8-pad DFN the CY15B104Q is offered in. Figure 3 compares the WSON pinouts of the AS3004101 to the CY15B104Q.

Figure 3: WSON vs DFN Pinout Comparison



In the Avalanche default setting, x1 SPI Mode, the pinout of the AS3004101 is the same as the CY15B104Q. Cypress supports the HOLD# pin which is a legacy feature not commonly used. For the AS1004204, it is recommended to tie Pin 7 to V_{CC} (do not leave pin floating).

Figure 4: WSON vs DFN Dimension Comparison

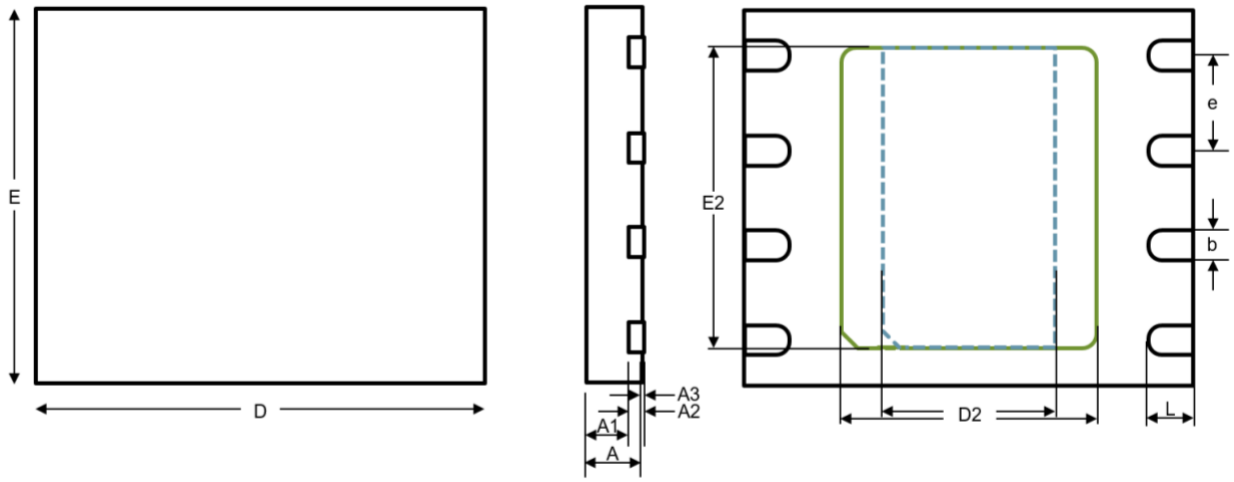


Table 3 lists the differences in dimensions between the WSON and DFN packages.

Table 3: WSON vs DFN Package Dimensions (Typical Values)

Package	A Thickness	A1 Mold Thick.	A2 Lead Thick.	A3 Stand off	D Body Width	E Body Len.	b Lead Width	D2 Pad Width	E2 Pad Len.	e Lead Pitch	L Lead Len.
WSON	0.75	0.55	0.2 Ref	0.02	6.00	5.00	0.40	3.4	4.0	1.27 BSC	0.60
DFN	0.75	0.547	0.203	0.025	6.00	5.00	0.40	2.3	4.0	1.27 BSC	0.60

4. Command (Op Code) Comparison

The AS3004101 supports a superset of the commands supported by the CY15B104Q. A comparison of the AS3004101 and the CY15B104Q Op Codes is listed in Table 4.

Table 4: Op Code Comparison

Instruction Name	Op Code		CY15B104Q	AS3004101	Comment
Write Status Register	WRSR	01h	✓	✓	
Write Data Bytes	WRITE	02h	✓	✓	
Read Data Bytes	READ	03h	✓	✓	
Write Disable	WRDI	04h	✓	✓	
Read Status Register	RDSR	05h	✓	✓	
Write Enable	WREN	06h	✓	✓	
Fast Read	FR	0Bh	✓		AS1004101 does not support Fast Read
Read Device ID	RDID	9Fh	✓	✓	
Exit Deep-Power Down	DPDX	ABh	-	✓	Avalanche provides options for user to exit DPD using either command opcode or driving CS# high
Enter Deep-Power Down	DPDE	B9h	✓	✓	

5. Read Device ID

Executing command op code 9Fh, Read Device ID, will return information about the device. The AS3004101 will return 4-bytes of information while the CY15B104Q returns 9-bytes of information. The format of the Read Device ID output is listed in Table 5: CY15B104Q Read ID Output and Table 6: AS3004101 Read ID Output.

Table 5: CY15B104Q Read ID Output

Manufacturer ID ID[71:16]	Product ID				
	Family ID[15-13]	Density ID[12-8]	Sub ID[7-6]	Rev ID[5-3]	Rsvd ID[2-0]
01111111011111110111111110111 11110111111101111111111000010	001	00110	00	001	000
7F7F7F7F7F7FC2h	2608h				

Table 6: AS3004101 Read ID Output

Manufacturer ID ID[31:24]	Device Configuration				
	Interface ID[23:20]	Voltage ID[19:16]	Temp ID[15:12]	Density ID[11:8]	Frequency ID[7:0]
1110 0110	0001 – SPI	0001 – 3V	0000 - -40ºC- 85ºC 0001 - -40ºC- 105ºC	0010 - 4Mb	0110 - 50MHz
E6h	01h	01h	00h or 01h	02h	06h

6. Registers

The AS3004101 provides a superset of registers to access features not supported by the CY15B104Q. A comparison of the AS3004101 and the CY15B104Q registers is listed in Table 7.

Table 7: Register Comparison

Register Name	CY15B104Q	AS3004101	Comment
Status Register	✓	✓	
Device Identification Register	✓	✓	

The Status Register functions for the AS3004101 and the CY15B104Q are the same for bits SR[0], SR[1], SR[2], SR[3] and SR[7]. The AS3004101 uses SR[4]-SR[5] to provide additional features not supported by the CY15B104Q. Table 8 lists the Status Register bit definition for the AS3004101 and CY15B104Q.

Note: The AS3004101 additional features are set after the device has boot-up. The default state of the status registers are same for both the AS3004101 and CY15B104Q. See *Table 9: Status Register – Default State Comparison*.

Table 8: Status Register – Bit Definition Comparison

Bits	CY15B104Q	AS3004101	Comment
SR[7]	WPEN	WP#EN	Hardware based WP# Protection Enable/Disable. 1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low **Functionally the same**.
SR[6]	Do Not Care	Reserved	Reserved
SR[5]	Do Not Care	TBSEL	Software Top/Bottom Memory Array Protection Selection. 1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range) **Note: Cypress only supports Top Block.**
SR[4]	Do Not Care	BPSEL[2]	High order Block Protection Bit provides additional memory array protection areas. **Note: Not supported by Cypress. Refer to 6. Block Protection Configuration for more detail.**
SR[3]	BP1	BPSEL[1]	Block Protection Bits
SR[2]	BP0	BPSEL[0]	Block Protection Bits
SR[1]	WEL	WREN	Write Operation Protection Enable/Disable. 1: Write Operation Protection Disabled 0: Write Operation Protection Enabled **Functionally the same.**
SR[0]	0	RSVD	'Reserved for future use' on Avalanche**.** **Functionally the same.**

The Status Register default setting on boot is 00H for the AS3004101 and 40H for the CY15B104Q. This means that both parts are initiated in the same state with Top Protection and write protection disabled for both the Status Register and the memory array.

Table 9: Status Register – Default State Comparison

Bits	CY15B104Q	AS3004101	Comment
SR[7]	0	0	Cypress: Protection Disabled – Doesn't write protect when WP# is Low Avalanche: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	1	0	Cypress: Function not supported Avalanche: Reserved
SR[5]	0	0	Cypress: Only Supports Top Protection Avalanche: Top Protection Enabled (Higher Address Range)
SR[4]	0	0	Cypress: All Blocks Unprotected Avalanche: All Blocks Unprotected
SR[3]	0	0	
SR[2]	0	0	
SR[1]	0	0	Cypress: Write Operation Protection Enabled Avalanche: Write Operation Protection Enabled
SR[0]	0	0	Cypress: N/A Avalanche: N/A

7. Block Protection Configuration

The AS3004101 provides four additional sizes for protecting the memory array in comparison to the CY15B104Q. To support this, the AS3004101 uses an extra bit in the Status Register SR[4] for BLSEL[2] as the high-order Block Protection Bit. BPSEL[2] on the Avalanche device must be set appropriately to match the Cypress configuration. Table 10 compares the Block Protection for the AS3004101 and the CY15B104Q.

Table 10: Block Protection Comparison

Block	CY15B104Q		AS3004101		
Protected	BP1	BP0	BPSEL[2]	BPSEL[1]	BPSEL[0]
None	0	0	0	0	0
Upper 1/64	Not Supported		0	0	1
Upper 1/32	Not Supported		0	1	0
Upper 1/16	Not Supported		0	1	1
Upper 1/8	Not Supported		1	0	0
Upper 1/4	0	1	1	0	1
Upper 1/2	1	0	1	1	0
All	1	1	1	1	1

8. DC Parameters

Table 11 compares the DC Parameters for the CY15B104Q and AS3004101. For most parameters, the Avalanche AS3004101 provides an advantage over the CY15B104Q.

Table 11: DC Parameter Comparison

Parameter	Symbol	CY15B104Q	AS3004101	Comments
Supply Voltage	V_{CC}	2.0V to 3.6V	2.70V to 3.6V[1]	
Read Current (1-1-1) SDR	I_{READ1}	1.4 mA @40MHz	8 mA @50MHz	
Write Current (1-1-1) SDR	I_{WRITE1}	1.4 mA @40MHz	14 mA @50MHz	
Standby Current	I_{SB}	100 µA	120 µA	
Deep Power Down	I_{DPD}	3 µA	5 µA	
Input High Voltage	V_{IH}	0.7xV_{CC} to V_{CC}+0.3	0.7xV_{CC} to V_{CC}+0.3	
Input Low Voltage	V_{IL}	-0.3V to 0.3xV_{CC}	-0.3V to 0.3xV_{CC}	
Output High Voltage Level	V_{OH}	V_{CC}-0.2V (min) I_{OH}= -100 µA V_{CC}-2.4V (min) I_{OH}= -1 mA	V_{CC}-0.2V (min) I_{OH}=-100 µA 2.4V (min) I_{OH} = -1 mA	
Output Low Voltage Level	V_{OL}	0.2V (max), I_{OL}=150 µA 0.4V (max) I_{OL} = 2 mA;	0.2V (max), I_{OL}=150 µA 0.4V (max) I_{OL} = 2 mA;	

2. The Avalanche AS3004101 supports 1.71V to 2.0V.

9. AC Parameters

Table 12 compares selected AC Parameters for the CY15B104Q and AS3004101. The Avalanche AS3004101 provides equivalent or better timing than the CY15B104Q.

Table 12: AC Parameter Comparison

Parameter	Symbol	CY15B104Q	AS3004101	Comments
Deep Power Down Entry Time	t_{EDPD}	Not Listed	3 µs (max)	
Deep Power Down Exit Time	t_{EXDPD}	450 µs (max)	400 µs (max)	Avalanche has a faster recovery time.
Output Disable Time (w.r.t. CS#)	t_{HZCS}	20 ns (max)	7.0 ns (max)	Avalanche device ensures the bus is available after 7ns while the Cypress device releases the output after 20ns.

10. Power-Up and Power-Down Behavior

Figure 5 and Figure 6 depict the Power-Up and Power-Down behavior. The AS3004101 provides a shorter Power-Up to first instruction time than the CY15B104Q.

Figure 5: Power-Up Behavior

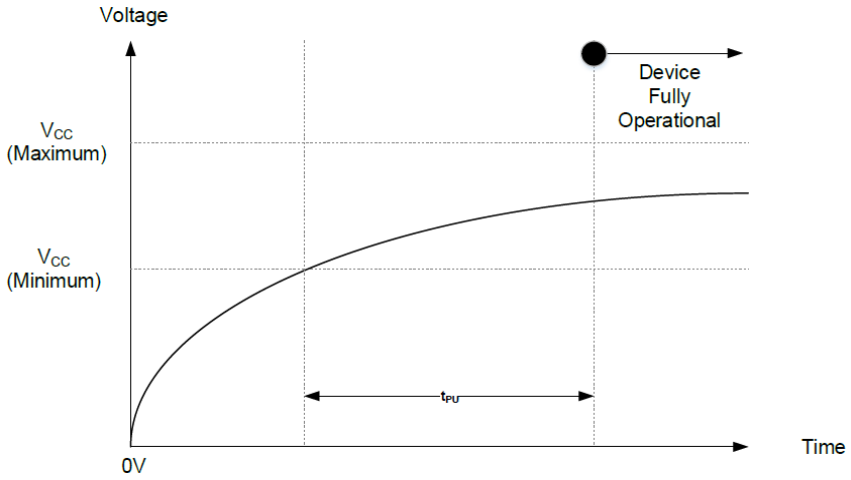


Figure 6: Power-Down Behavior

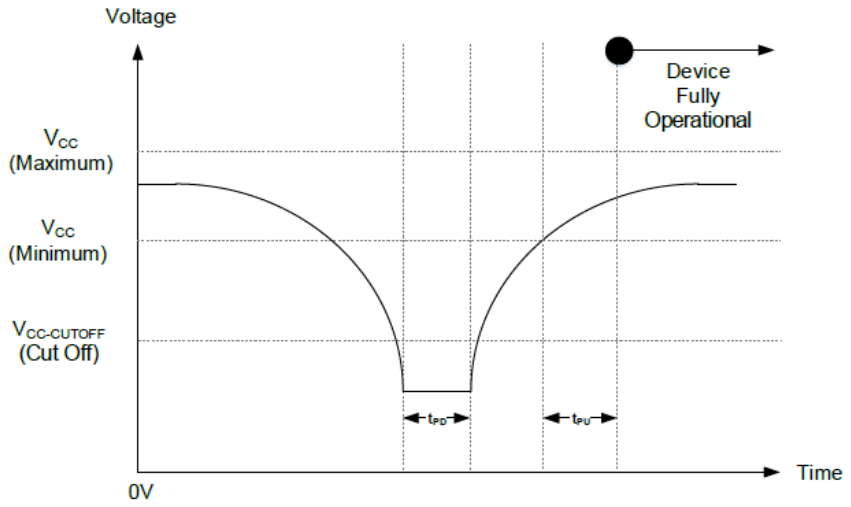


Table 13: Power-Up and Power-Down Comparison

Parameter	Symbol	CY15B104Q	AS3004101	Comment
V_{CC} Power Up to First Instruction	t_{PU}	1000 µs (min)	250 µs (min)	Avalanche supports a shorter power-up time
V_{CC} Ramp Up Time	R_{VR}	50 µs/V (min)	30 µs/V (min)	Avalanche device permits a slower ramp-up time versus Cypress
V_{CC} Ramp Down Time	R_{VF}	100 µs/V (min)	20 µs/V (min)	Avalanche device permits a slower ramp-down time versus Cypress

11. Summary

The features of the AS3004101 provide system designers a straightforward migration path from the CY15B104Q while also providing higher in-system performance for read and write operations.

10. Revision History

Revision	Date	Change Summary
REV A	09/22/2020	Initial release