Migration from Cypress CY14B104NA-BA45XI nvSRAM to Avalanche AS3004316

AN000016 details the feature differences when migrating from the Cypress CY14B104NA-BA45XI nvSRAM to Avalanche AS3004316 Persistent SRAM (P-SRAM).

1. Introduction

AS3004316 is a 4Mb magneto-resistive random-access memory (MRAM). MRAM technology is analogous to Flash technology with SRAM compatible 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution.

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually unlimited endurance and data retention, high performance and scalable memory technology.

AS304316 is available in small footprint 48-Ball FBGA (10mm x 10mm) packages. These packages are compatible with similar low-power volatile and non-volatile products.

AS3004316 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

This application note provides a comparison of features that need to be taken into consideration when migrating from the Cypress nvSRAM to the Avalanche P-SRAM.

2. Feature Comparison

The AS3004316 is a standard asynchronous SRAM parallel interface STT-MRAM memory device. Every write into the P-SRAM is non-volatile with data retention exceeding 20 years. There is no data transfer from an SRAM into a low endurance/low speed non-volatile memory, no capacitors or back up batteries are needed and system design and SW implementation is simplified and reliability is dramatically improved. Additionally, higher density memories are available if needed to upgrade the system without major PCB redesign.

Table 1 provides a feature comparison between the MR10Q010 and the AS3001204.

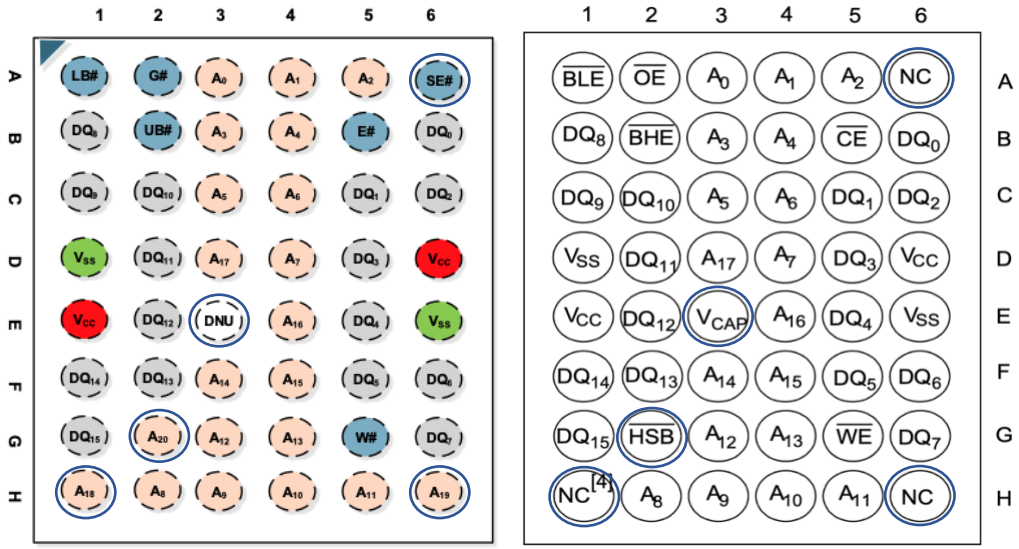
Table 1: Feature Comparison

Feature		Cypress CY14B104NA-BA45xI	Avalanche AS3001204
Family		Parallel	Parallel
Technology		nvSRAM	STT-MRAM
Density		1Mb, 4Mb, 8Mb, 16Mb	1Mb, 4Mb, 8Mb, 16Mb, 32Mb
Voltage - V_{CC}		2.7V to 3.6V	2.7V to 3.6V
Interface		Standard Asynchronous SRAM Parallel	Standard Asynchronous SRAM Parallel
Bus Width		x16	x16
Performance		45ns	45ns
Endurance		1000000 store operations or power cycles	10^{14} write operations
Data Retention (yrs)		20	>20
Operating Temperature	-40°C to +85°C	✓	✓
	-40°C to +105°C	✓	✓
Package	FBGA48	6 x 10 (Body) 3.75 x 5.25 (Ball Array)	10 x 10 (Body) 3.75 x 5.25 (Ball Array)

3. Pinout Comparison

Referring to the pinouts in the device data sheets we notice that they are similar, however, different functionality for five balls needs to be addressed.

Figure 1: 48-Ball BGA Pinout Comparison (Avalanche AS3004316 on the left and CY14B104NA-BA on the right)



- Ball **A6** is SE# (sleep enable) on the Avalanche device where-as it is NC on the Cypress device. Customers not using the sleep functionality of the Avalanche P-SRAM can connect the pin to Vcc or leave it floating (the device has a weak pull-up on this pin).
- Ball **E3** is DNU on the Avalanche device where-as it is VCAP on the Cypress device. Customers migrating from Cypress nvSRAM to the Avalanche P-SRAM can leave this pin NC by depopulating the capacitor.
- Ball **G2** is ADDR[20] on the Avalanche device and HSB# on the Cypress device. Customers migrating from nvSRAM to P-SRAM should leave this pin NC.
- Balls **H1** and **H6** are ADDR[18] and ADDR[19] on the Avalanche device and NC on the Cypress device. Customers migrating to the P-SRAM should leave these balls NC.

4. Package Comparison

The main difference in the packages is that the body size of the Avalanche package is 10x10 where-as it is 6x10 for the Cypress package. Customers desiring to migrate from the nvSRAM to the P-SRAM must ensure that the board has the required mechanical keep out to accommodate the Avalanche package. The solder balls on the Avalanche package are laid out in a 6x8 grid that is a drop-in replacement for the Cypress package solder ball 6x8 grid.

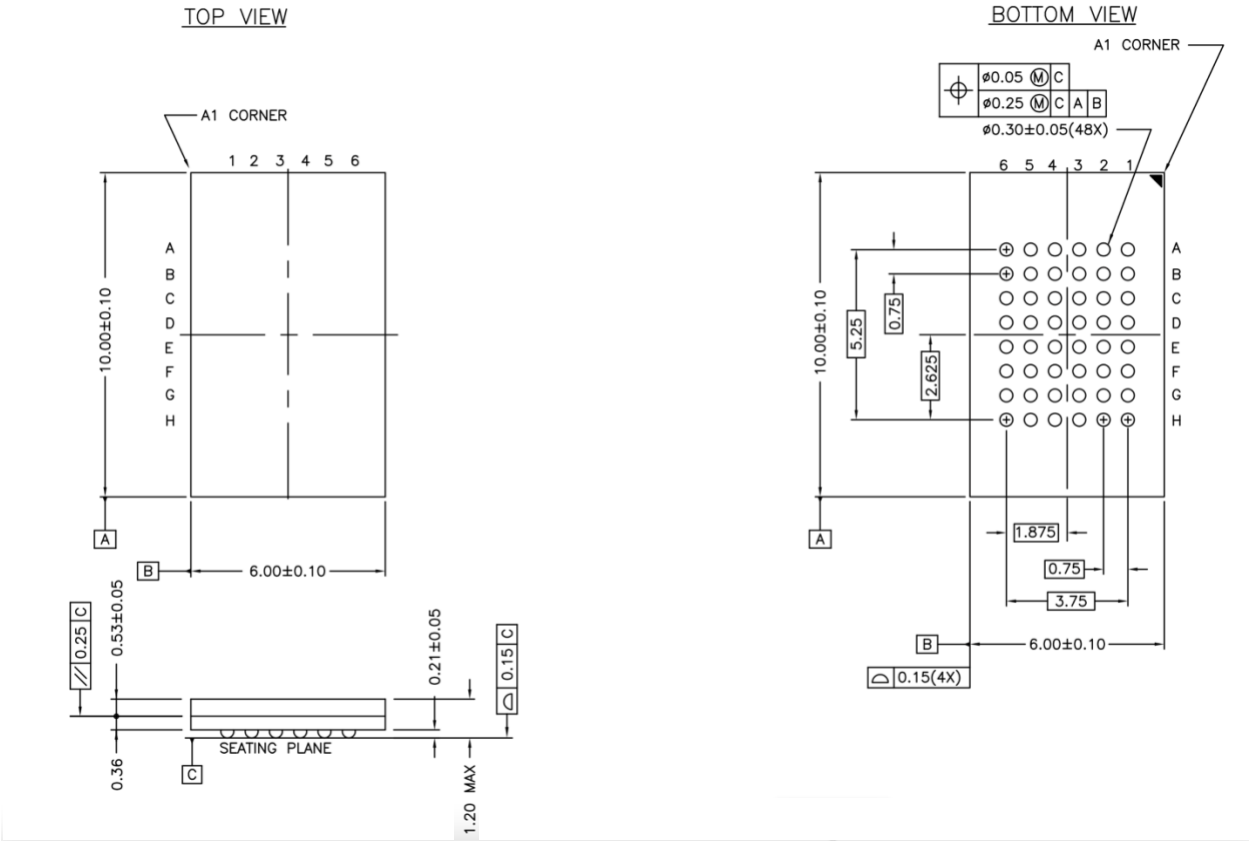


Figure 2: 48-Ball FBGA Package from Cypress

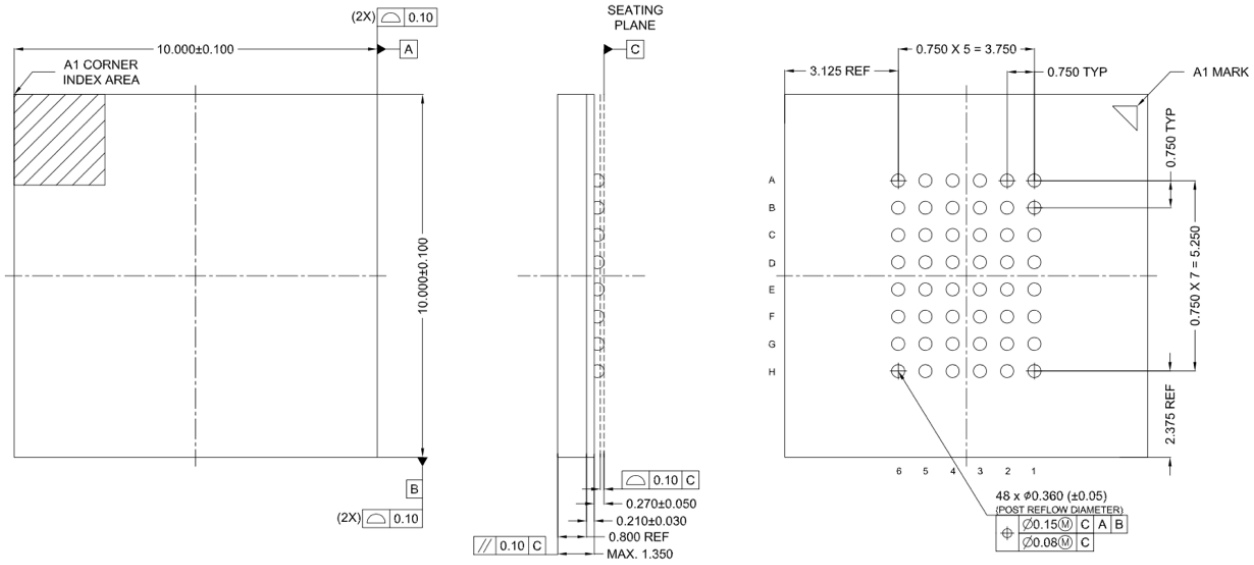


Figure 3: 48-Ball FBGA Package from Avalanche

5. DC Parameters Comparison

A comparison of DC parameters shows that the devices only differ in I_{CC} (read/write) and I_{SB}. The Avalanche P-SRAM device requires an I_{CC} and I_{SB} that is significantly lower than that required by the Cypress nvSRAM device. Customers can confidently replace the nvSRAM with P-SRAM devices without worrying about DC parameter incompatibility.

6. AC Parameters

Both Avalanche P-SRAM and nvSRAM have standard, compatible asynchronous SRAM timing. With a 45 ns read/write cycle time, the Avalanche P-SRAM is compatible with similar nvSRAM speed grade options.

It is important to note that the Avalanche P-SRAM requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (see T_{WHAX} and T_{EHAX} in the data sheet). Most microprocessors can accommodate this Hold time.

7. Simplified Power-Up and Power-Down Behavior

Both P-SRAM and nvSRAM operate from standard 3.3V power supplies. However, data written into the P-SRAM is inherently non-volatile unlike the nvSRAM. This difference imposes limitations on the power cycling behavior of the nvSRAM – it must stay up longer to complete the auto store operation and it takes longer to become available after power is restored to load the data from the non-volatile storage into the SRAM of the nvSRAM. Additionally, due to the lower write endurance of the non-volatile storage element the nvSRAM cannot be duty cycle power controlled to manage overall power consumption. These limitations are removed when customers migrate from nvSRAM to P-SRAM.

8. Summary

The Avalanche AS3004316 provides system designers a straightforward migration path from the CY14B104NA-BA45XI.

10. Revision History

Revision	Date	Change Summary
REV A	01/22/2021	Initial release