AS3xxx332 Reference Design Utilizing Lattice MachX03 FPGA Platform Application Note

AN000018 provides basis functional operation of the Avalanche ASxxx332 P-SRAM Parallel x32 devices and several key SRAM board design considerations.

1. Introduction

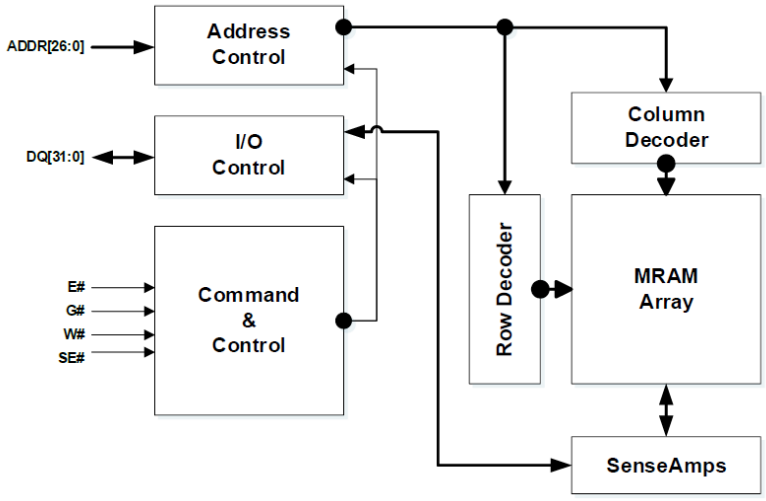
The AS3xxx332 is a high-speed asynchronous SRAM with densities offered in 1Gb and 4Gb, organizing in 32K bytes x 32 bits and 128K bytes x 32 bits respectively. The scalarly advanced 22nm STT-MRAM technology coupled with innovative circuit design provide low latency, high performance, and very reliable non-volatile memory solution. The Avalanche's 3rd Generation P-SRAM is ideal for Defense and Aerospace applications.

Memory access is controlled by Chip Enable (E#), Output Enable (G#) and Write Enable (W#).

To write to the device, drive Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[31]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[24]).

To read from the device, drive Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[24]) to appear on I/O pins (DQ[0] to DQ[31]).

Figure 1: Functional Block Diagram



Signal Description

Table 1: Signal Description

Signal	Type	Description
E#	Input	**Chip Enable:** Enables or disables the MRAM.
G#	Input	**Output Enable:** Enables the output drivers for data transfer I/Os.
W#	Input	**Write Enable:** Transfers serial data from the host system to the MRAM when Low (Logic '0'). Transfers serial data from the MRAM to the host system when High (Logic '1').
ADD[27:0]	Input	**Address:** I/Os for address transfer. **1Gb:** ADDR[25:0] – 26 Address pins for 1Gb **4Gb:** ADDR[27:0] – 28 Address pins for 4Gb
DQ[31:0]	Input/Output	**Data Inputs/Outputs:** The bi-directional I/Os transfer data [15:0].
INT#	Output	**Interrupt:** Output generated by the MRAM when an unrecoverable ECC error is detected during read operation (output goes Low on error).
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.
NC	-	**No Connect:** NCs are not internally connected. They can be driven or left unconnected
DNU	-	**Do Not Use:** DNUs must be left unconnected.

2. Functional Feature

2.1 Write & Read Timing

2.1.1 Write Operation

Figure 2: Write Timing

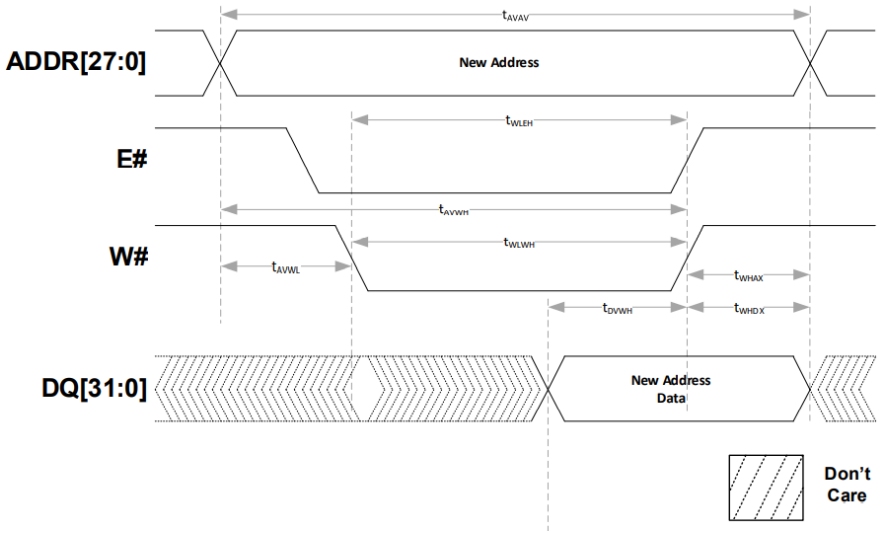


Table 2: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{AVAV}	45	-	ns
Address Set-Up Time	t_{AVWL}	0	-	ns
Address Valid to end of Write (G# High)	t_{AVWH}	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVWH}	30	-	ns
Write Pulse Width (G# High)	t_{WLWH}, t_{WLEH}	25	-	ns
Write Pulse Width (G# Low)	t_{WLWH}, t_{WLEH}	25	-	ns
Data Valid to end of Write	t_{DVWH}	15	-	ns
Data Hold Time	t_{WHDX}	0	-	ns
Write recovery Time	t_{WHAX}	12	-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

2.1.2 Read Operation

Figure 3: Read Timing

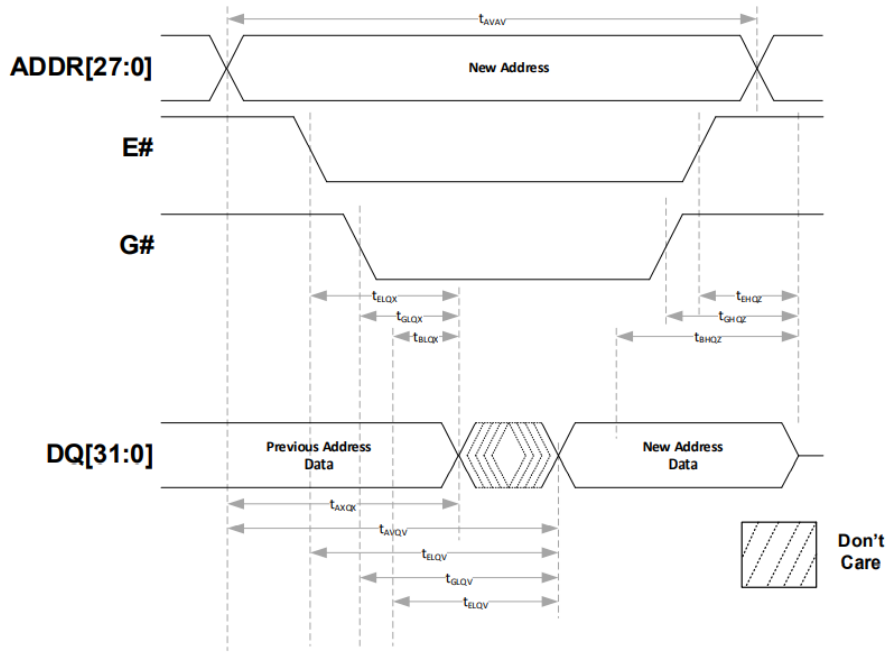


Table 3: Read Operation

Parameter	Symbol	Minimum	Maximum	Units
Read Cycle Time	t_{AVAV}	45	-	ns
Address Cycle Time	t_{AVQV}	-	45	ns
Chip Enable Access Time	t_{ELQV}	-	45	ns
Output Enable Access Time	t_{GLQV}	-	25	ns
Byte Enable Access Time	t_{BLQV}	-	25	ns
Output Hold From Address Change	t_{AXQX}	3	-	ns
Chip Enable Low to Output Active	t_{ELQX}	3	-	ns
Output Enable Low to Output Active	t_{GLQX}	0	-	ns
Byte Enable Low to Output Active	t_{BLQX}	0	-	ns
Chip Enable High to Output Hi-Z	t_{EHQZ}	0	15	ns
Output Enable High to Output Hi-Z	t_{GHQZ}	0	15	ns
Byte Enable High to Output Hi-Z	t_{BHQZ}	0	10	ns

Notes:
W# is High (Logic '1') for Read operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

2.3 P-SRAM Power Up and Power Down Consideration

When powering up, the following procedure is required to initialize the device correctly:

- E#, W#, G#, SE# must follow VCC during power-up

Figure 4: Power Up Behavior

When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G#, must follow V_{CC} during power-down
- During power loss or brownout, where Vcc goes below Vwi, read/write operations are prohibited. The power-up timing needs to be observed after Vcc goes above Vcc (minimum)

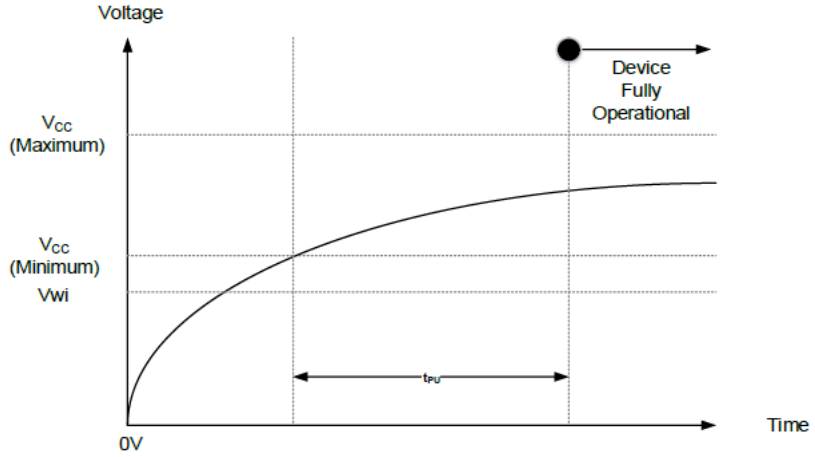


Figure 5: Power Down Behavior

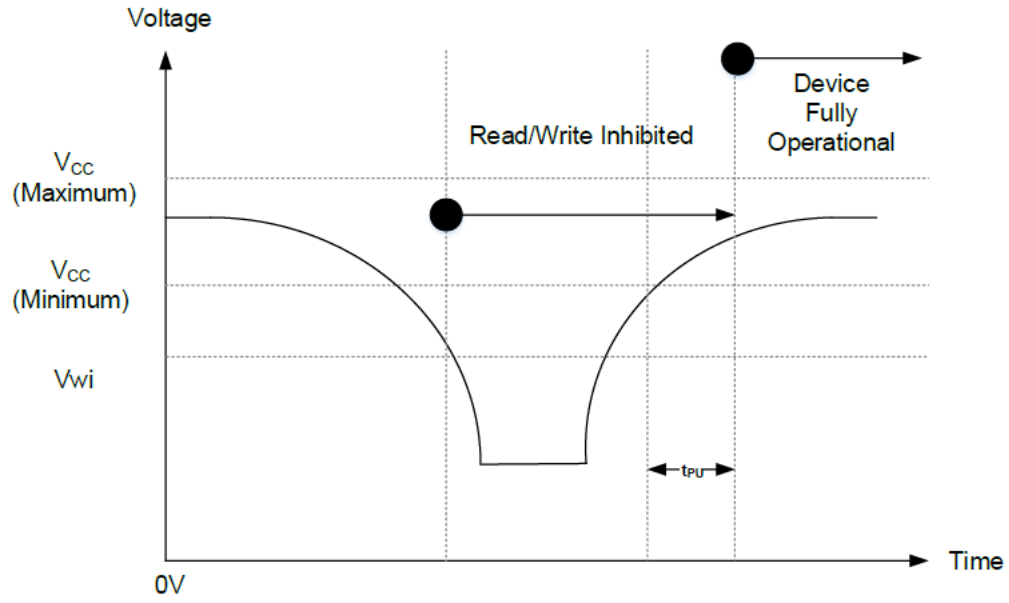


Table 4: Device Initialization Timing

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Power Up to First Instruction	t_{PU}	All operating voltages and temperatures	-	-	1	ms

3. P-SRAM Parallel System Design Consideration

3.1 PCB Layout Guideline

3.1.1 Power and Ground Planes

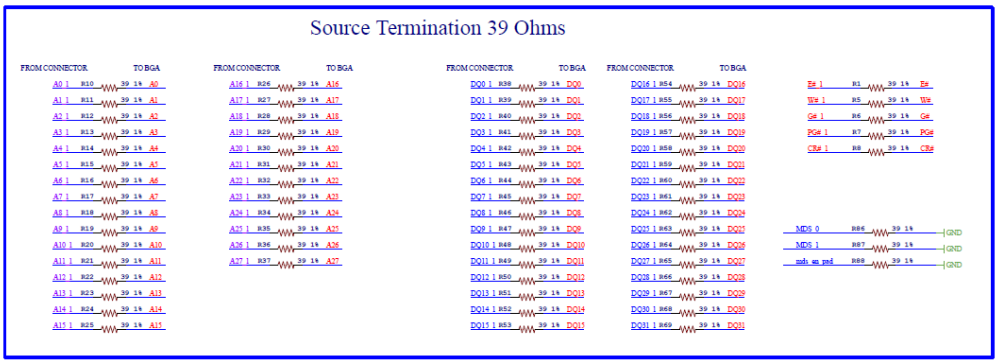
Power planes improve decoupling between circuits, preventing noise from propagating through the power supply from one circuit to another. In addition, they enable larger current carrying capacity, lowering the operating temperature of the board.

Ground planes in multi-layer board simplifies connecting each component to the ground net, provides clear return path on the ground plane and reduces noise and interference.

- The test board is designed with 8-layers, including 2 power planes and 2 ground planes. 50Ω ±10%, 8mil traces are used to reduce the trace impedance.

3.1.2 Reflection, Terminations and CrossTalk

Figure 6: Termination Resistor



- Clock signal is kept 3-4 times (24-25mil) away from other signals to avoid crosstalk.
- 39 Ohm resistor is used on each address, data and control signal

3.1.3 Signal Length Matching

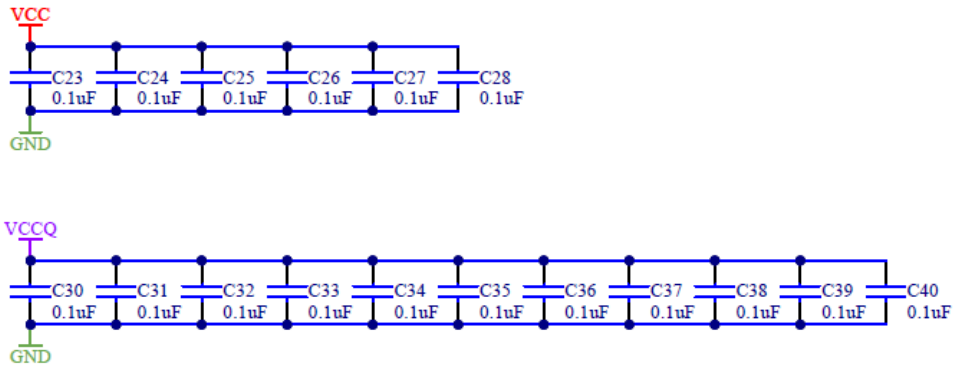
- Address signal group, data signal group, control signal group and clock are within 10ps. Clock signal is kept about 25mil away from other signals to ensure signal integrity.

3.2 Decoupling/Bypass Capacitor

Selecting the right decoupling capacitor is important in the P-SRAM parallel design. It provides a low impedance path from the power plane to the ground plan and further prevent voltage swing on the power and ground pins. The recommendations are as follows:

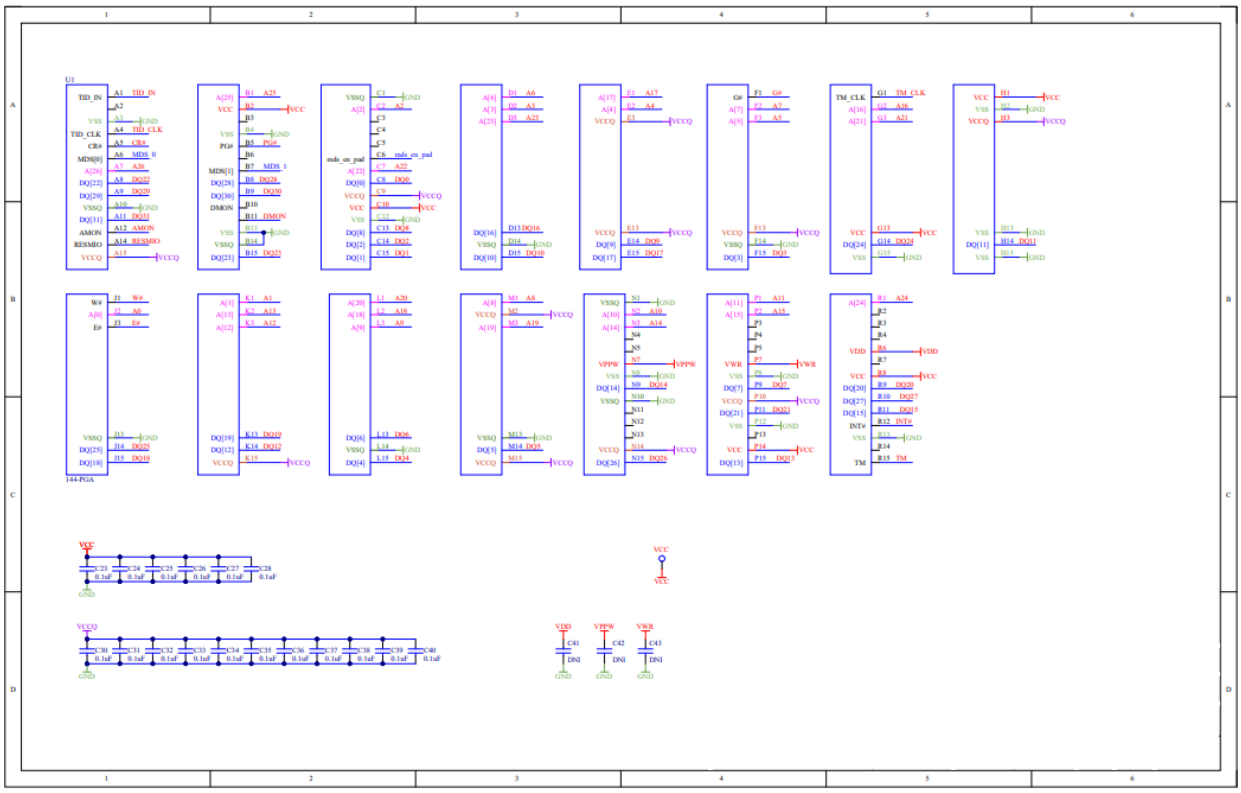
- Keep decoupling capacitors as close to the component as possible
- For each active component, additional capacitors are required (refer to schematic below)
- Keep capacitors on the same side of the AS3xx332 if possible
- On V_{CC} and V_{CCQ}, multiple 0.1µF capacitors are required (refer to figure 7)

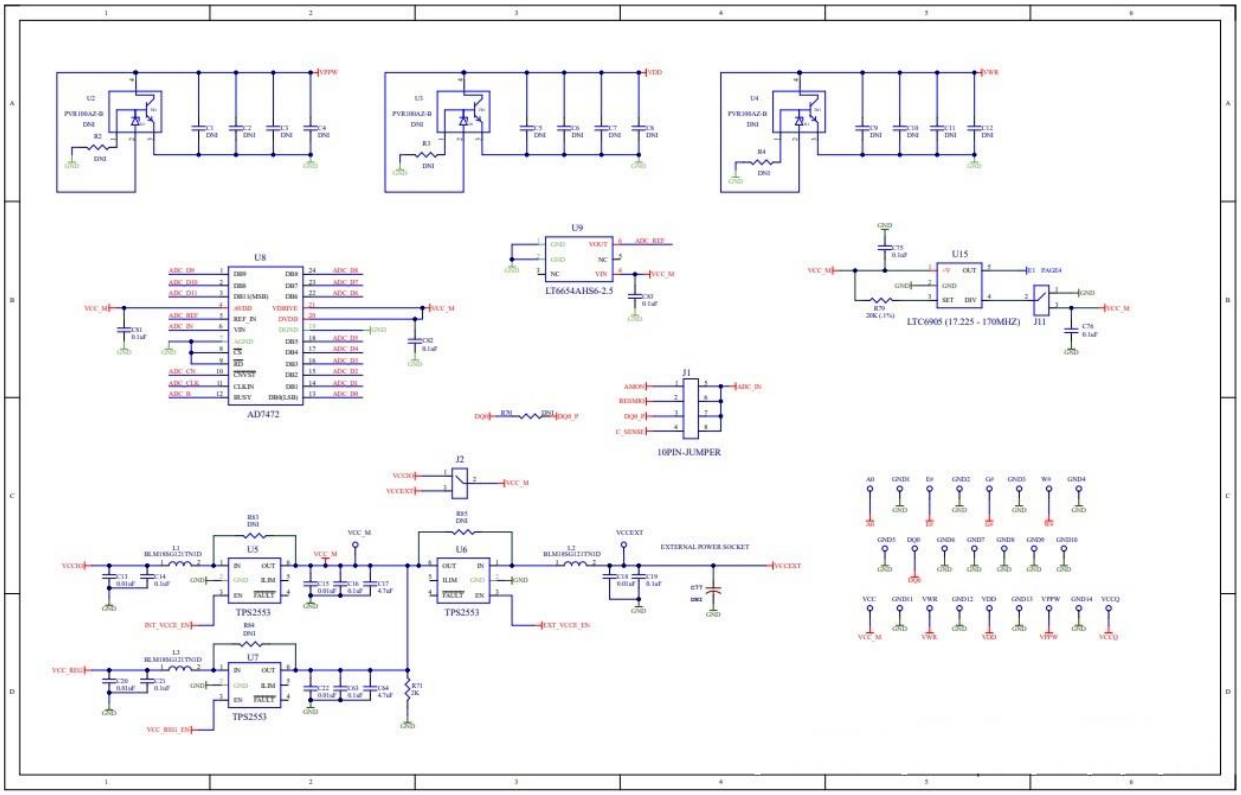
Figure 7: Decoupling Capacitor

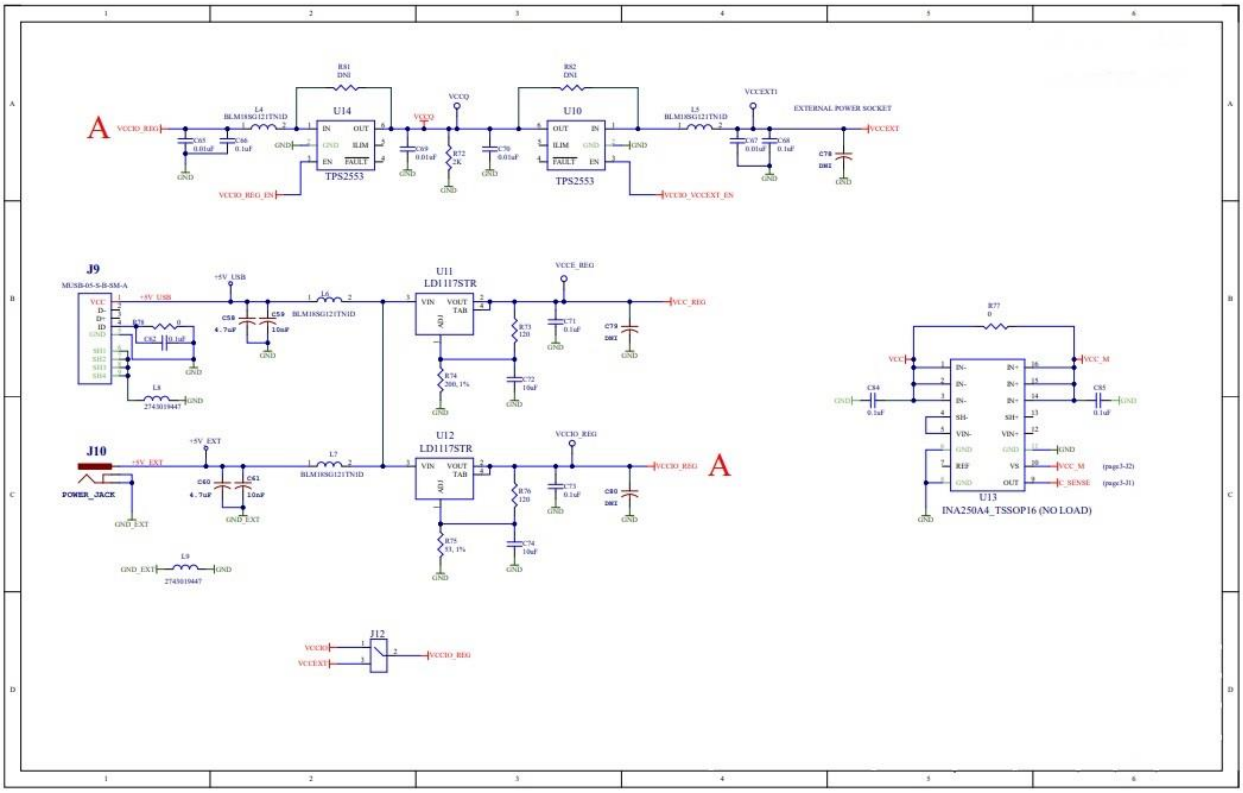


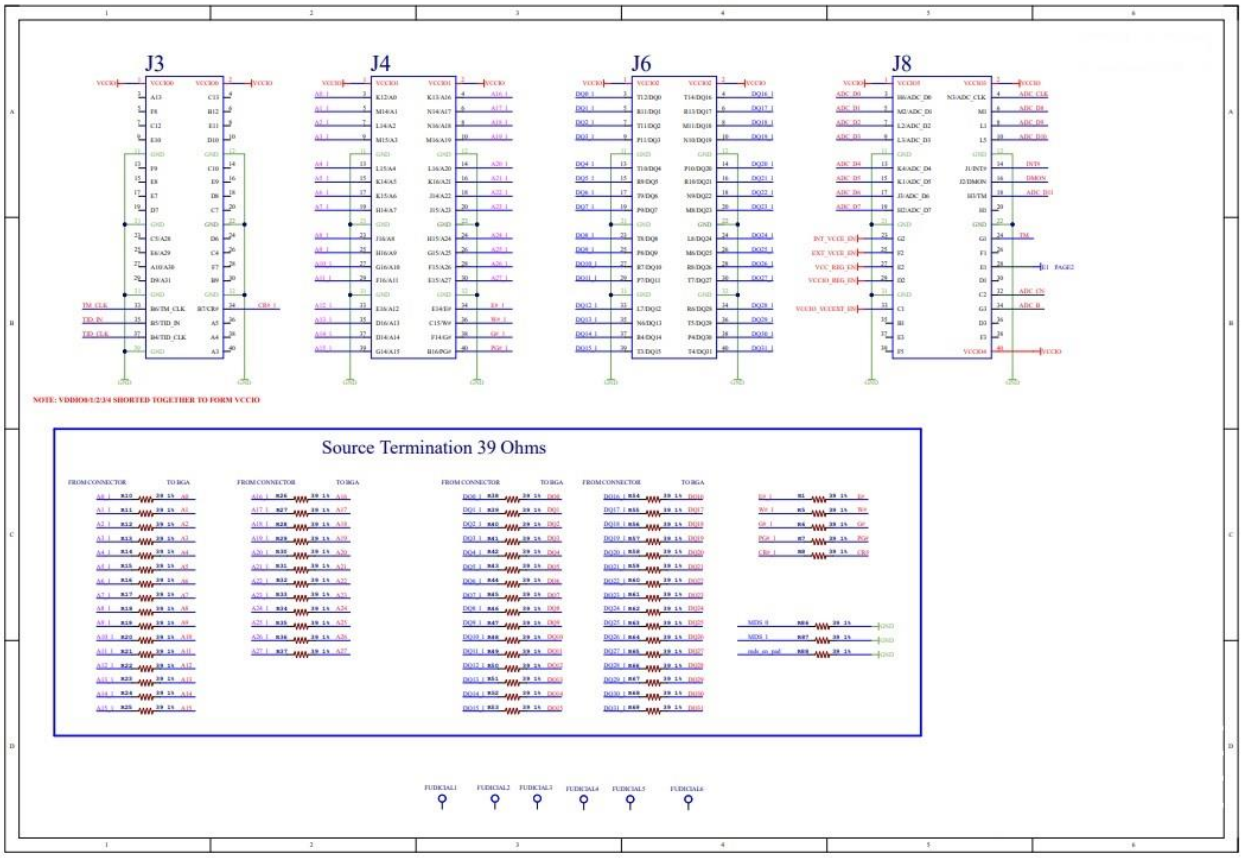
3.3 Reference Schematic

Figure 8: PS-RAM Parallel x32 Test Board Schematic




U2
PVR100AZ-B
U3
PVR100AZ-B
U4
PVR100AZ-B
U8
AD7472
U9
LT6654AHS6-2.5
U15
LTC6905 (17.225 - 170MHZ)
J11
J1
10PIN-JUMPER
J2
EXTERNAL POWER SOCKET
U5
TPS2553
U6
TPS2553
U7
TPS2553


U14
TPS2553
U10
TPS2553
EXTERNAL POWER SOCKET
J9
MUSB-05-S-B-SM-A
U11
LD1117STR
U12
LD1117STR
J10
POWER_JACK
U13
INA250A4_TSSOP16 (NO LOAD)
J12



- BOMs, Board Layout, Gerber File and IBIS/Verilog models are available per request.

4. P-SRAM Evaluation Kit

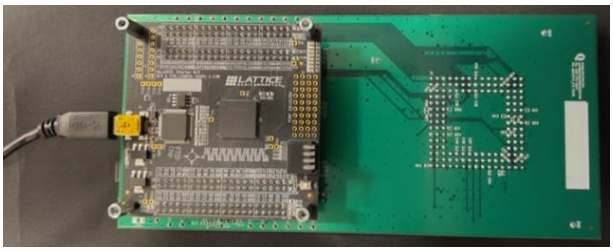
The Avalanche P-SRAM™ parallel x32 evaluation kit enables the users to evaluate Avalanche's 3rd generation P-SRAM parallel x32 product using a Lattice LCMXO3LF-6900C FPGA connected to Avalanche daughterboard via Avalanche proprietary FPGA based Asynchronous SRAM interface. The Lattice LCMXO3LF-6900C FPGA board communicates with the computer using a micro-USB cables type B connector.

The Lattice Mach XO3 evaluation board is a low-cost and easy-to-use development kit used to evaluate and quickly start a development with Avalanche AS3xxx332 devices. Key features include:

- Small form factor, low cost
- Instant-on boot-up
- Flexible programing I/O expansion – up to 384 I/O pins
- 4 expansion header landings to allow access to user GPIOs
- Supports both 1.8V and 3V I/Os
- Internal oscillator & PLLs
- Custom hardware timing
- Extended temperature flexibility

Figure 9: Lattice MachOX3 Breakout Board (Top & Bottom)

Figure 10: Avalanche P-SRAM Parallel x32 Daughter Board



Refer to the Eval Kit User Guide for more information on how to use the evaluation kit. The user guide can be downloaded from this link: https://www.avalanche-technology.com/products/discrete-mram/aerospace/

5. Revision History

Revision	Date	Change Summary
REV A	10/25/2021	Initial release