AS3xxx332 Reference Design Utilizing Lattice MachX03 FPGA Platform Application Note

AN000018 provides basis functional operation of the Avalanche ASxxx332 P-SRAM Parallel x32 devices and several key SRAM board design considerations.

1. Introduction

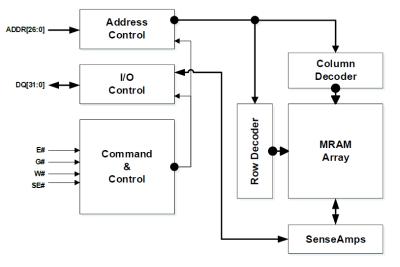
The AS3xxx332 is a high-speed asynchronous SRAM with densities offered in 1Gb and 4Gb, organizing in 32K bytes x 32 bits and 128K bytes x 32 bits respectively. The scalarly advanced 22nm STT-MRAM technology coupled with innovative circuit design provide low latency, high performance, and very reliable non-volatile memory solution. The Avalanche's 3rd Generation P-SRAM is ideal for Defense and Aerospace applications.

Memory access is controlled by Chip Enable (E#), Output Enable (G#) and Write Enable (W#).

To write to the device, drive Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[31]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[24]).

To read from the device, drive Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[24]) to appear on I/O pins (DQ[0] to DQ[31]).







Signal Description

Table 1: Signal Description

Signal	Туре	Description
E#	Input	Chip Enable: Enables or disables the MRAM.
G#	Input	Output Enable: Enables the output drivers for data transfer I/Os.
W#	Input	Write Enable: Transfers serial data from the host system to the MRAM when Low (Logic '0'). Transfers serial data from the MRAM to the host system when High (Logic '1').
ADD[27:0]	Input	Address: I/Os for address transfer. 1Gb: ADDR[25:0] – 26 Address pins for 1Gb 4Gb: ADDR[27:0] – 28 Address pins for 4Gb
DQ[31:0]	Input/Output	Data Inputs/Outputs: The bi-directional I/Os transfer data [15:0].
INT#	Output	Interrupt: Output generated by the MRAM when an unrecoverable ECC error is detected during read operation (output goes Low on error).
Vcc	Supply	Vcc: Core and I/O power supply.
Vss	Supply	Vss: Core and I/O ground supply.
NC	-	No Connect: NCs are not internally connected. They can be driven or left unconnected
DNU	-	Do Not Use: DNUs must be left unconnected.

2. Functional Feature

2.1 Write & Read Timing

2.1.1 Write Operation

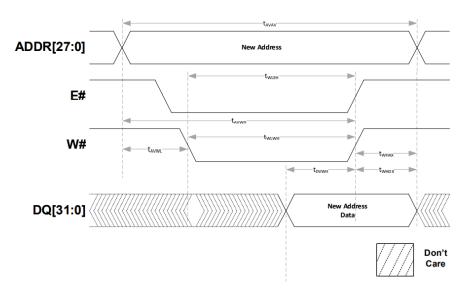


Figure 2: Write Timing



Table 2: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	tavav	45	-	ns
Address Set-Up Time	t avwl	0	-	ns
Address Valid to end of Write (G# High)	tavwн	28	-	ns
Address Valid to end of Write (G# Low)	tavwн	30	-	ns
Write Pulse Width (G# High)	twlwh, twleh	25	-	ns
Write Pulse Width (G# Low)	twlwh, twleh	25	-	ns
Data Valid to end of Write	tovwн	15	-	ns
Data Hold Time	t _{WHDX}	0	-	ns
Write recovery Time	t _{WHAX}	12	-	ns

Notes:

G# is High (Logic '1') for Write operation Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

2.1.2 Read Operation

Figure 3: Read Timing

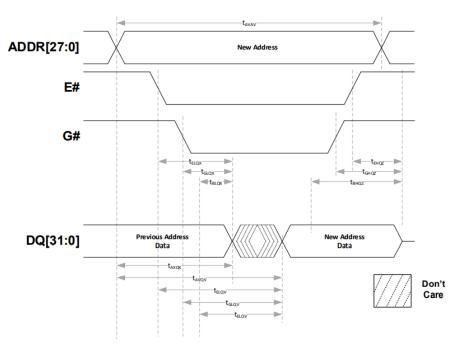




Table 3: Read Operation

Parameter	Symbol	Minimum	Maximum	Units
Read Cycle Time	tavav	45	-	ns
Address Cycle Time	t AVQV	-	45	ns
Chip Enable Access Time	t ELQV	-	45	ns
Output Enable Access Time	t GLQV	-	25	ns
Byte Enable Access Time	t _{BLQV}	-	25	ns
Output Hold From Address Change	taxqx	3	-	ns
Chip Enable Low to Output Active	telox	3	-	ns
Output Enable Low to Output Active	t GLQX	0	-	ns
Byte Enable Low to Output Active	t BLQX	0	-	ns
Chip Enable High to Output Hi-Z	t EHQZ	0	15	ns
Output Enable High to Output Hi-Z	t _{GHQZ}	0	15	ns
Byte Enable High to Output Hi-Z	t _{BHQZ}	0	10	ns

Notes:

W# is High (Logic '1') for Read operation

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

2.3 P-SRAM Power Up and Power Down Consideration

When powering up, the following procedure is required to initialize the device correctly:

• E#, W#, G#, SE# must follow VCC during power-up

Figure 4: Power Up Behavior

When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G#, must follow Vcc during power-down
- During power loss or brownout, where Vcc goes below Vwi, read/write operations are prohibited. The power-up timing needs to be observed after Vcc goes above Vcc (minimum)

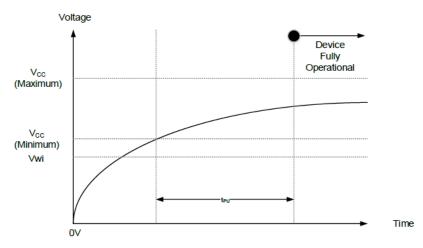




Figure 5: Power Down Behavior

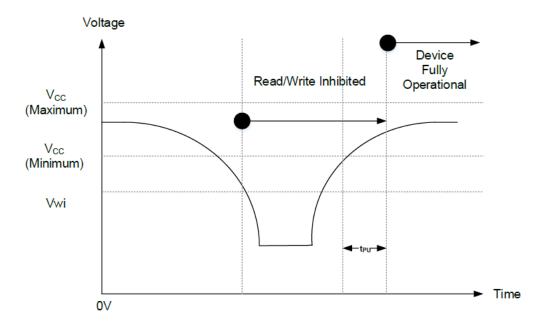


Table 4: Device Initialization Timing

Parameter	Symbol	Test Conditions	3.0V			
Farameter	Symbol	Symbol Test conditions		Typical	Maximum	Units
Vcc Range		All operating voltages and temperatures	2.7	-	3.6	V
Vcc Power Up to First Instruction	t₽U	All operating voltages and temperatures	-	-	1	ms

3. P-SRAM Parallel System Design Consideration

3.1 PCB Layout Guideline

3.1.1 Power and Ground Planes

Power planes improve decoupling between circuits, preventing noise from propagating through the power supply from one circuit to another. In addition, they enable larger current carrying capacity, lowering the operating temperature of the board.

Ground planes in multi-layer board simplifies connecting each component to the ground net, provides clear return path on the ground plane and reduces noise and interference.

• The test board is designed with 8-layers, including 2 power planes and 2 ground planes. $50\Omega \pm 10\%$, 8mil traces are used to reduce the trace impedance.



3.1.2 Reflection, Terminations and CrossTalk

Figure 6: Termination Resistor

	Source re	rmination 39 Ohms		
ROM CONNECTOR TO BGA	FROM CONNECTOR TO BGA	FROM CONNECTOR TO BGA	FROM CONNECTOR TO BGA	
A0 1 810 WW 39 18 A0	A16 1 826 WW 39 18 A16	DQ0 838 WW 39 18 DQ0	DQ16 1 #54 39 1% DQ16	E#] R1 WW 39 1% E#
Al R11_WW 39 18 Al	A17 1 827 W 39 18 A17	DQ1 1 839 AWA 39 18 DQ1	DQ17 1 855 WW 39 18 DQ17	W# 1 R5_WW-39 18 W#
A2 1 812 WW 39 18 A2	A15 828 WW 39 18 A15	DQ2 1 840 WW 39 18 DQ2	DQ18 856 WW 39 18 DQ18	Ge 1 R6 WW 39 18 Ge
A3 1 813 WW 39 18 A3	A19 1 829 WW 39 18 A19	DQ3 1 841 WW 39 18 DQ3	DQ19 1 #57 WW 39 18 DQ19	PG# 1 R7_WW-39 18 PG#
A4 1 814 WW 39 18 A4	A20 1 R30 WW 39 18 A20	DQ4 1 842 WW 39 18 DQ4	DQ20 1 858 WW 39 18 DQ20	CR# 1 R8 WW 39 1% CR#
A5 1 815 WW 39 18 A5	A21 1 R31 WW 39 18 A21	DQ5 1 843 WW 39 18 DQ5	DQ21 1 859 WW 39 18 DQ21	
A6 1 816 WW 39 1% A6	A22 1 R32 WW 39 1% A22	DQ6 1 R44 AMA 39 18 DQ6	DQ22 1 860 WW 39 1% DQ22	
A7 1 817 39 18 A7	A23 1 R33 WW 39 18 A23	DQ7 1 R45 AWA 39 18 DQ7	DQ23 1 861 WW 39 1% DQ23	
AS R18 WW 39 18 AS	A24 1 R34 WW 39 18 A24	DOS 1 846 AMA 39 18 DOS	DQ24 1 862 WW 39 1% DQ24	
A9 R19 WW 39 18 A9	A25 1 R35 WW 39 1% A25	DQ9 1 847 WW 39 18 DQ9	DQ25 1 R63 WW 39 1% DQ25	MDS 0 R86_WW-39 1% (GND
A10 1 820 39 18 A10	A26 1 R36 WW 39 1% A25	DQ10 R48 39 18 DQ10	DQ26 1 R64 WW 39 1% DQ26	MDS 1 R87_WW 39 1% (GND
All 821_WW 39 18 All	A27 1 R37 WW 39 1% A27	DOII 1 849 WW 39 18 DOII	DQ27 1 R65 39 1% DQ27	
A12 1 822 WW 39 18 A12		DQ12 1 850 WW 39 18 DQ12	DQ28 1 R66 39 1% DQ28	
Al3 1 923 WW 39 18 Al3		DQ13 851 WW 39 18 DQ13	DQ29 1 867 WW 39 18 DQ29	
Al4 1 824 WW 39 18 Al4		DQ14 1 R52 WW 39 18 DQ14	DQ30 1 R68 39 18 DQ30	
A15 1 825 WW 39 18 A15		DQ15 1 R53 AMA 39 18 DQ15	DQ31 1 R69 AVA 39 18 DQ31	

- Clock signal is kept 3-4 times (24-25mil) away from other signals to avoid crosstalk.
- 39 Ohm resistor is used on each address, data and control signal

3.1.3 Signal Length Matching

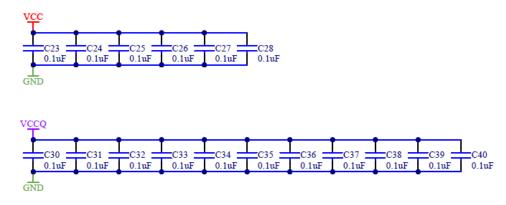
• Address signal group, data signal group, control signal group and clock are within 10ps. Clock signal is kept about 25mil away from other signals to ensure signal integrity.

3.2 Decoupling/Bypass Capacitor

Selecting the right decoupling capacitor is important in the P-SRAM parallel design. It provides a low impedance path from the power plane to the ground plan and further prevent voltage swing on the power and ground pins. The recommendations are as follows:

- Keep decoupling capacitors as close to the component as possible
- For each active component, additional capacitors are required (refer to schematic below)
- Keep capacitors on the same side of the AS3xx332 if possible
- On V_{cc} and V_{cco}, multiple 0.1µF capacitors are required (refer to figure 7)

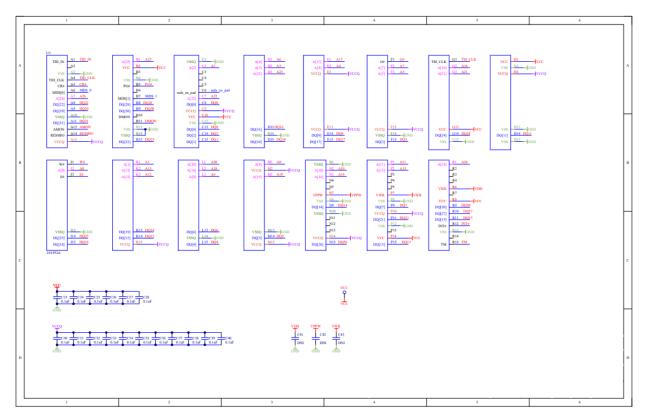
Figure 7: Decoupling Capacitor



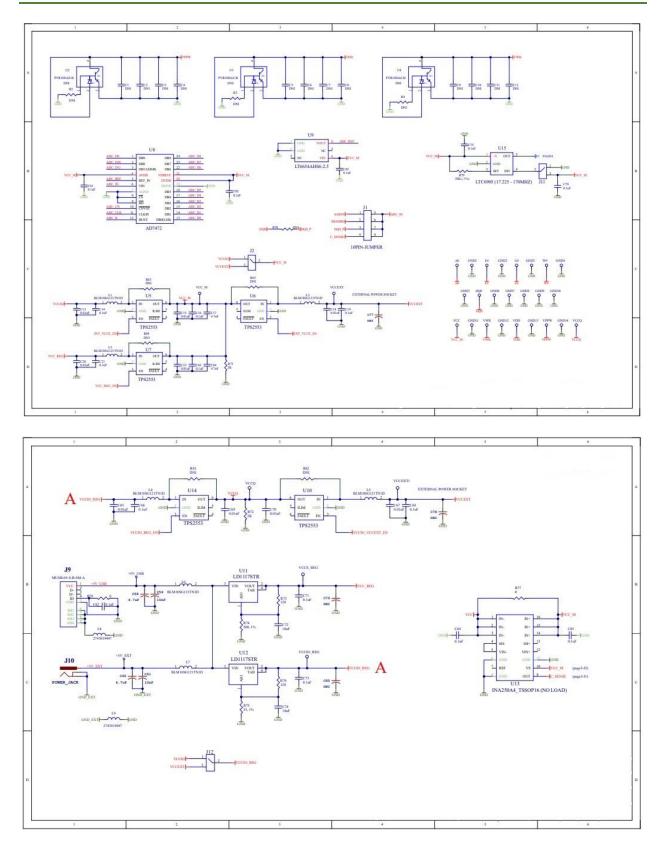


3.3 Reference Schematic

Figure 8: PS-RAM Parallel x32 Test Board Schematic









	1	3	4-		5	4
J3	J4		J6	J8		
	4 NEIO 1 VICIO	KIEAIA 4 Alle 1	VICEO 1 VIERO VICEO 2 DOB 1 3. TI2DO0 TI4D016 4	VCD0 VCD0 VCD0 VCD0 D016 1 VCD0 3 INVADC 1	WCCHIS 2 PCCHID	
L 78 B12			DOL1 5 811001 811001 0	DQIT I ADC DI 2 MOADC		
	2 <u>62 1 7</u> 13462		000 J 7 TI DO2 MILDON 8	0015_1 ADC 02 T L2ADC 1		
910 010 - B10	Jo AL 9 MISA		DOLI 9 PILDOJ NSEDQIS 10	DOIN ADC DI . LEADC I		
II and and	12 cites	00 0	- 11 tota can 12	DOD I AIK IN II		
13 19 C10	24 <u>At 1</u> 13 135A4	L16A20	004 1 13 TIAD04 710 D020 14	KAADC I	M JUDITS	
¹⁵ 18 19		KIGAN	DQS 1 15 RHDQS R1H/DQ21 Hit DQ8 1 17 78/D08 NHD022 18	0021 1 AIK DS B K1020C 1 0022 1 AIK DS IT JLADE D	8 JUDION	
	20 <u>67.1 19</u> 10467	335.522	DOT 1 19. PHD07 MED023 20	0021 1 ADC 07 19 SECON 1	e marin	
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	24 01 J2 THEAS		DOR.1 .22 TKINGS LINDON 24	22 (0.11) NT WOLDN - 22 CZ	ca 24 TM	
²⁵ 86/429 C4		GIS/AD	DON 1 25 PEDQ9 MEDQ25 28	0023 1 EXT_VOTE_EN 25 F2	n 🖓	
²⁷ AUGAID #7 ²⁰ DRA31 BP	28 AUL 27 GIONIS 29 AUL 28 DISAU		0001 27 ETDON ESDOX 28 0001 20 77000 17:0027 20	0025 VCC EIG TN 27 12 0027 VCC0 EIG TN 28 72		
11 CHD CHD	12 DIG COD	115027 10	11 DED CHE 12	WEID RIG IN THE	C2 22 ADC DN	
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TED. IN 15 BUTTE IN AS			DQ13 1 35 N6DQ13 T5:DQ29 36	2009-1 ³² at	103 -26	
TID CLK 37 BATTD CLK A4		Press.	DOI-1 37 BADQH PADQB 28	<u>1008.1</u> 7. 13	12 - 24	
-20 (HC) A3	-40 011 - 22 GI4IXIS	BIARCO 49 0001	DOIS 1 27 TIDQIS TADQII 48	2031_1 ³⁶ _ 13	VICIDA HI VICID	
	Source Ter	rmination 39 Ohms				
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AL 820 MIL 28 15 AD	FROM CONNECTOR TO BGA	FROM CONNECTOR TO BGA	DOIS 1 884	<u>p. a</u>		
AL 1 820 MM 28 15 AL	FROM-CONNECTOR TO BGA	TROMICONNECTOR TO BGA	DOID 1 884 900 39 14 DOID DOIT 1 888 900 19 15 15 DOIT	No 1 85 WW 28 35 The		
AL 820 MIL 28 15 AD	JIGM CONNECTOR TO BGA alic #86 #10 33 Alli Al7 #37 #10 15 Al7 alic #86 #10 33 Alli alic #88 #10 33 Alli alic #88 #10 33 Alli	FROM CONNECTOR TO BIGA DOI 48.8 34.54 DOI DOI 48.8 34.94 DOI DOI 48.8 34.94 DOI DOI 1.94.9 34.94 DOI DOI 1.94.9 34.94 DOI DOI 1.94.9 34.94 DOI DOI 1.94.9 34.90 DOI	DOIS 1 884	Wir T R5 200 25 THE Gir I R6 WW 200 25 Gir POir I R7 WW 200 25 ROF		
All BLD 29 15 All	FRONCOMMETCINE TO BIGA <u>216.1</u> 895	FROM CONNECTOR DOBCA 1001 488	DOID 1 844	01 1 84 100 28 35 100 01 1 84 100 28 35 00		
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• BOMs, Board Layout, Gerber File and IBIS/Verilog models are available per request.

4. P-SRAM Evaluation Kit

The Avalanche P-SRAM[™] parallel x32 evaluation kit enables the users to evaluate Avalanche's 3rd generation P-SRAM parallel x32 product using a Lattice LCMXO3LF-6900C FPGA connected to Avalanche daughterboard via Avalanche proprietary FPGA based Asynchronous SRAM interface. The Lattice LCMXO3LF-6900C FPGA board communicates with the computer using a micro-USB cables type B connector.

The Lattice Mach XO3 evaluation board is a low-cost and easy-to-use development kit used to evaluate and quickly start a development with Avalanche AS3xxx332 devices. Key features include:

- Small form factor, low cost
- Instant-on boot-up
- Flexible programing I/O expansion up to 384 I/O pins
- 4 expansion header landings to allow access to user GPIOs
- Supports both 1.8V and 3V I/Os
- Internal oscillator & PLLs
- Custom hardware timing
- Extended temperature flexibility



Figure 9: Lattice MachOX3 Breakout Board (Top & Bottom)



Figure 10: Avalanche P-SRAM Parallel x32 Daughter Board



Refer to the Eval Kit User Guide for more information on how to use the evaluation kit. The user guide can be downloaded from this link: <u>https://www.avalanche-technology.com/products/discrete-mram/aerospace/</u>

5. Revision History

Revision	Date	Change Summary
REV A	10/25/2021	Initial release