AS3xxGB32 Reference Design Utilizing Lattice MachX03 FPGA Platform Application Note

AN000018 provides basis functional operation of the Avalanche AS3xxGB32 P-SRAM Parallel x32 devices and several key P-SRAM board design considerations.

1. Introduction

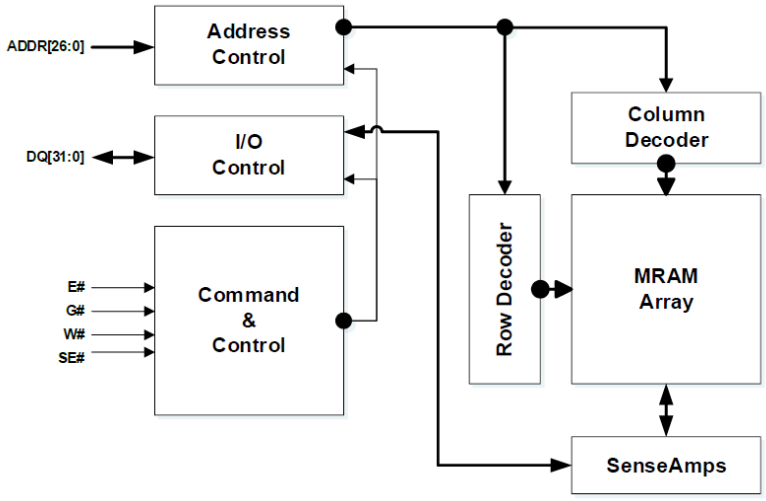
The AS3xxGB32 is a high-speed asynchronous SRAM with densities offered in 1Gb and 4Gb, organizing in 32K bytes x 32 bits and 128K bytes x 32 bits respectively. The scalarly advanced 22nm STT-MRAM technology coupled with innovative circuit design provide low latency, high performance, and very reliable non-volatile memory solution. The Avalanche's 3rd Generation P-SRAM is ideal for Defense and Aerospace applications.

Memory access is controlled by Chip Enable (E#), Output Enable (G#) and Write Enable (W#).

To write to the device, drive Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[31]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[24]).

To read from the device, drive Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[24]) to appear on I/O pins (DQ[0] to DQ[31]).

Figure 1: Functional Block Diagram



Signal Description

Table 1: Signal Description

Signal	Ball Assignment	Type	Description
E#	P8	Input	**Chip enable:** Enables or disables the MRAM.
G#	P7	Input	**Output enable:** Enables the output drivers for data transfer I/Os.
CR#	J2	Input	**Configuration Register enable:** Enables access to the Configuration registers
W#	M8	Input	**Write enable:** Transfers serial data from the host system to the MRAM when Low (Logic '0').Transfers serial data from the MRAM to the host system when High (Logic '1').
ADDR[26:0]	M2, L4, K13, M3, L3, M7, P12, L12, N11, N6, P6, L13, M13, P10, N10, M12, N13, L11, M11, P5, P3, N5, N4, M4, N2, N9, M9	Input	**Address:** I/Os for address transfer 1G: ADDR[24:0] – 25 Address pins for 1Gb x32 devices.* 4G: ADDR[26:0] – 27 Address pins for 4Gb x32 devices.
DQ[31:0]	E2, F2, D2, E3, E12, D10, C9, C7, G4, G3, F13, D13, C10, E8, F6, E5, E13, G11, E10, F9, C8, C6, D6, D4, G12, C12, D11, D9, E7, C5, D5, C3	Input / Output	**Data inputs/outputs:** The bidirectional I/Os transfer data [15:0].
INT#	G13	Output	**Interrupt:** Output generated by the MRAM when an unrecoverable ECC error is detected during read operation (output goes low on error).
V_{CCIO}	F12, J12, E11, M10, D8, N8, D7, N7, M5, E4, F3, J3	Supply	I/O power supply.
V_{SSIO}	F10, L10, E9, L9, F8, L8, F7, L7, E6, L6, G5,	Supply	I/O ground supply.
V_{CC}	C13, P13, D12, N12, C11, F11, H11, J11, K11, P11, C4, F4, H4, J4, K4, P4, D3, N3, C2, P2	Supply	Core power supply.
V_{SS}	A14, B14, C14, H13, R14, T14, A13, T13, A12, G10, H10, J10,	Supply	Core ground supply.

Signal	Ball Assignment	Type	Description
	K10, F5, L5, A2, T2, A1, B1, R1, T1		
DNU	J13, H12, K12, P9, M6, H5, J5, K5, H3, G2, H2, K2, L2		**Do Not Use:** DNUs must be left unconnected.
RFU	K3		**Reserved for Future Use:** requires to have an external pull-up resistor (10KΩ)

* Unused ADDR[26:25] balls should be connected to Ground

2. Functional Feature

2.1 Write & Read Timing

2.1.1 Write Operation

Figure 2: Write Timing

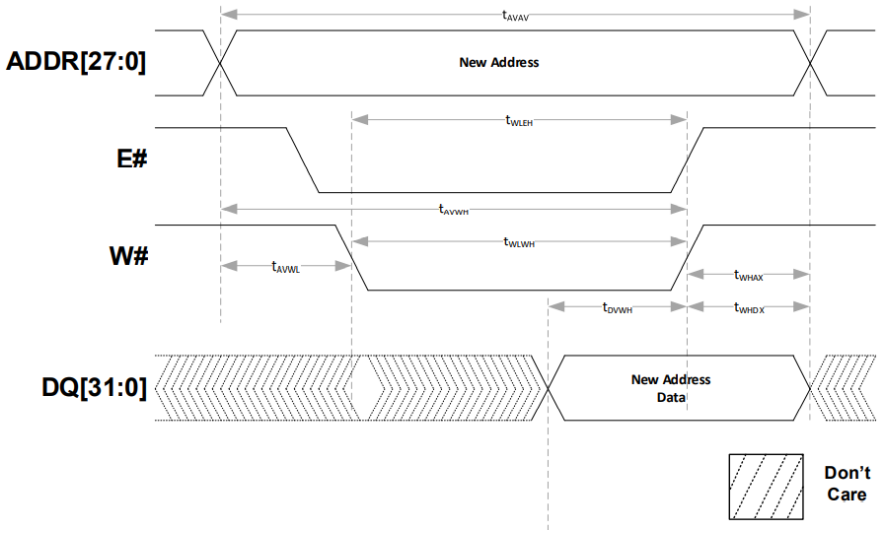


Table 2: Write Operation

Parameter	Symbol	Minimum	Maximum	Units
Write Cycle Time	t_{AVAV}	45	-	ns
Address Set-Up Time	t_{AVWL}	0	-	ns
Address Valid to end of Write (G# High)	t_{AVWH}	28	-	ns
Address Valid to end of Write (G# Low)	t_{AVWH}	30	-	ns
Write Pulse Width (G# High)	t_{WLWH}, t_{WLEH}	25	-	ns
Write Pulse Width (G# Low)	t_{WLWH}, t_{WLEH}	25	-	ns
Data Valid to end of Write	t_{DVWH}	15	-	ns
Data Hold Time	t_{WHDX}	0	-	ns
Write recovery Time	t_{WHAX}	12	-	ns

Notes:
G# is High (Logic '1') for Write operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

2.1.2 Read Operation

Figure 3: Read Timing

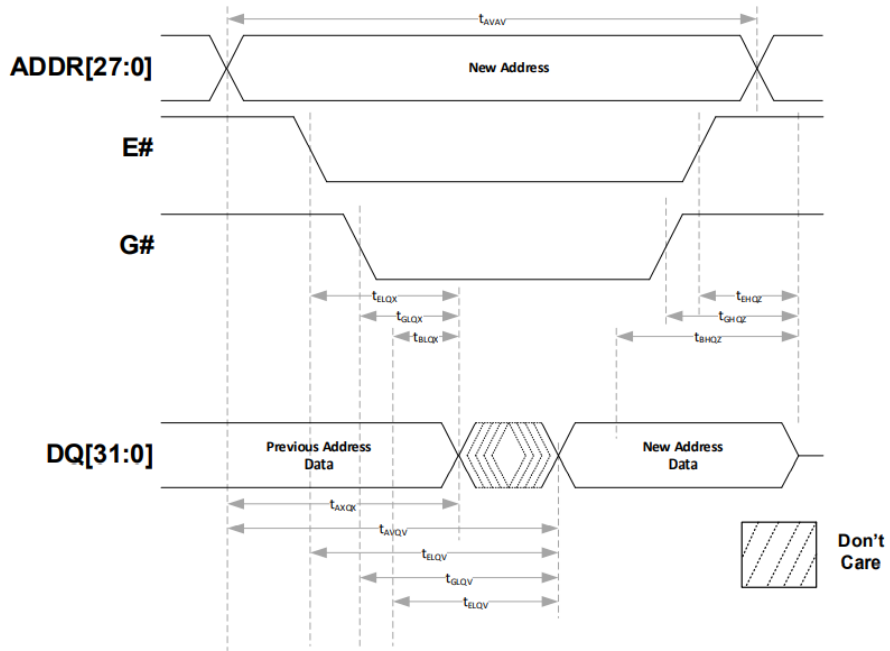


Table 3: Read Operation

Parameter	Symbol	Minimum	Maximum	Units
Read Cycle Time	t_{AVAV}	45	-	ns
Address Cycle Time	t_{AVQV}	-	45	ns
Chip Enable Access Time	t_{ELQV}	-	45	ns
Output Enable Access Time	t_{GLQV}	-	25	ns
Byte Enable Access Time	t_{BLQV}	-	25	ns
Output Hold From Address Change	t_{AXQX}	3	-	ns
Chip Enable Low to Output Active	t_{ELQX}	3	-	ns
Output Enable Low to Output Active	t_{GLQX}	0	-	ns
Byte Enable Low to Output Active	t_{BLQX}	0	-	ns
Chip Enable High to Output Hi-Z	t_{EHQZ}	0	15	ns
Output Enable High to Output Hi-Z	t_{GHQZ}	0	15	ns
Byte Enable High to Output Hi-Z	t_{BHQZ}	0	10	ns

Notes:
W# is High (Logic '1') for Read operation
Power supplies must be stable
Addresses valid either before or at the same time as E# goes low

2.3 P-SRAM Power Up and Power Down Consideration

When powering up, the following procedure is required to initialize the device correctly:

- V_{CC} and V_{CCIO} can ramp up together (R_{VR}), if not possible then V_{CC} first followed by V_{CCIO}. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-up (E# must follow the applied voltage on V_{CC} (a 10KΩ pull-up Resistor to V_{CC} is recommended)) until V_{CC} reaches V_{CC}(minimum) and then a further delay of t_{PU} (Figure 8).
- During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences (Figure 4).

When powering down, the following procedure is required to turn off the device correctly:

- V_{CC} and V_{CCIO} can ramp down together (R_{VF}), if not possible then V_{CC} first followed by VCCIO. The maximum difference between the two voltages should not exceed 0.7V.
- The device must not be selected at power-down (E# must follow V_{CC} during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended)) until V_{CC} reaches VSS.
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum).
- During power loss or brownout, when V_{CC} goes below $V_{CC\text{-}CUTOFF}$. The voltage must drop below V_{CC}(Reset) for a period of t_{PD}. The power-up timing needs to be observed after V_{CC} goes above V_{CC}(minimum)

Figure 4: Power Up Behavior

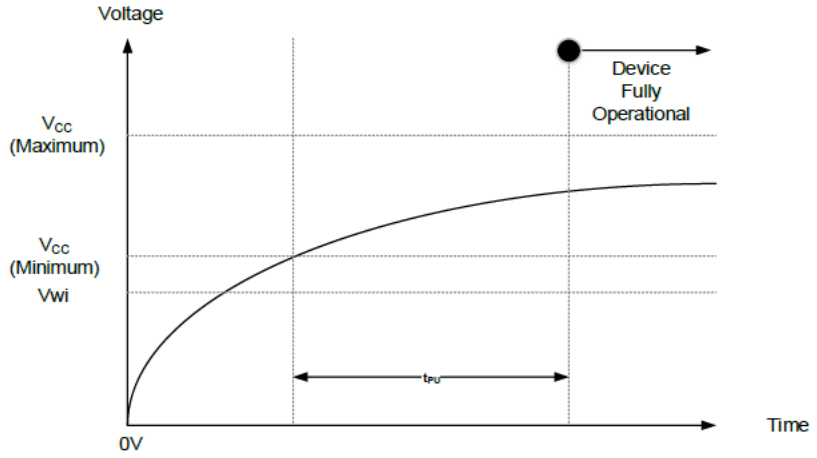


Figure 5: Power Down Behavior

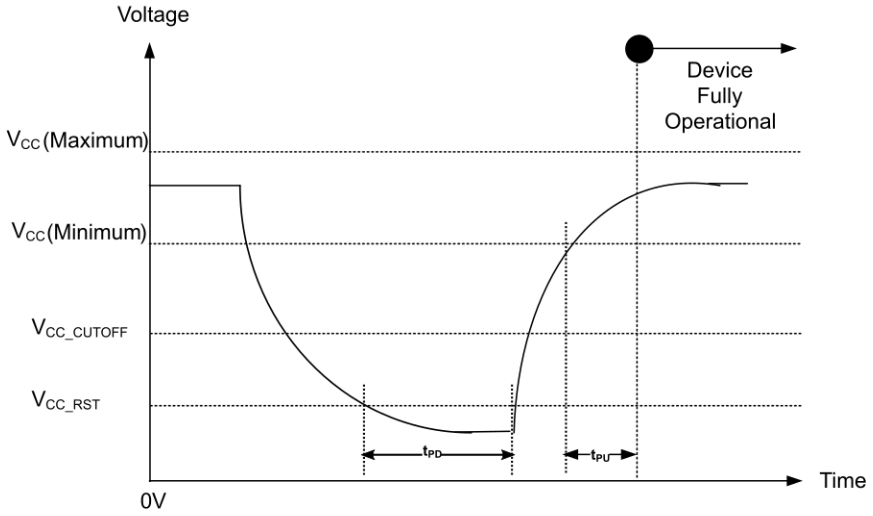


Table 4: Device Initialization Timing

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}		30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		1	-	-	ms

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} (low) time	t_{PD}		1			ms
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} (Reset)	V_{CC_RST}		0		0.3	V

3. P-SRAM Parallel System Design Consideration

3.1 PCB Layout Guideline

3.1.1 Power and Ground Planes

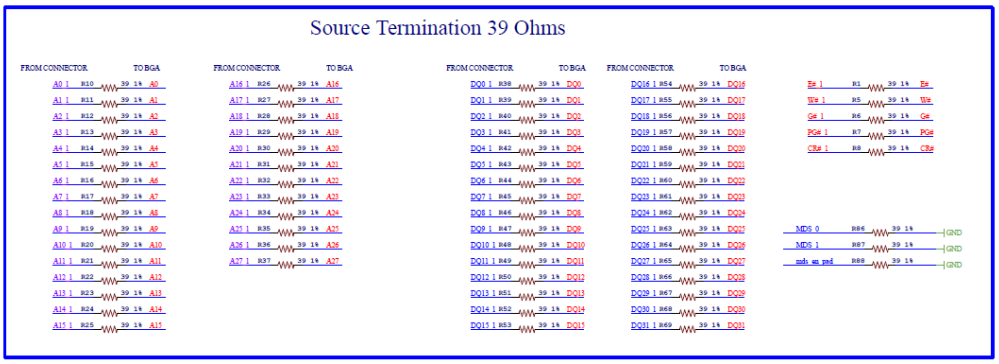
Power planes improve decoupling between circuits, preventing noise from propagating through the power supply from one circuit to another. In addition, they enable larger current carrying capacity, lowering the operating temperature of the board.

Ground planes in multi-layer board simplifies connecting each component to the ground net, provides clear return path on the ground plane and reduces noise and interference.

- The test board is designed with 8-layers, including 2 power planes and 2 ground planes. 50Ω ±10%, 8mil traces are used to reduce the trace impedance.

3.1.2 Reflection, Terminations and CrossTalk

Figure 6: Termination Resistor



- Clock signal is kept 3-4 times (24-25mil) away from other signals to avoid crosstalk.
- 39 Ohm resistor is used on each address, data and control signal

3.1.3 Signal Length Matching

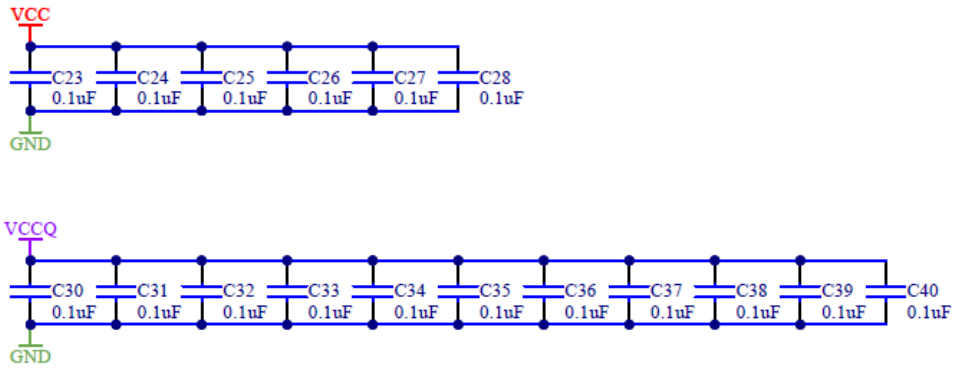
- Address signal group, data signal group, control signal group and clock are within 10ps. Clock signal is kept about 25mil away from other signals to ensure signal integrity.

3.2 Decoupling/Bypass Capacitor

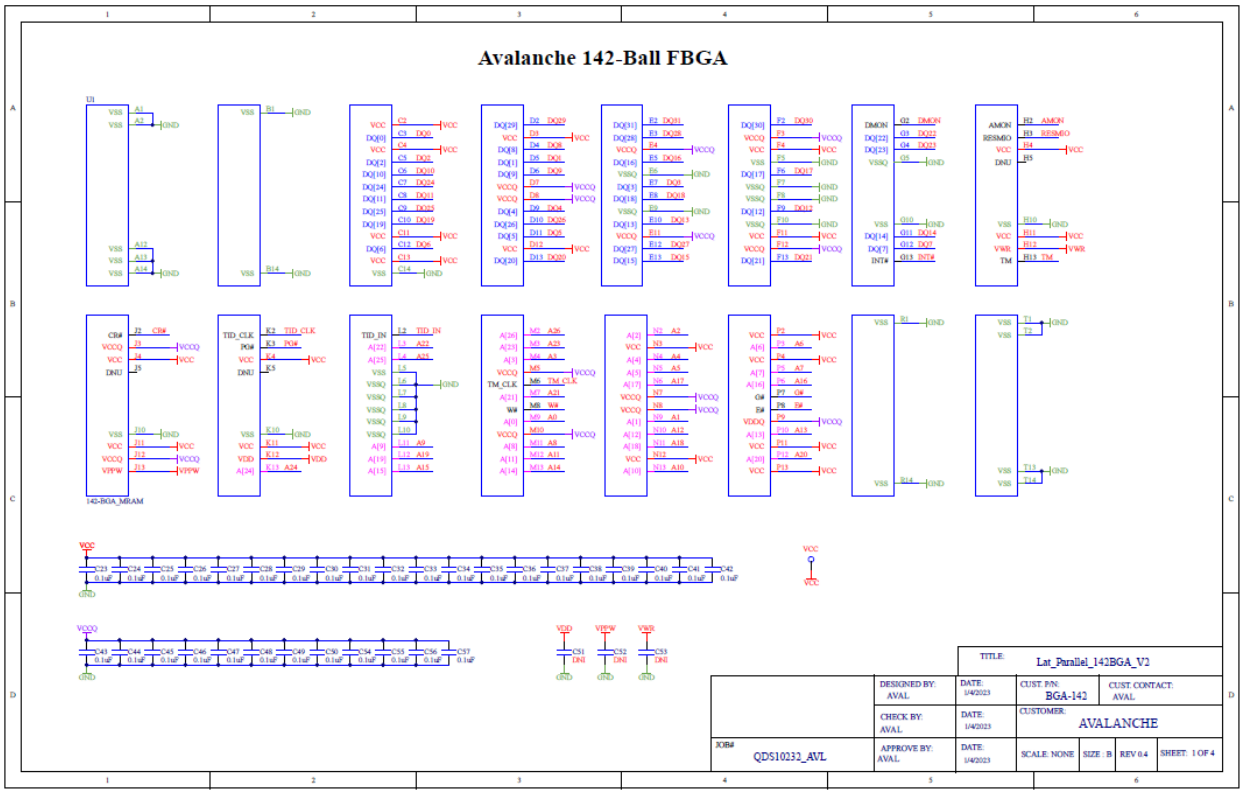
Selecting the right decoupling capacitor is important in the P-SRAM parallel design. It provides a low impedance path from the power plane to the ground plan and further prevent voltage swing on the power and ground pins. The recommendations are as follows:

- Keep decoupling capacitors as close to the component as possible
- For each active component, additional capacitors are required (refer to schematic below)
- Keep capacitors on the same side of the AS3xxGB32 if possible
- On V_{CC} and V_{CCQ}, multiple 0.1µF capacitors are required (refer to figure 7)

Figure 7: Decoupling Capacitor



3.3 Reference Schematic


Avalanche 142-Ball FBGA
142-BGA_MRAM
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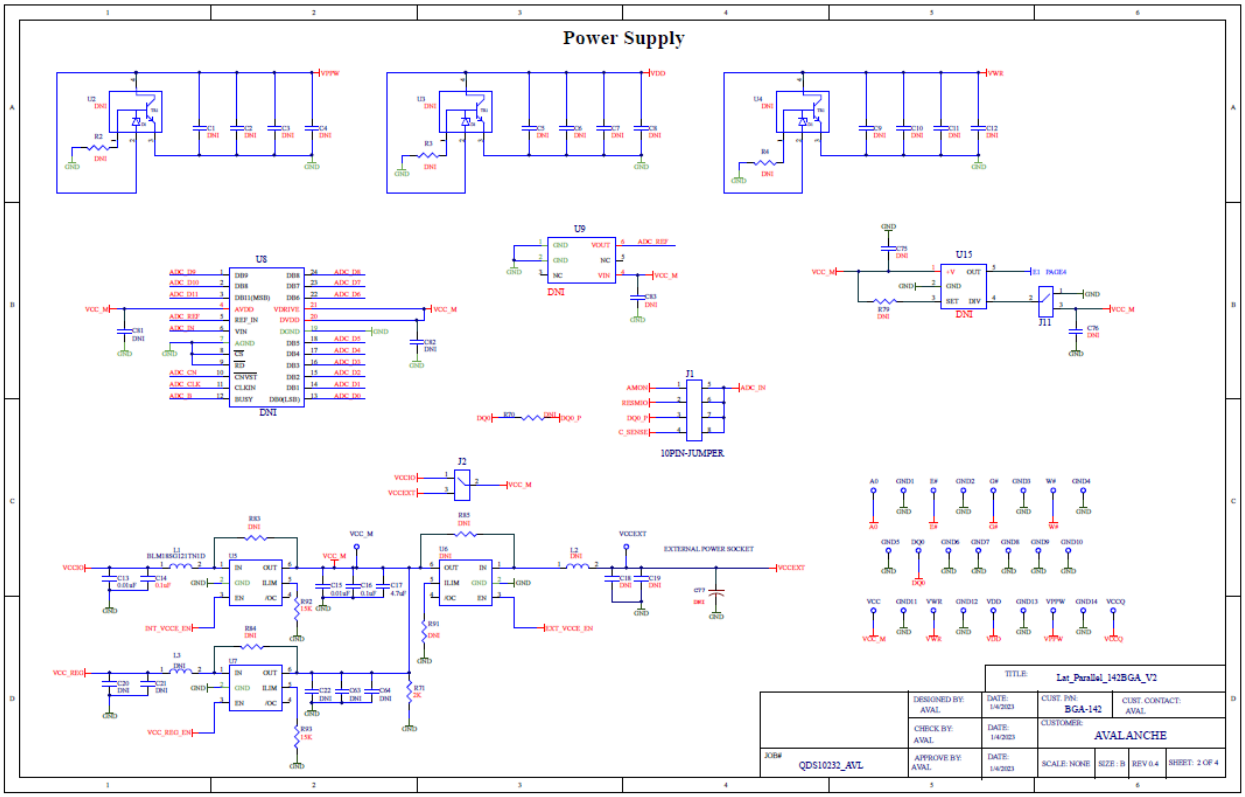
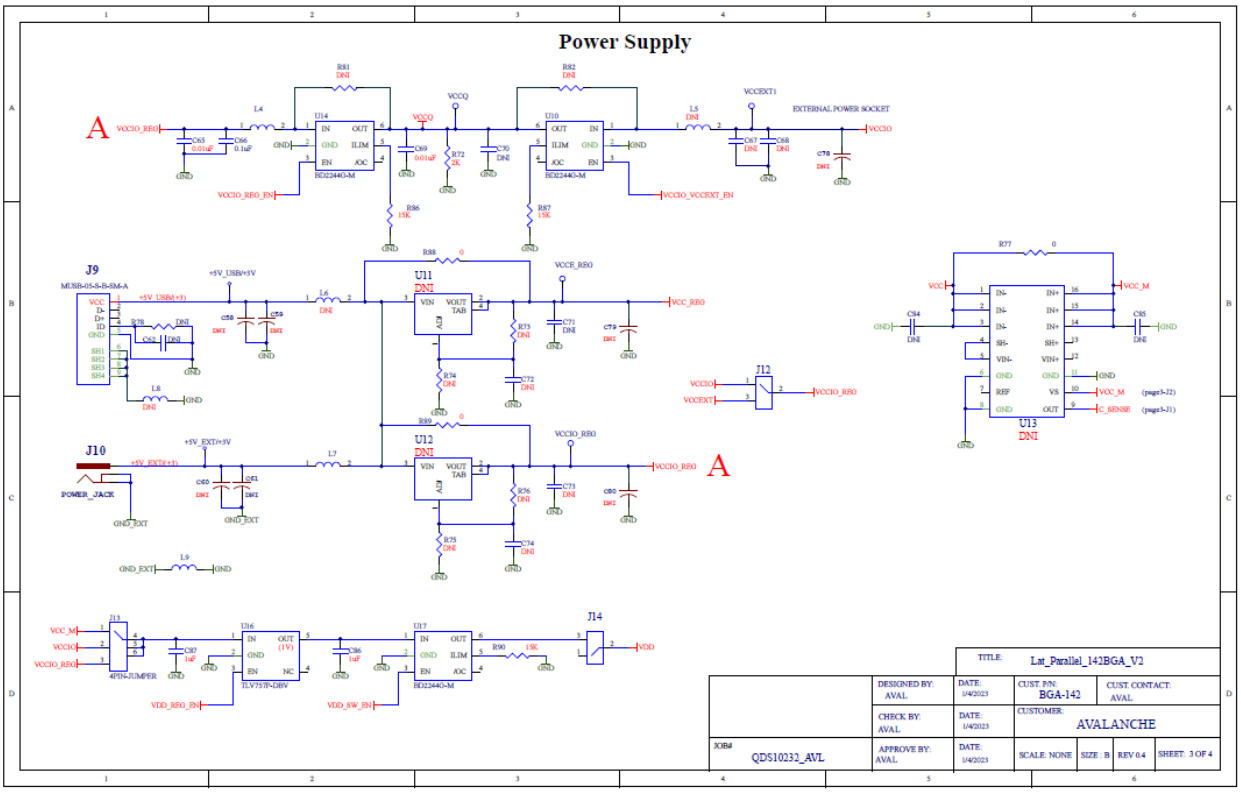
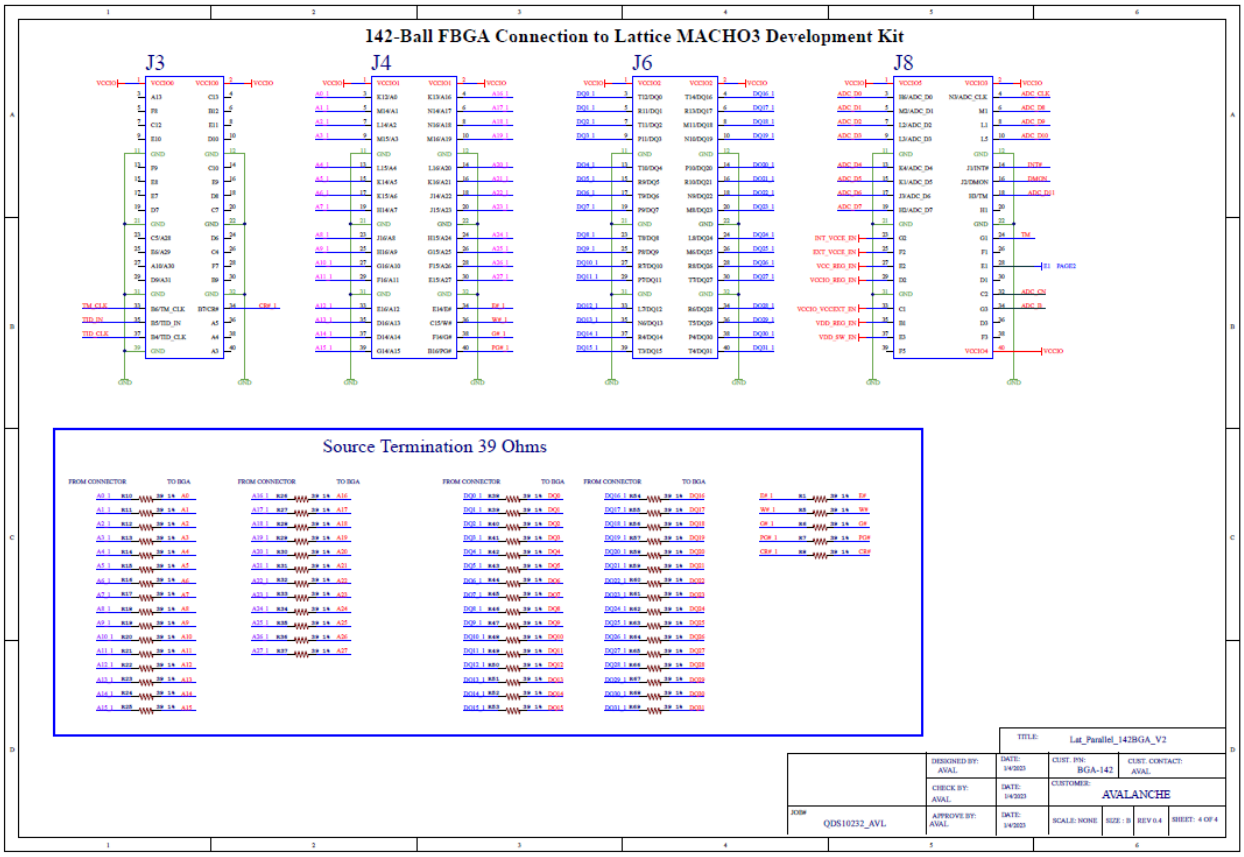
DESIGNED BY: AVAL
DATE: 1/4/2023
CUST. P/N: BGA-142
CUST. CONTACT: AVAL
CHECK BY: AVAL
DATE: 1/4/2023
CUSTOMER: AVALANCHE
JOB# QDS10232_AVL
APPROVE BY: AVAL
DATE: 1/4/2023
SCALE: NONE
SIZE : B
REV 0.4
SHEET: 1 OF 4


Power Supply
DNI
10PIN-JUMPER
EXTERNAL POWER SOCKET
TITLE: Lat_Parallel_142BGA_V2
DESIGNED BY: AVAL
DATE: 1/4/2023
CUST. P/N: BGA-142
CUST. CONTACT: AVAL
CHECK BY: AVAL
DATE: 1/4/2023
CUSTOMER: AVALANCHE
JOB# QDS10232_AVL
APPROVE BY: AVAL
DATE: 1/4/2023
SCALE: NONE
SIZE : B
REV 0.4
SHEET: 2 OF 4


Power Supply
J9
J10
J12
J13
J14
U11
U12
U13
U14
U16
U17
U10
POWER_JACK
4PIN-JUMPER
TLV757P-DBV
BD22440-M
EXTERNAL POWER SOCKET
TITLE: Lat_Parallel_142BGA_V2
DESIGNED BY: AVAL
CHECK BY: AVAL
APPROVE BY: AVAL
CUST. P/N: BGA-142
CUSTOMER: AVALANCHE
JOB# QDS10232_AVL
SCALE: NONE
SIZE : B
REV 0.4
SHEET: 3 OF 4



- BOMs, Board Layout, Gerber File and IBIS/Verilog models are available per request.

4. P-SRAM Evaluation Kit

The Avalanche P-SRAM™ parallel x32 evaluation kit enables the users to evaluate Avalanche's 3rd generation P-SRAM parallel x32 product using a Lattice LCMXO3LF-6900C FPGA connected to Avalanche daughter board via Avalanche proprietary FPGA based Asynchronous SRAM interface. The Lattice LCMXO3LF-6900C FPGA board communicates with the computer using a micro-USB cables type B connector.

The Lattice Mach XO3 evaluation board is a low-cost and easy-to-use development kit used to evaluate and quickly start a development with Avalanche AS3xxGB32 devices. Key features include:

- Small form factor, low cost
- Instant-on boot-up
- Flexible programing I/O expansion – up to 384 I/O pins
- 4 expansion header landings to allow access to user GPIOs
- Supports both 1.8V and 3V I/Os
- Internal oscillator & PLLs
- Custom hardware timing
- Extended temperature flexibility

Figure 8: Avalanche P-SRAM Daughter Board (front and back) with 142-Ball FBGA Socket

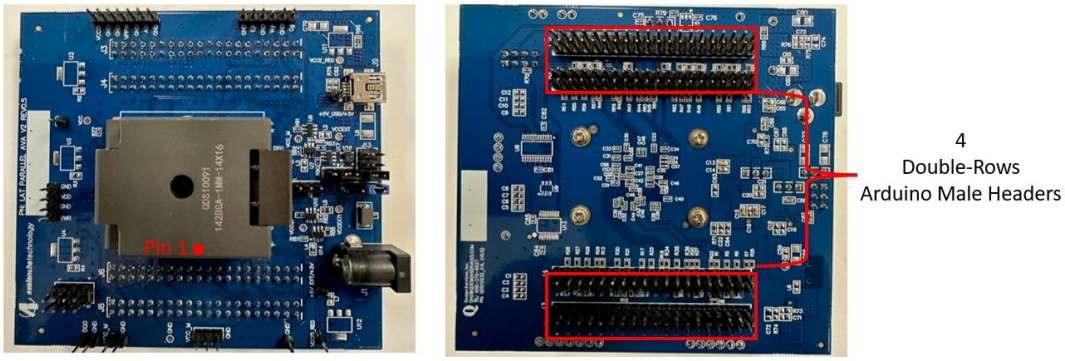
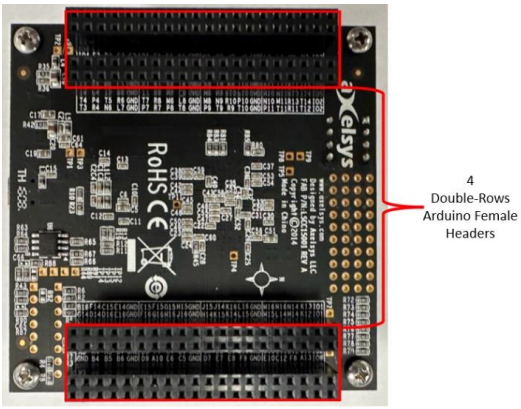


Figure 9: Lattice LCMX03L/LF-6900C FPGA board (back side) with 4 Installed Double-Row Arduino Female Header



Refer to the Eval Kit User Guide for more information on how to use the evaluation kit. Click here to download the user guide.

5. Revision History

Revision	Date	Change Summary
REV A	10/25/2021	Initial release
REV B	01/24/2023	Updated Signal Description Table Updated Power-Up and Power Down Behavior Diagrams and Descriptions Updated Avalanche Daughter Board Photo