Safe and Reliable Power Sequencing for Avalanche Space-Grade High Performance Dual Quad Serial P-SRAM Memory

AN000019 describes method used for implementing safe and reliable power sequencing for Avalanche Space-Grade HP Dual Quad Serial P-SRAM when operating in an Extended Safe Operation Area. It also explains the timing diagrams and provides examples of correct power sequencing using Lattice MachX03 Development Kit.

1. Introduction

The ASxxxx208 is a Spin-Transfer Torque Magnetoresistive Random Access Memory (STT-MRAM). It is offered in densities ranging from 1Gbit to 8Gbit. MRAM technology is analogous to Flash technology in its non-volatility and use cases but has SRAM compatible read/write timings (e.g., no wait states) so it is most aptly designated as Persistent SRAM (P-SRAM). Data is always non-volatile with 10^{16} write cycles endurance and greater than 20-year retention @ 85°C.

Avalanche Space-Grade MRAMs are designed to operate in typical LEO environments which falls within its Safe Operating Area (SOA) without the need for external voltage references. If your mission requirements are higher than a typical LEO environment, Avalanche has provided access for an external voltage reference for enhanced radiation tolerance of the supply to the CMOS circuitry, creating an Extended Safe Operating Area (ESOA). Please reference the available third-party radiation reports for our third generation MRAM devices, provided by request and under nondisclosure. The details for how to achieve this ESOA, for the ASxxxx208 are outlined in this document. When multiple power supplies are used, the supplies must be turned on in a specific sequence for the device to power up in a known, defined state, preventing circuit latch-up or burning out due to unexpected current paths. Specially, for the larger devices, the reference voltage(s) must also be supervised to ensure that the device cannot come out of reset until both voltages reach to the levels within the operating V_{DD}/V_{DD2} voltage range as specified in the device datasheet.

2. Device Power Sequence Overview

The ASxxxx208 has a Serial Peripheral Interface (SPI), a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (low to high) or falling (high to low) or both edges of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data. The ASxxxx208 connects two Quad SPI devices, providing an eight bit I/O data path.

The ASxxxx208 is available in a 96-ball FBGA package. The package has separate balls for CS1#, CLK1#, and INT1 (Dual-Quad SPI device 1) and CS2#, CLK2#, and INT2 (Dual-Quad SPI device 2).

In addition to V_{CC} and V_{CCIO}, the part offers V_{DD} and V_{DD2} which are two reference supply voltages to enable the device to operate reliably in an ESOA. The host is required to supply a V_{DD} power supply of 1V to the device (1Gb-4Gb density) or both V_{DD} and V_{DD2} to the device (8Gb density). Combination of both host's

external V_{DD} and device's internal V_{DD} will ensure a stable voltage source for the device's internal logics to operate reliably and robustly.

In a normal operation, however, the host is not required to supply V_{DD} and/or V_{DD2} to the device. V_{DD} and V_{DD2} should be left as No Connect (NC).

Table 1: Signal Description

Signal	Ball Assignment	Type	Description
CS1#	L7	Input	**Chip Select 1:** When CS1# is driven High, the Quad SPI device 1 will enter standby mode. All other input pins are ignored, and the output pin is tri-stated. Driving CS1# Low enables device 1, placing it in the active mode. After power-up, a falling edge on CS1# is required prior to the start of any instructions.
CLK1	K7	Input	**Clock 1:** Provides the timing for device 1 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT1#	J10	Output	**Interrupt 1:** Output generated by device 1 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI1	M8	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 1 on the rising edge of the clock in Single SPI mode.
IO[0]		Bidirectional	**Bidirectional Data 0 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
SO1	M7	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 1 on the falling edge of the clock in Single SPI mode.
IO[1]		Bidirectional	**Bidirectional Data 1 (QPI):** The bidirectional I/O that transfers data into and out of device 1 in Quad SPI mode.
WP1#	L9	Input	**Write Protect 1 (SPI):** Write protects the status register of device 1 in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only, and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[2]		Bidirectional	**Bidirectional Data 2 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode.
IO[3]	M9	Bidirectional	**Bidirectional Data 3 (QPI):** The bidirectional I/O transfers data into and out of device 1 in Quad SPI mode. This pin can be tied to Vcc if not used.
CS2#	J8	Input	**Chip Select 2:** When CS2# is driven High, the Quad SPI device 2 will enter standby mode. All other input pins are ignored, and the output pin is tri-stated. Driving CS2# Low enables device 2, placing it in the active mode. After

Signal	Ball Assignment	Type	Description
			power-up, a falling edge on CS2# is required prior to the start of any instructions.
CLK2	K6	Input	**Clock 2:** Provides the timing for device 2 serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR • SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only
INT2#	K8	Output	**Interrupt 2:** Output generated by device 2 when an unrecoverable ECC error is detected during read operation (output goes low on error).
SI2	M10	Input	**Serial Data Input (SPI):** The unidirectional I/O transfers data into device 2 on the rising edge of the clock in Single SPI mode.
IO[4]		Bidirectional	**Bidirectional Data 4 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
SO2	N8	Input	**Serial Data Output (SPI):** The unidirectional I/O transfers data out of device 2 on the falling edge of the clock in Single SPI mode.
IO[5]		Bidirectional	**Bidirectional Data 5 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
WP2#	N7	Input	**Write Protect 2 (SPI):** Write protects the status register of device 2 in conjunction with the enable/disa le bit of the status register. This is important since other write protection features are controlled 1through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only, and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used.
IO[6]		Bidirectional	**Bidirectional Data 6 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
IO[7]	N6	Bidirectional	**Bidirectional Data 7 (QPI):** The bidirectional I/O transfers data into and out of device 2 in Quad SPI mode.
RESET#	J9	Input	**RESET:** This is a RESET# signal. When this signal is driven high, the device is in the normal operating mode. When this signal is driven low, the device is in reset mode and the output is High-Z.
V_{CCIO}	G4, P4, G5, J5, P5, M6, H7, H9, N9, J11, M11, G12, P12	Supply	I/O power supply.
V_{SSIO}	M5, H6, L6, P8, H10, N10, P10, H11, N11	Supply	I/O ground supply.
V_{CC}	K4, M4, K5, G7, P7, G9,	Supply	Core power supply.

Signal	Ball Assignment	Type	Description
	K9, P9, K11, K12, M12		
V_{SS}	A1, B1, W1, Y1, A2, Y2, F3, G3, P3, R3, F4, H4, J4, L4, N4, R4, L5, N5, G6, P6, G8, H8, G10, G11, L11, P11, F12, H12, J12, L12, R12, N12, F13, G13, P13, R13, A14, Y14, A15, B15, W15, Y15	Supply	Core ground supply.
V_{DD}	K10	Supply	Supply reference: This is an optional reference supply to allow the safe operating zone in harsh environments to be extended. If not necessary, this ball should be left as a NC.
V_{DD2}	J6	Supply	Supply reference only on the 8Gb device This ball is a NC in 2 cases a) In 1, 2 & 4Gb devices this ball is a NC (not internally connected. They can be driven or left unconnected). b) Same as V_{DD} (Ball K10). If the device is not expected to operate in the extended zone, it should be left as a NC
V_{BYP}	L10	Input	V_{DD} bypass. If the device is not operating in normal mode and not extended Safe Operating Area, this pin should be connected to V_{SS}. See Device initialization sequence extended safe zone for correct operation if this signal is used.
DNU	H5, J7, L8		**Do not use:** DNUs must be left unconnected.

3. Power Sequence in Normal Operation

No requirements are needed for the V_{DD} source in previously defined Safe Operating Area. Refer to datasheet for normal power sequence.

Table 2: V_{DD} and V_{BYD} Requirement in a Normal Operation

Density	512Mb Die	1Gb Die	Host's External V_{DD} Connection Required	Host's External V_{DD2} Connection Required	V_{BYD}
1Gb	x2	-	No (No Connect)	No (No Connect)	Not used (connected to VSS)
2Gb	-	x2			
4Gb	-	x4			
8Gb	-	x8			

4. Power Sequence in ESOA

For the previously defined Extended Safe Operating Area, the host is required to supply a V_{DD} power supply of 1V to the device for the 1Gb, 2Gb and4Gb density devices and both V_{DD} and V_{DD2} to the device for the larger 8Gb density. V_{BYD} signal is used to manage the device's internal V_{DD} source.

Table 3: V_{DD} and V_{BYD} Requirement in ESOA

Density	512Mb Die	1Gb Die	Host's External V_{DD} Connection Required	Host's External V_{DD2} Connection Required	V_{BYD}
1Gb	x2	-	Yes	No	Active
2Gb	-	x2	Yes	No	Active
4Gb	-	x4	Yes	No	Active
8Gb	-	x8	Yes	Yes	Active

4a. Power Up Sequence in ESOA

In an operation mode, both host's V_{DD} power source and device's internal V_{DD} power source are required for the device to operate reliably in ESOA.

With multiple V_{DD} supply voltage sources, it's critical that specific power up sequence is followed as indicated in Figure 1 & 2 below to ensure that each V_{DD} voltage source reaches its target as intended:

1. During Phase 1 of the power up sequence, host must provide V_{DD} of 1V to the device and drive V_{BYP} HIGH to turn off device's internal V_{DD}. V_{BYD} remains HIGH until VDD reaches VDD (min).
2. During Phase 2 of the power up sequence, host must drive V_{BYP} LOW to turn ON device's internal V_{DD}. The device has now been correctly powered up and initialized, receiving dual V_{DD} power sources.

Additional considerations below are also required for power up sequence:

3. For V_{CC}, V_{CCIO}, V_{DD}:
    a. V_{CC} and V_{CCIO} can ramp together if not possible then V_{CC} first followed by V_{CCIO}.
    b. V_{DD} supply should be kept low until V_{CC} and V_{CCIO} has reached their minimum voltage values.
    c. There are no timing requirements between the power supplies if the sequence is followed
4. It is recommended that no instructions are sent to the device before completion of power up sequence
    a. CS# cannot be active during power-up (a 10KΩ pull-up Resistor to V_{CC} is recommended)
5. During Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences

Figure 1: Key Parameters Required during Power Up Sequence

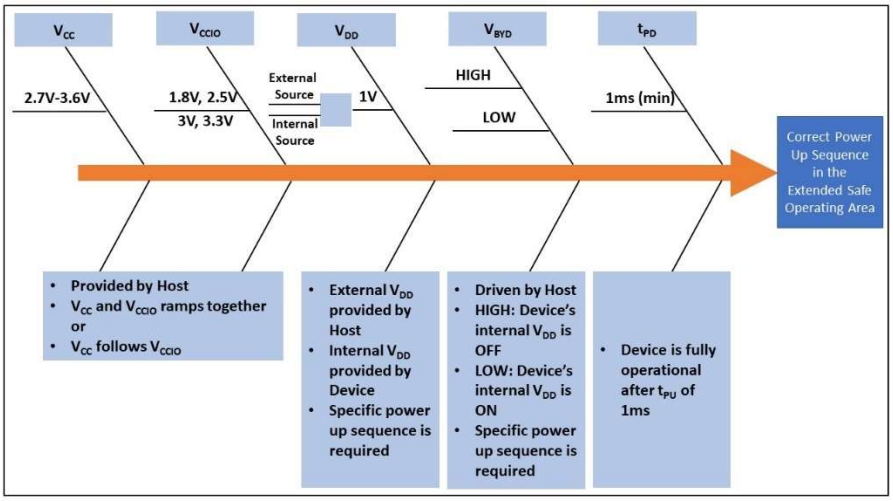
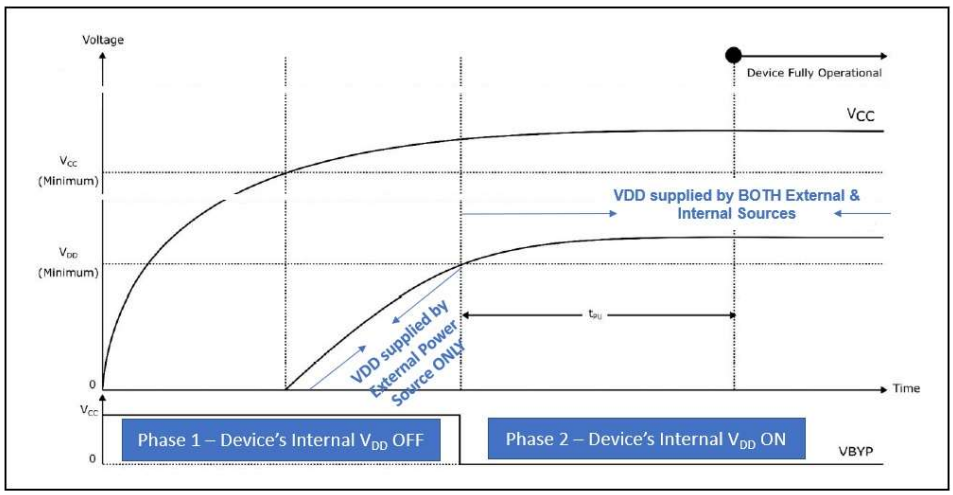


Figure 2: Power Up Sequence



4b. Power Down Sequence in ESOA

The following procedure is required to power down the device correctly:

- It is recommended to power down all supplies together. If not possible then the following sequence must be followed: 1-V_{CC}, 2-V_{CCIO}, 3-V_{DD}.
- Timing for Ramp down rate should follow ramp down time (R_{VF}).
- CS# cannot be active during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended).
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} minimum.
- During power loss or brownout, if V_{CC} goes below $V_{CC\text{-}CUTOFF}$ or V_{DD} goes below $V_{DD\text{-}CUTOFF}$. All supply voltages V_{CC}, V_{CCIO} and V_{DD} must be dropped below their respective (RESET) values V_{CC_RST} and V_{DD_RST} for a period of t_{PD}. Figure 2 timing needs to be observed for the subsequence power-up.

Figure 3: Power Down Sequence

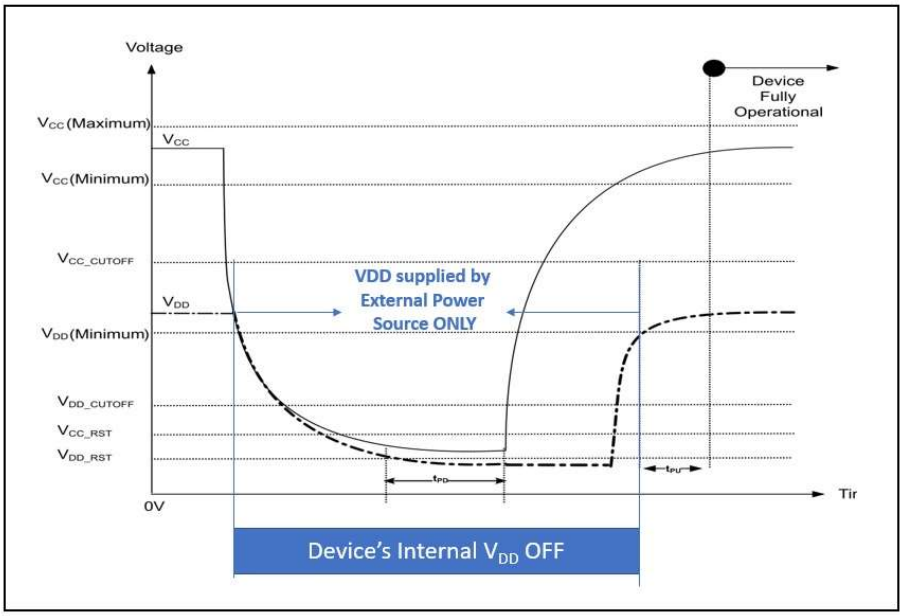


Table 4: Power Down Timing and Voltages

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{DD} Range			0.90	-	1.05	V
V_{CC} Ramp Down Time	R_{VF}		20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}		1	-	-	ms
V_{CC} (low) time	t_{PD}		1			ms

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC} Cutoff – Must Initialize Device	$V_{CC\text{-}CUTOFF}$		1.6	-	-	V
V_{CC} (Reset)	V_{CC_RST}		0		0.3	V
V_{DD} Range			0.9	-	1.05	V
V_{DD} Cutoff – Must initialize Device	V_{DD_CUTOFF}		0.6	-	-	V
V_{DD} (Reset)	V_{DD_RST}		0	-	0.15	V

5. Lattice MachX03 Development Kit

The Lattice development kit uses TI 3-Pin Voltage Supervisors TLV810x to ensure the V_{DD} reference voltage has to be at 1.1V threshold before the device can power up correctly for safe operation.

As figure 4 below indicated, during power up, the TLV810 monitors the V_{DD} voltage rail and stays in RESET until V_{DD} reaches 1.1V or higher threshold. During power down, the TLV810 also monitors the V_{DD} voltage rail and stays in RESET after V_{DD} reaches below 1.1V threshold.

Refer to the schematic, BOMs and layout for complete implementation method of host's external VCC, VCCIO, VDD and VDD2.

Figure 4: TI Voltage Supervisors/Detectors

TI Voltage Supervisors/Detectors

TLV810M, TLV810R
TLV810S, TLV810Z

TEXAS INSTRUMENTS

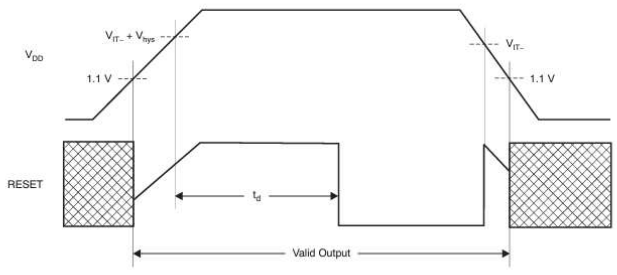
SBVS158A – APRIL 2011 – REVISED JUNE 2011 www.ti.com

SWITCHING CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

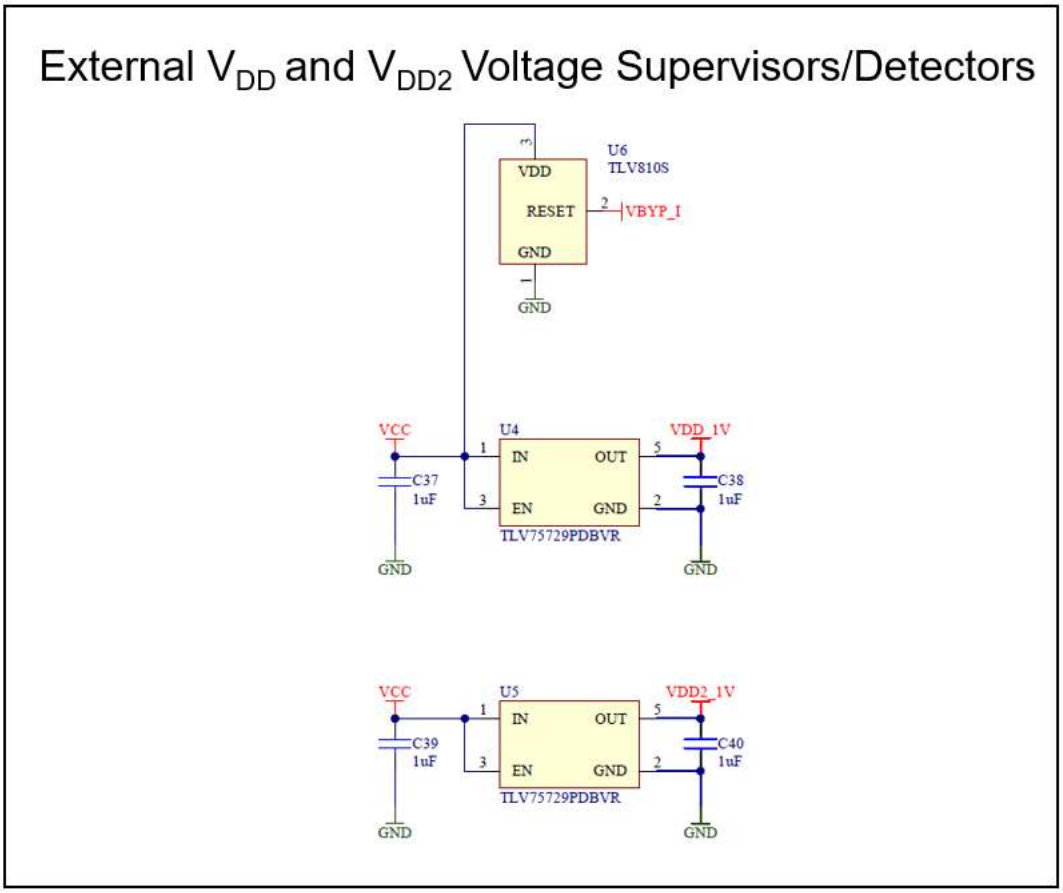
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width at V_{DD}	V_{DD} = 1.08 V_{IT-} to 0.92 V_{IT-}		1		µs
t_d	Delay time	$V_{DD} \geq V_{IT-}$ + 0.2 V; see Timing Diagram	120	200	280	ms

TIMING DIAGRAM



Source: https://www.ti.com/product/TLV810

Figure 5: Host's external V_{DD} and V_{DD2} Supervisors Circuits



5a. Avalanche 96-Ball FBGA Schematic & BOMs

Figure 6: Schematic – Avalanche 96-Ball FBGA

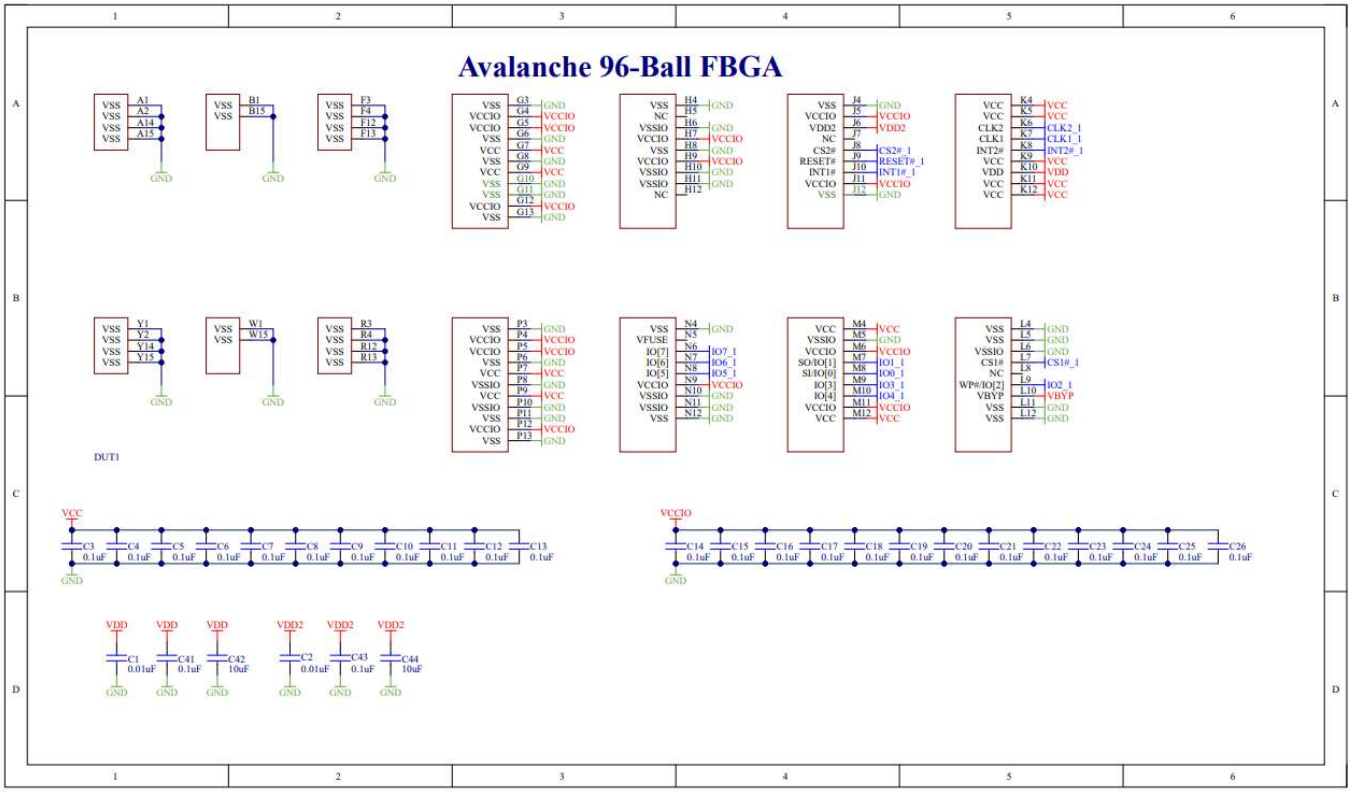


Figure 7: Schematic – Avalanche 96-Ball FBGA Connection to Lattice MACHXO3 Development Kit

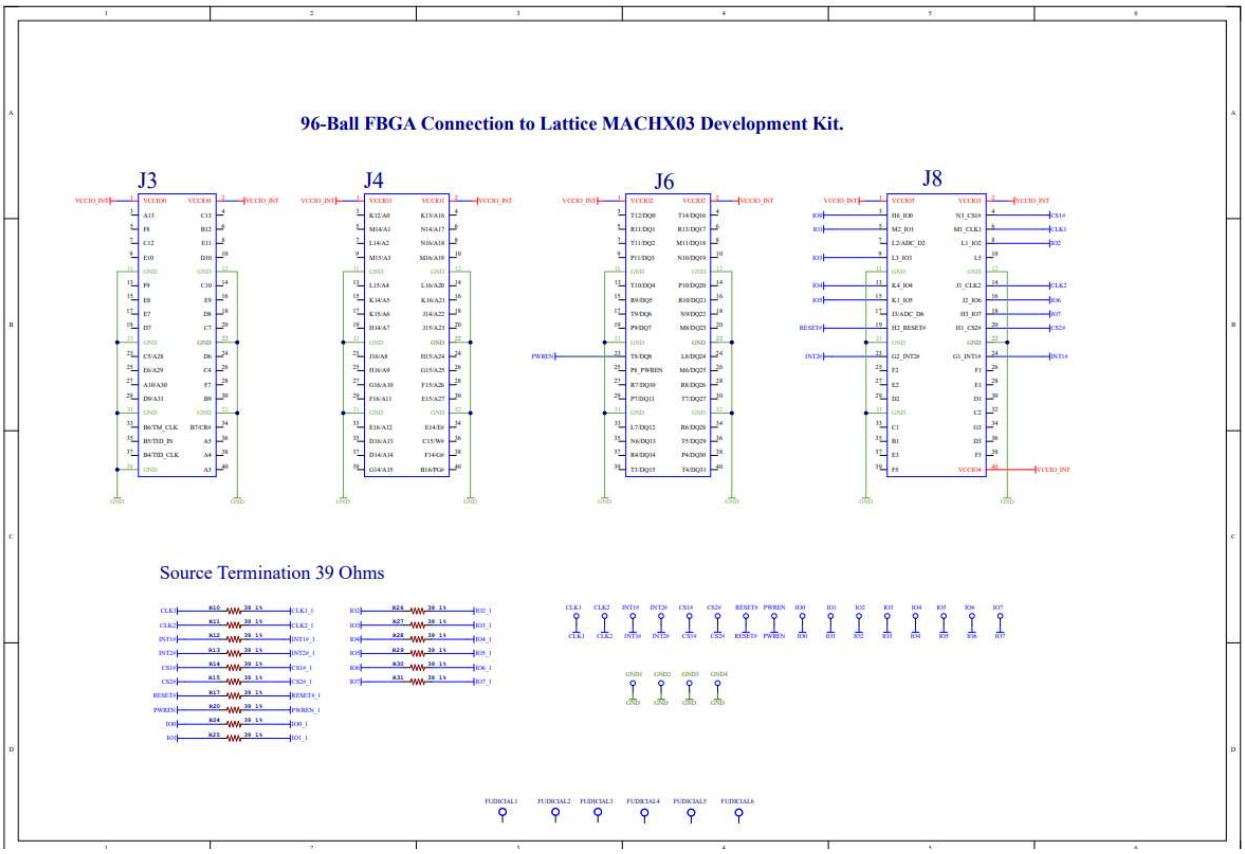


Figure 8: Schematic – Power Supply

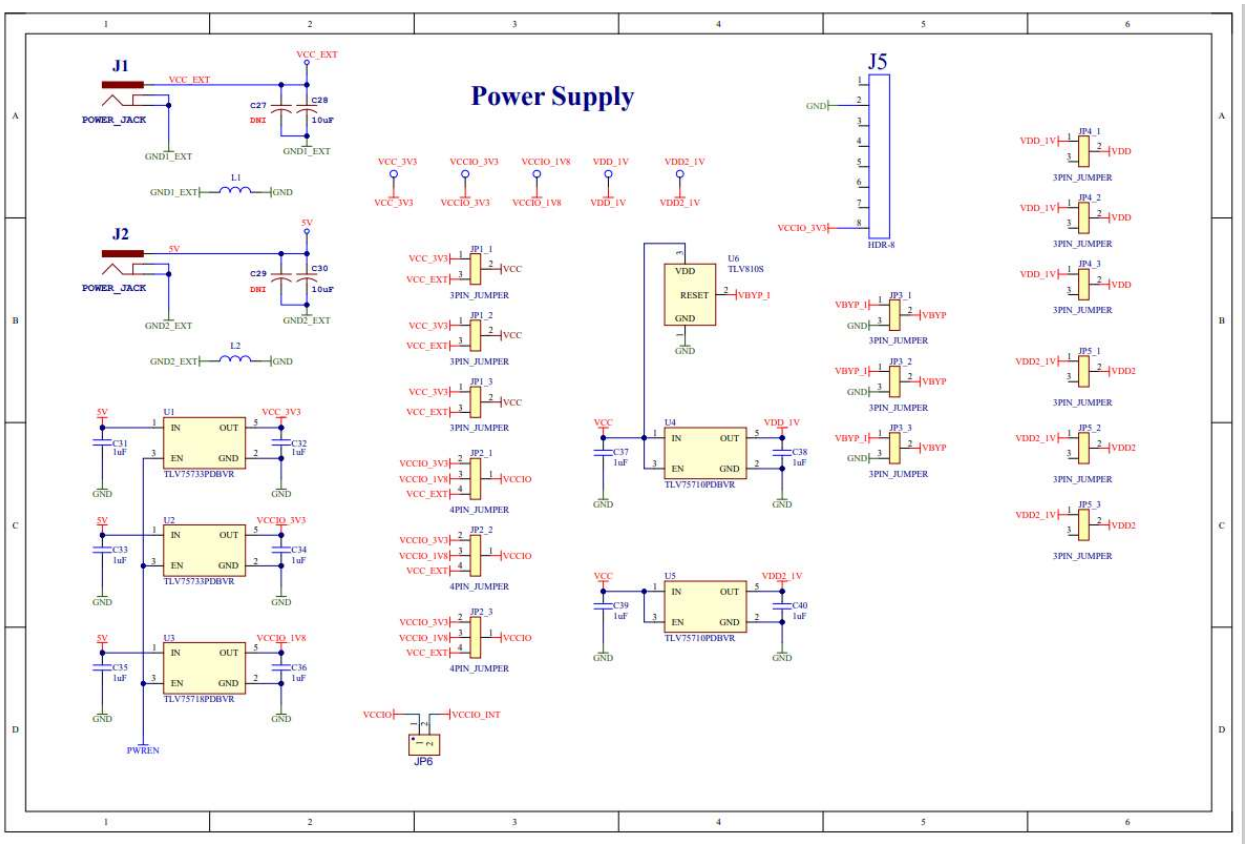


Figure 8: Board Layout (1 of 3)

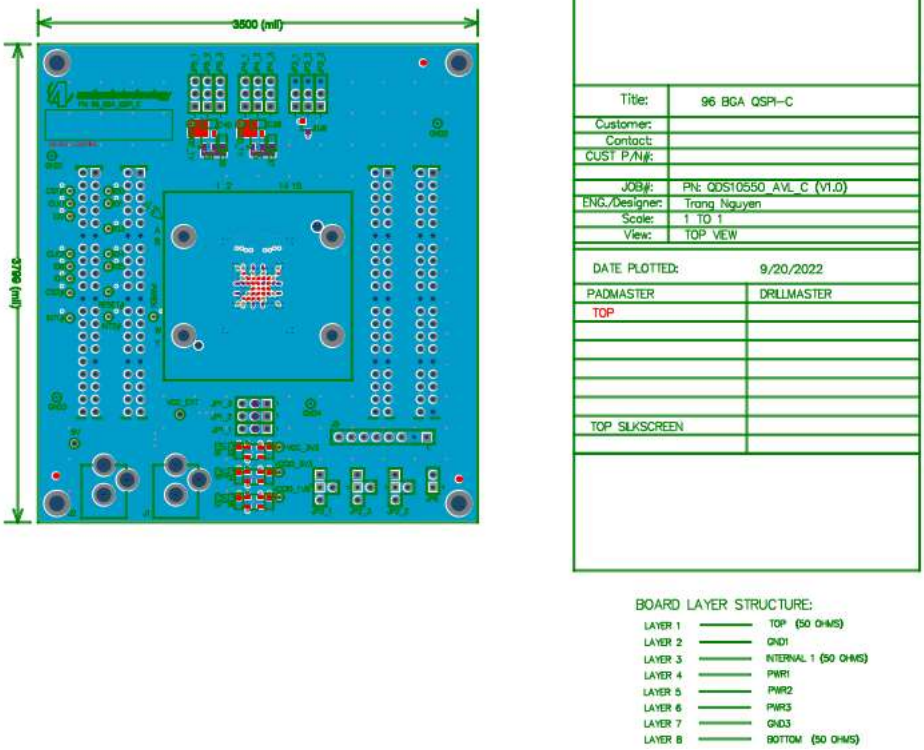
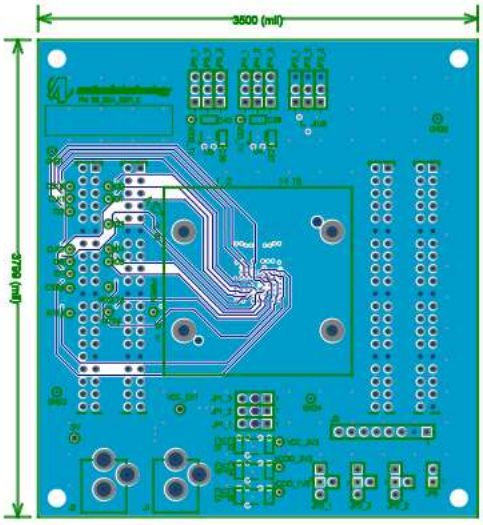


Figure 9: Board Layout (2 of 3)

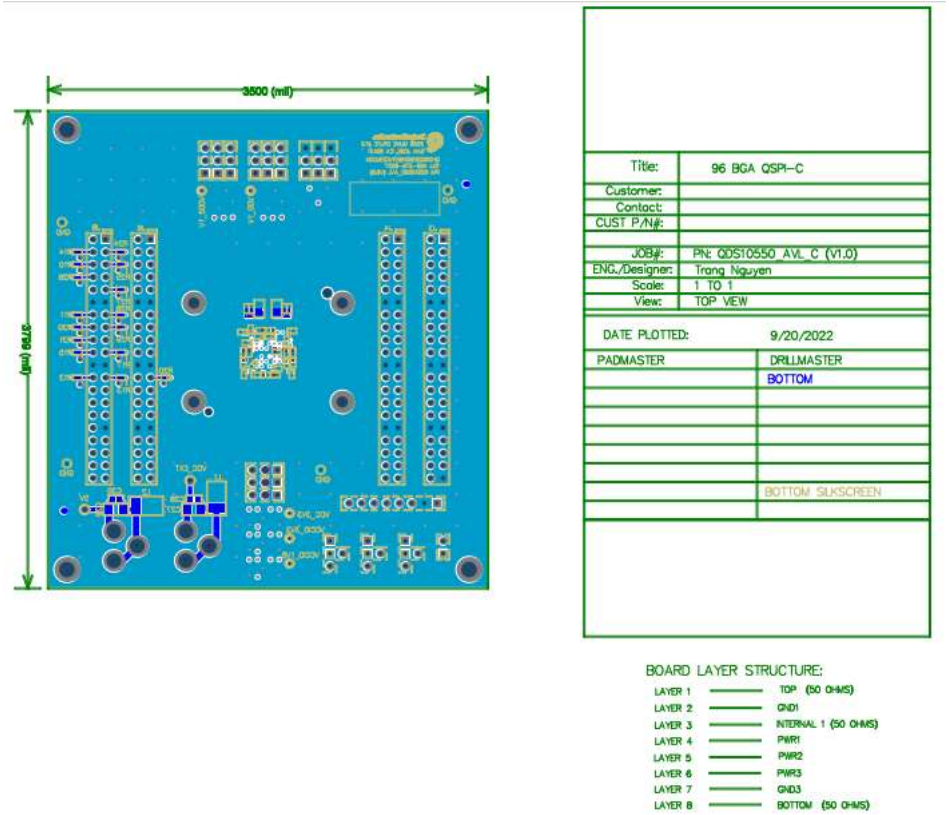


Title:	96 BGA QSPI-C
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: QDS10550_AVL_C (V1.0)
ENG./Designer:	Trang Nguyen
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED:	9/20/2022
PADMASTER	DRILLMASTER
INTERNAL1	
TOP SILKSCREEN	

BOARD LAYER STRUCTURE:

LAYER 1	TOP (50 OHMS)
LAYER 2	GND1
LAYER 3	INTERNAL 1 (50 OHMS)
LAYER 4	PWR1
LAYER 5	PWR2
LAYER 6	PWR3
LAYER 7	GND3

Figure 10: Board Layout (3 of 3)



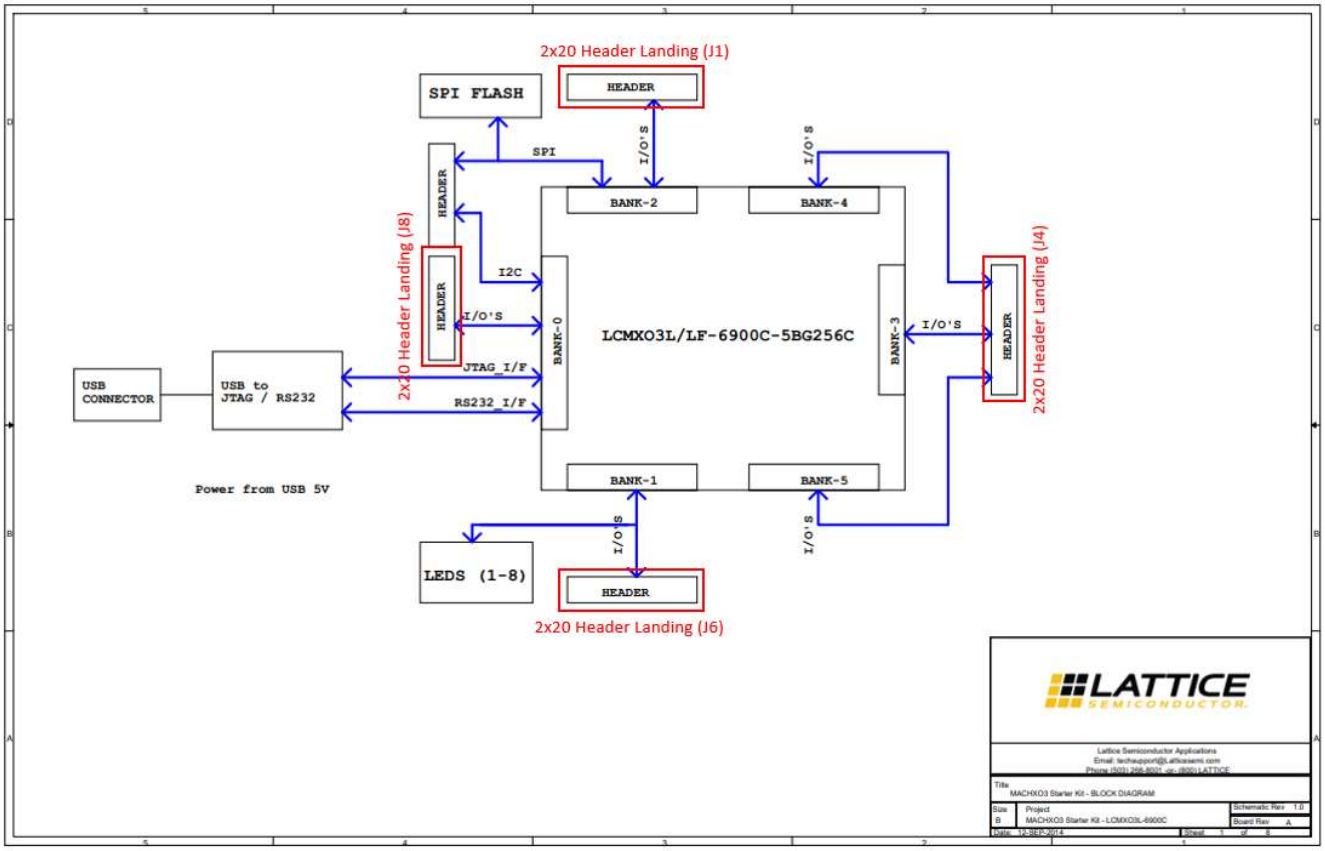
BOMs

Quantity	Reference	Description	Designator	Footprint
2	Test Point		5V, VCC_EXT	Test Point
2	0.01uF	CAP CER 10000PF 50V X7R 0402	C1, C2	N_0402
26	0.1uF	CAP CER 10000PF 50V X7R 0402	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C41, C43	N_0402
2	DNI	DNI	C27, C29	N_1206
2	10uF		C28, C30	N_0603
10	1uF		C31, C32, C33, C34, C35, C36, C37, C38, C39, C40	N_0603

Quantity	Reference	Description	Designator	Footprint
2	10uF	CAP CER 10000PF 50V X7R 0402	C42, C44	N_0805
25	Test Point		CLK1, CLK2, CS1#, CS2#, GND1, GND2, GND3, GND4, INT1#, INT2#, IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7, PWREN, RESET#, VCC_3V3, VCCIO_1V8, VCCIO_3V3, VDD2_1V, VDD_1V	Test Point 40X20_010819
1	Avalanche 96-Ball FBGA		DUT	96-Ball FBGA
6	Fudicial		FUDICIAL1, FUDICIAL2, FUDICIAL3, FUDICIAL4, FUDICIAL5, FUDICIAL6	FUDICIAL
2	Power Jack		J1, J2	POWER_JACK_PTH
4	2x20 Header Landing 100mil		J3, J4, J6, J8	2X20-HEADER
1	HDR-8		J5	HDR1X8
12	3-Pin Jumper		JP1_1, JP1_2, JP1_3, JP3_1, JP3_2, JP3_3, JP4_1, JP4_2, JP4_3, JP5_1, JP5_2, JP5_3	JUMPER_3PIN
3	4-Pin Jumper		JP2_1, JP2_2, JP2_3	JUMPER_4PIN
1	HDR-TH 2P-P2.54		JP6	1X2 HEADER WITH SHUNT_051914
2		Ferrite Beads 43 SM BEAD Z=47 OHM @ 100MHz	L1, L2	FB_274301944
16	39 1%	RES 39 OHM 1% 1/16W 0402	R10, R11, R12, R13, R14, R15, R17, R20, R24, R25, R26, R27, R28, R29, R30, R31	N_0402
2	TI TLV75733PDBVR		U1, U2	SOT23-5
1	TI TLV75718PDBVR		U3	SOT23-5
2	TI TLV75710PDBVR		U4,U5	SOT23-5
1	TI TLV810S		U6	SOT23-3

5b. Lattice MACHXO3 Block Diagram & Schematic

Figure 11: Lattice MACHXO3 Block Diagram



Note: Avalanche 96-Ball FBGA test board is connected to the Lattice MACHXO3 development kit via 4 sets of 2x20 Header Landings 100mil (J3, J4, J6, J8).

MACHXO3 development kit user guide including expansion header pin functions, schematic, and BOMs can be downloaded here.

Figure 12: Lattice MACHXO3 Schematic – USB Interface to JTAG

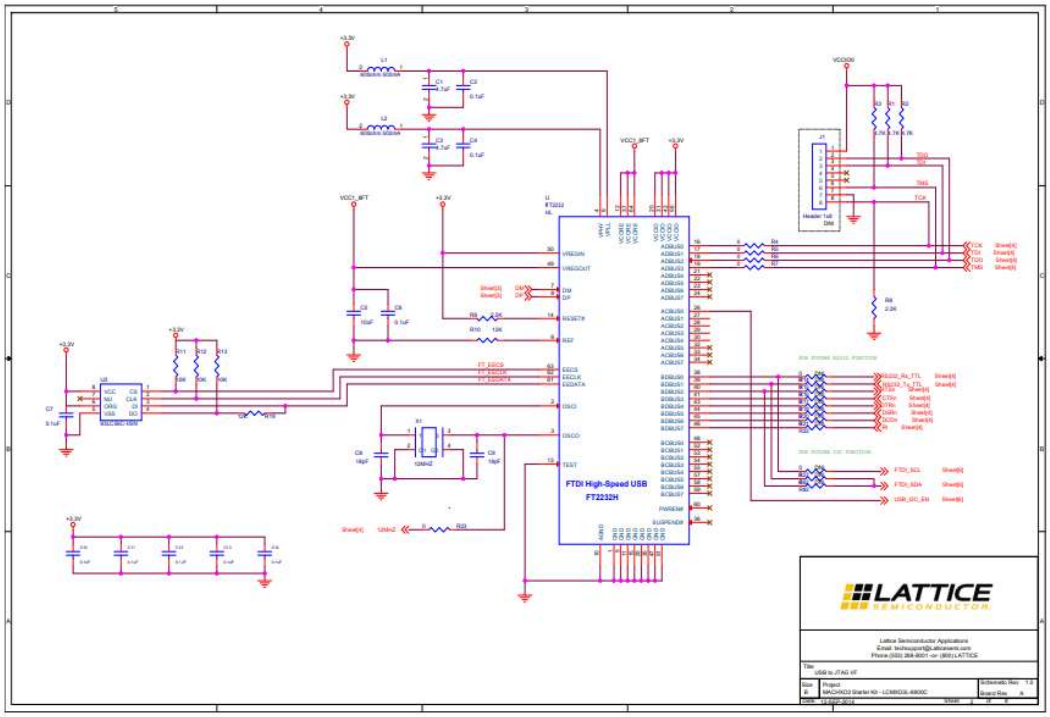


Figure 13: Lattice MACHXO3 Schematic – FPGA

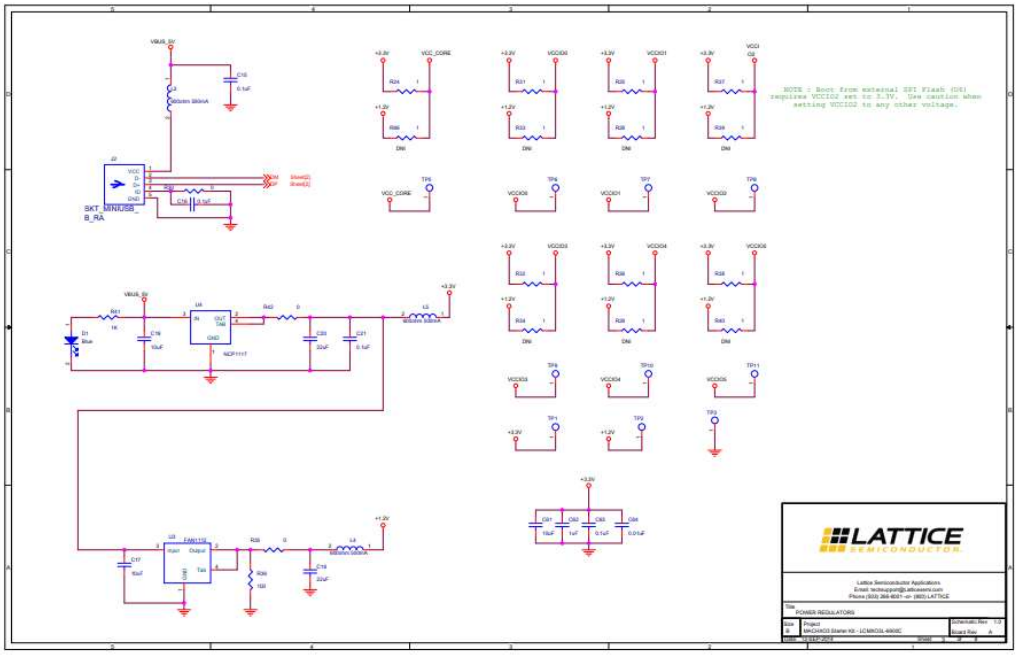


Figure 14: Lattice MACHXO3 Schematic – FPGA

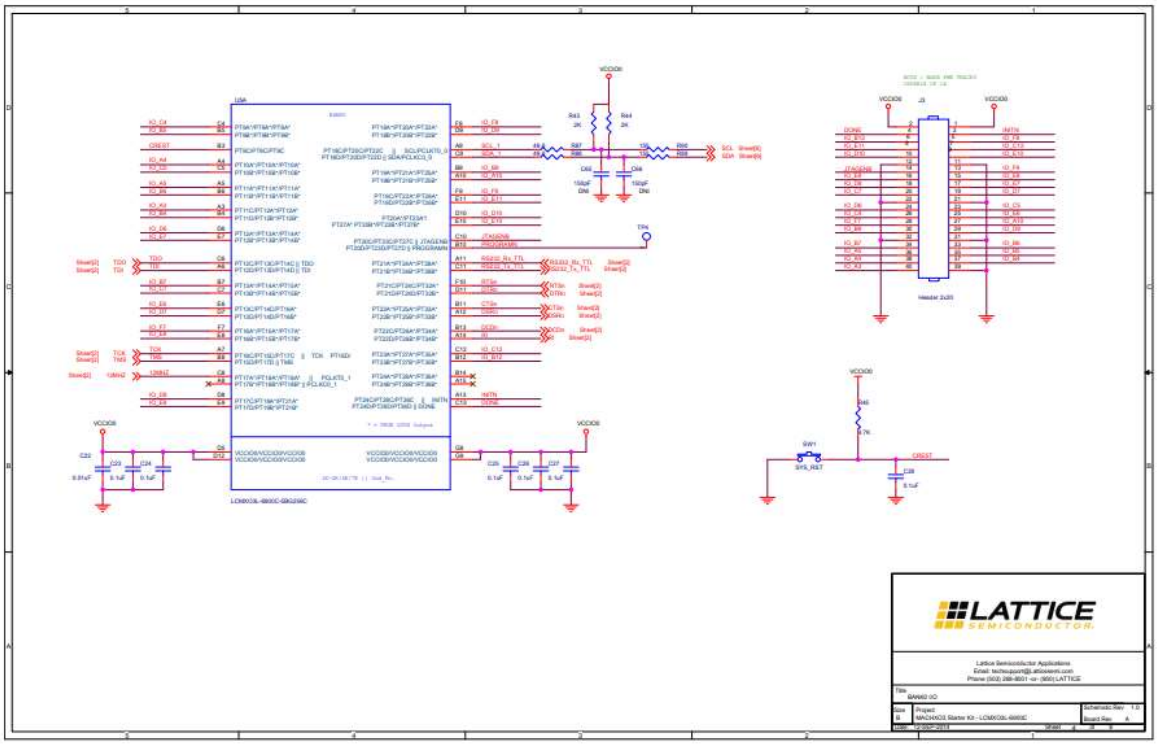


Figure 15: Lattice MACHXO3 Schematic – Power LEDs

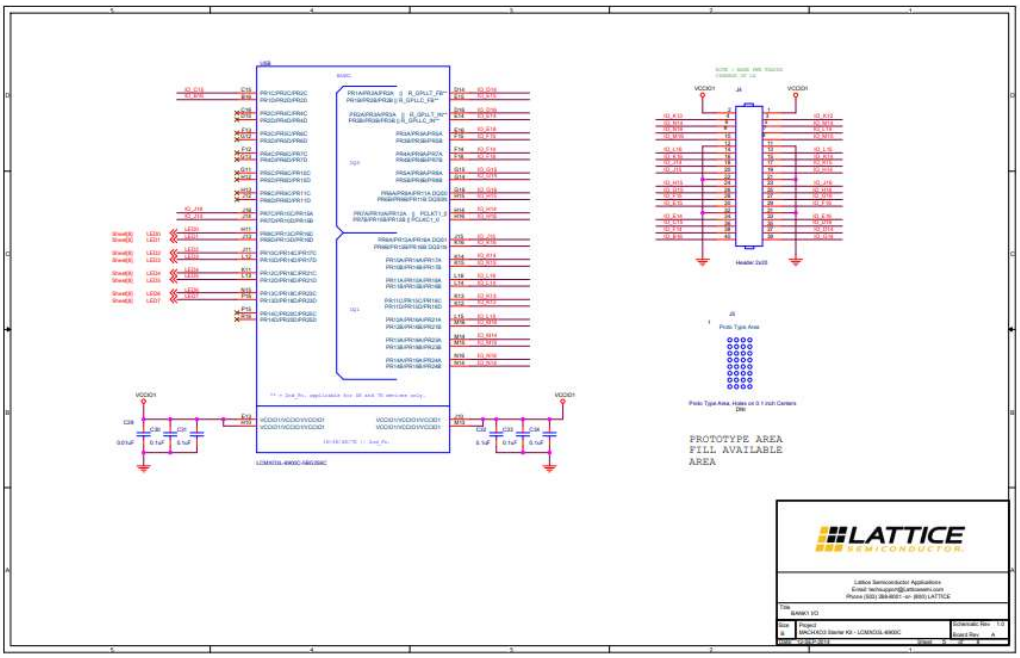


Figure 16: Lattice MACHXO3 Schematic – Bank 2 I/O

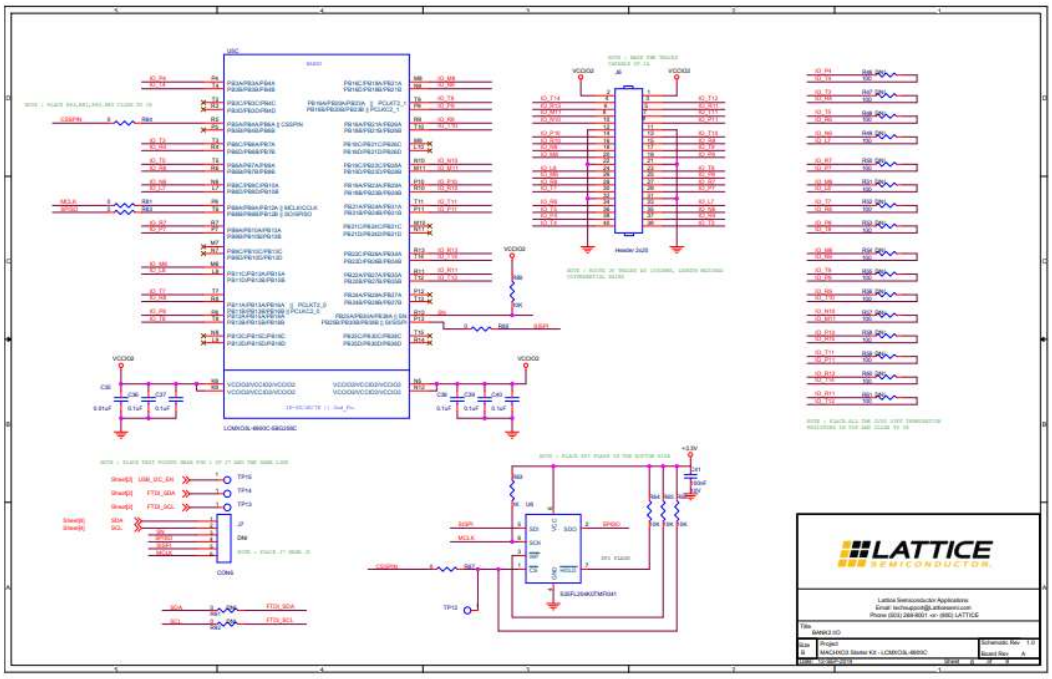


Figure 17: Lattice MACHXO3 Schematic – Bank 3,4,5 I/O

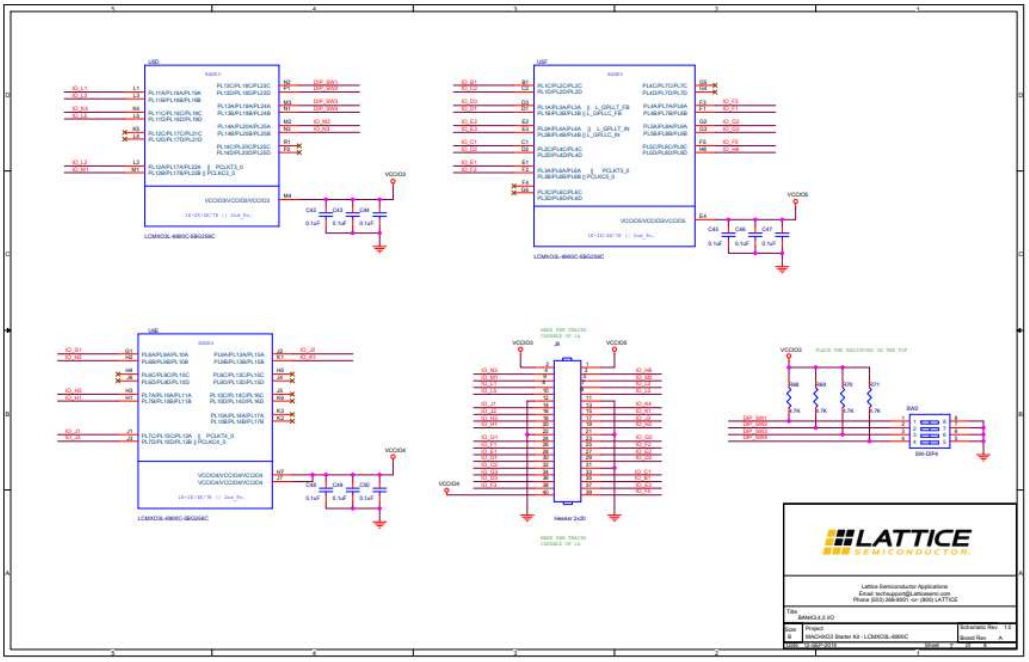
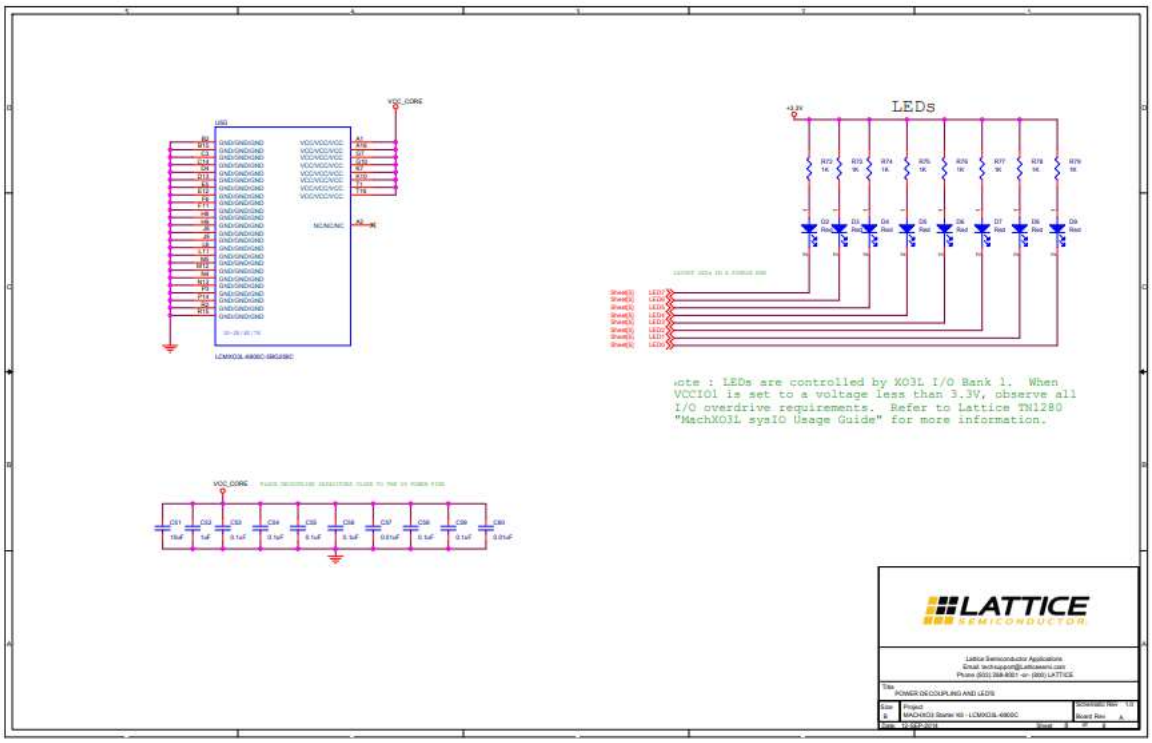


Figure 18: Lattice MACHXO3 Schematic – Power Decoupling and LEDs



10. Revision History

Revision	Date	Change Summary
REV A	07/30/2022	Initial release
REV B	09/21/2022	Updated Ava schematic, added Lattice MACHXO3 schematic