

Programming the Avalanche Dual Quad SPI P-SRAM Memory through JTAG in the Xilinx KCU105 Evaluation Platform

AN000022 serves as a quick guideline to programming the Avalanche project with Vivado on the Kintex UltraScale KCU105 Evaluation Platform. It covers project setup, script execution, device programming, and SPI memory programming

1. Introduction

The KCU105 evaluation board for the Xilinx Kintex UltraScale FPGA provides a hardware environment to program an Avalanche Dual Quad SPI P-SRAM memory device through JTAG connection and boot the device in the QSPI mode.

This application note provides detailed steps to configure the KCU105 in the JTAG mode, program the FPGA bitstream, and boot up the Avalanche Dual Quad SPI P-SRAM memory device in the QSPI mode.

Other program and/or boot options are outside of the scope of this application note.

2. Requirements

- Xilinx Vivado 2022.2 or later
- A Xilinx Kintex UltraScale KCU105 evaluation board
- USB-JTAG connection with micro-B USB connector
- An Avalanche DQSPI MRAM memory device
- An optional Avalanche flexible 96/224-ball FBGA to 16-pin SOIC cable adapter
- Avalanche project files and scripts:
 - AVA_MRAM_write.tcl
 - moving_led_compressed.hex
 - AVA_MRAM_Flashprogrammer_top.bit

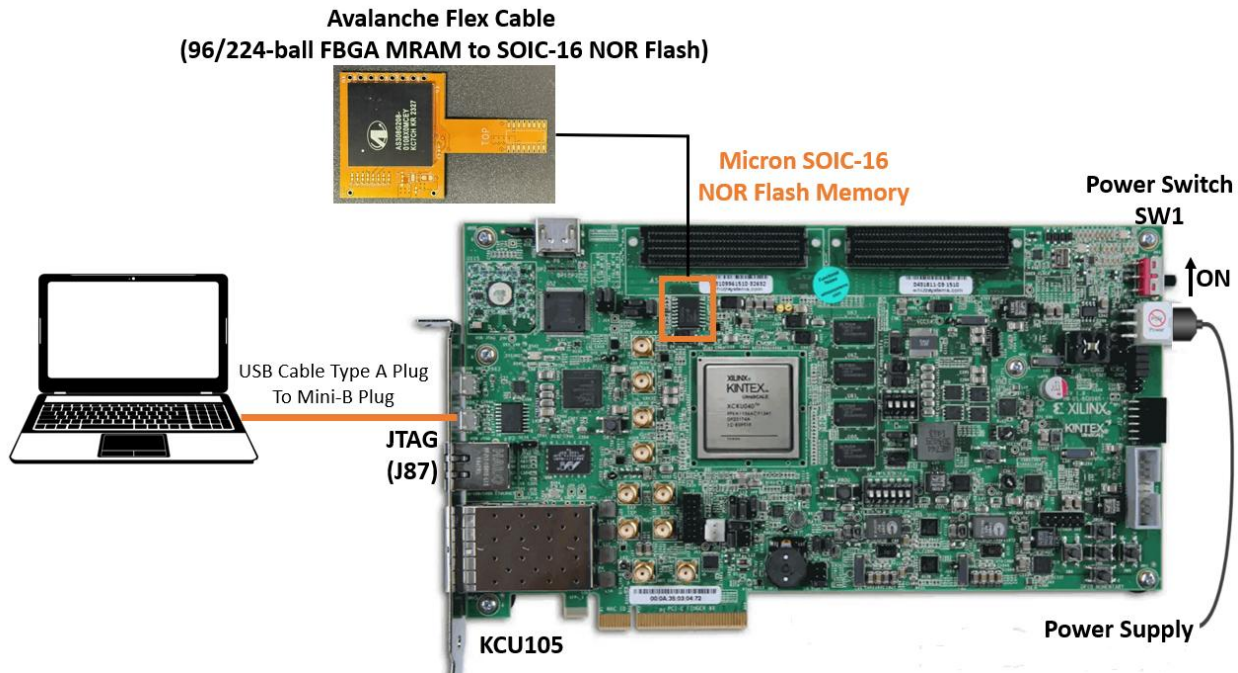
Click [here](#) to download the project files and scripts.

3. Configuration

The configuration scheme includes the following steps:

3.1 Setting up KCU105

1. Connect an Avalanche DQSPI MRAM device to KCU105 using optional_Flexible cable to replace the existing Micron NOR Flash memory as shown below.
2. Place switch SW1 to the OFF position and connect the power supply.
3. Connect the USB cables between the computer and the and JTAG connector (J87) on the KCU105 board and the computer.
4. Turn switch SW15.6 ON and SW15.5 OFF to configure KCU105 in JTAG mode.
5. Turn on KCU105 power.



3.2 Creating Vivado Project

- Open Vivado design tool
- Navigate to "File > Project > New"
- Follow the prompt:
 - Set a "Project Name" and "Location"
 - Select "RTL Project"
 - Proceed through default steps by clicking "Next"
- On the "Parts" tab, select "xcku040-ffva1156-2-e"

- Click “Next” then “Finish”

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Category: All

Package: fva1156

Temperature: E

Family: Kintex UltraScale

Speed: -2

Static power: All Remaining

Search: Q: XCKU040

(1 match)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	HNICX
xcku040-fva1156-2-e	1156	520	242400	484800	600	0	1920	

< Back

Next >

Finish

Cancel

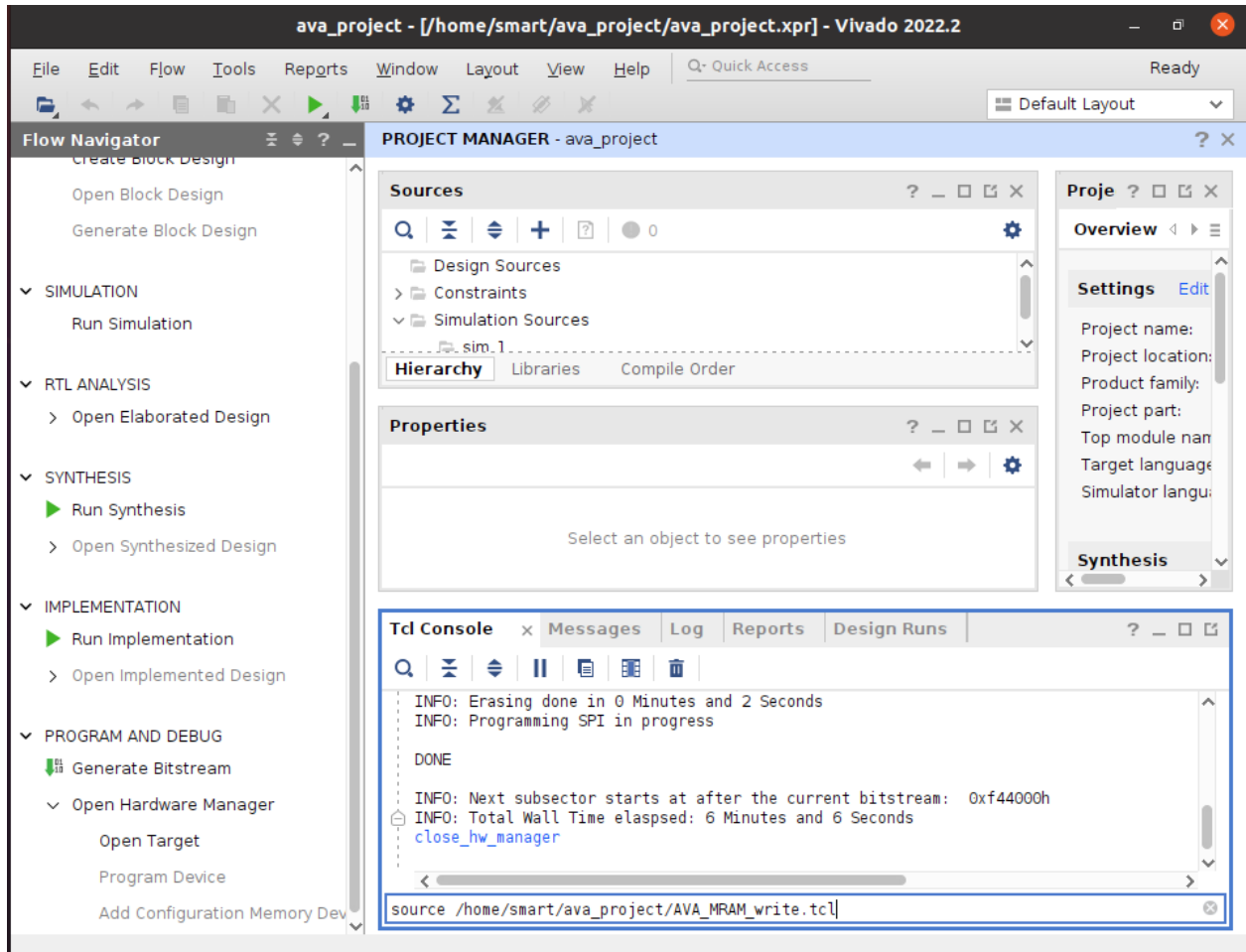
Create a new project

Copy these files to the Project Directory:

- AVA_MRAM_write.tcl
- moving_led_compressed.hex
- AVA_MRAM_flashprogrammer_top.bit

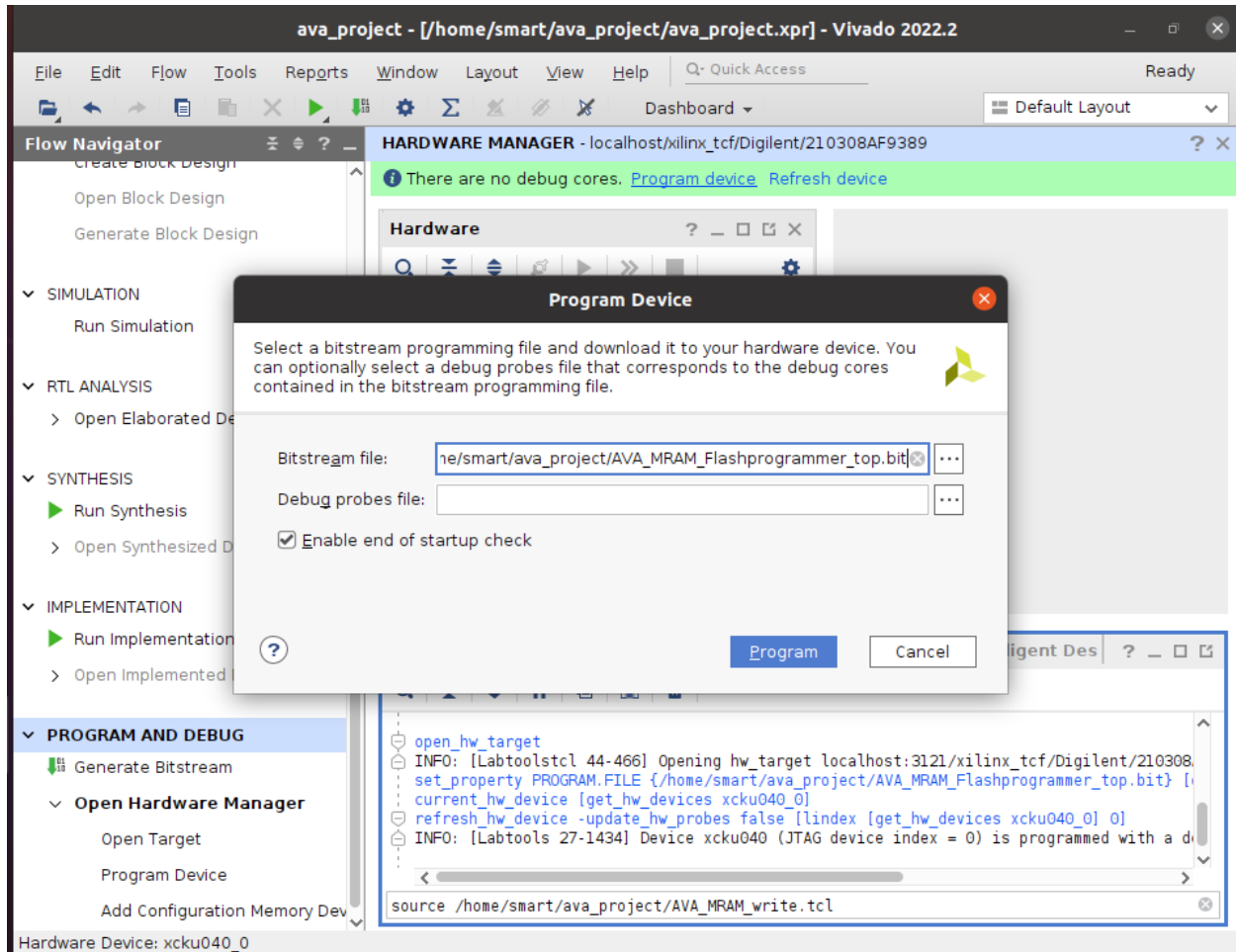
3.3 Loading the SPI Programming Scripts

- Open Vivado and navigate to the “Tcl Console” tab
- Enter the following commands as shown in screenshot below:
 - `Source~/avaXapp/ AVA_MRAM_write.tcl`



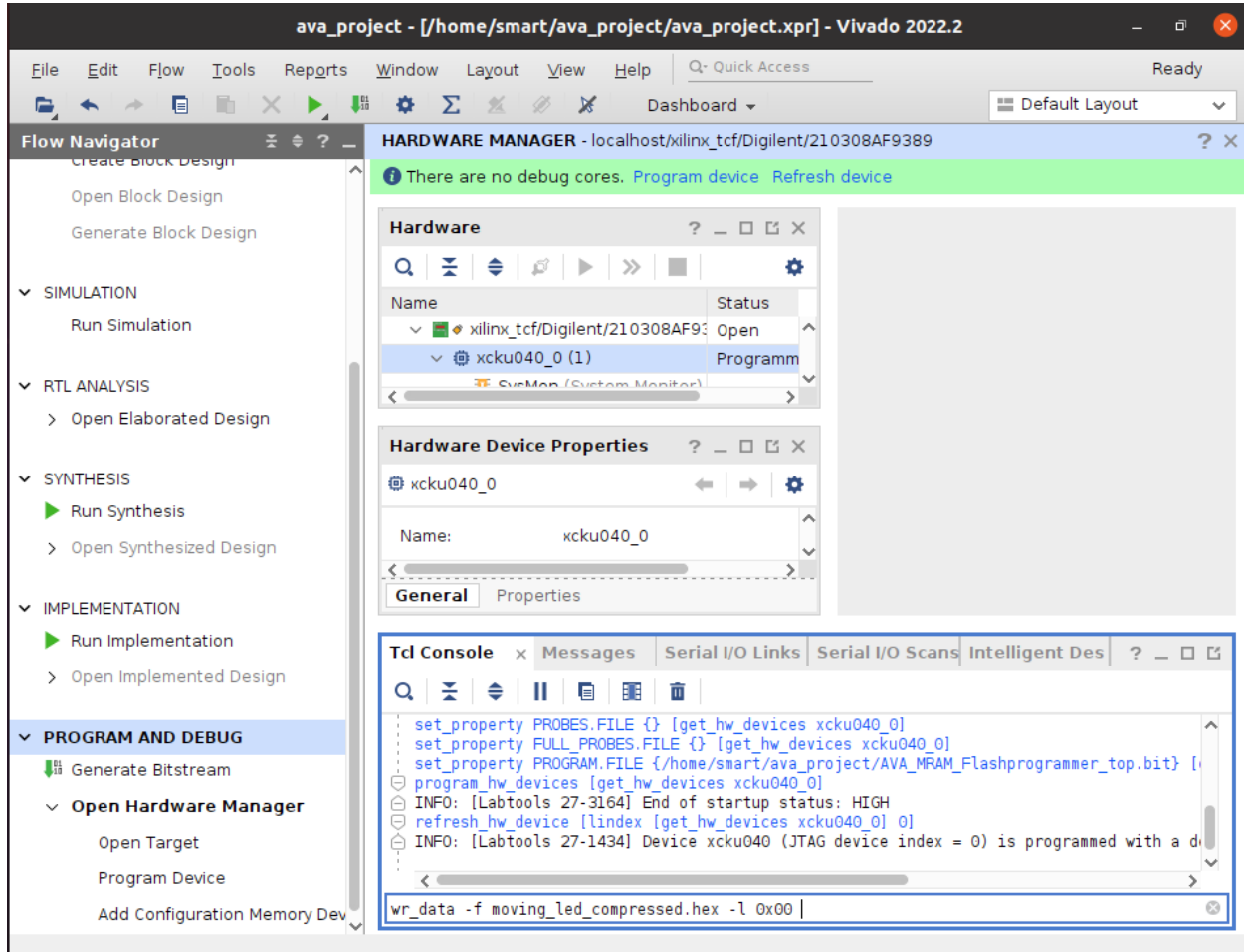
3.4 Programming the FPGA Bitstream

- In the “Flow Navigator”, navigate to “Program and Debug > Open Hardware Manager”
- Click on “Open Target > Auto Connect”
- In the upper right corner window, click on “Program Device”
- In the pop-up dialog, confirm the “.bit” file path and then click on “Program”



3.5 Writing the HEX File to the Avalanche Dual Quad SPI P-SRAM

- In the “Tcl Console”, type: `wr_data -f moving_led_compressed.hex -l 0x00`



3.6 Booting the Avalanche Dual Quad SPI P-SRAM in the Single Quad SPIx4 Mode

To boot the Avalanche P-SRAM memory device in a single Quad SPIx4 mode, follow the steps below:

- Turn switch SW15.1 through SW15.6 OFF
- Power up the KCU105 board. The LEDs should now blink to indicate that the QSPI boot is successful

Alternatively, the user can copy the Avalanche provided project file and then follow steps 3.2 through 3.6. The user can program a custom hex file by copying it to the project directory and substitute the hex file in step 3.5 of the configuration procedure.

Revision History

Revision	Date	Change Summary
REV A	04/15/2025	Initial release