Decoupling Capacitor Selection and Placement in P-SRAM Memory Systems

AN000023 provides design recommendations for optimal decoupling capacitor selection and PCB integration in P-SRAM memory systems. Proper decoupling practices are essential to maintain power integrity, suppress noise, and ensure robust signal performance in memory system designs.

Overview

In high-speed P-SRAM memory systems, decoupling capacitors play a critical role in stabilizing supply voltages by providing a low-impedance path between the power rails (VCC, VCCIO) and ground. Effective decoupling suppresses voltage transients and reduces simultaneous switching noise, improving overall system reliability.

Design Guidelines

1. Capacitance Selection and Proximity Placement

- Use 0.01µF and 0.1µF ceramic capacitors connected in parallel per VCC and VCCIO pin to ensure noise suppression across a wide frequency spectrum.
- Position capacitors within 2 mm of the corresponding power pins to reduce parasitic inductance resistance.
- If same-side placement is not feasible, locate the capacitors on the opposite PCB side directly beneath the power pins to maintain a short, low-impedance connection.

2. Per-P-SRAM Memory Device Capacitor Allocation

Allocate one 10µF ceramic capacitor for each active P-SRAM device. Bulk decoupling capacitors avoids shared impedance paths that can lead to power noise coupling across P-SRAM devices.

3. PCB Layer Consistency

Whenever possible, mount decoupling capacitors on the same PCB layer as the P-SRAM memory device. Keeping the power delivery path on a single layer minimizes loop inductance and enhances current return path efficiency.

4. Via and Trace Routing Optimization

- Route short, wide traces (≥10 mils) between capacitor terminals and power/ground vias to reduce series impedance.
- Place vias immediately adjacent to capacitor pads to connect directly to internal power and ground planes.
- Avoid routing signal traces between capacitor pads and associated vias, as this introduces parasitic inductive loops and degrades high-frequency decoupling performance.

Conclusion

Following these decoupling guidelines is essential for stable and reliable P-SRAM operation, particularly in high-speed or noise-sensitive environments. Careful consideration of capacitor selection, placement, and routing will significantly enhance power delivery and noise immunity in your memory subsystem.

Revision History

Revision	Date	Change Summary
REV A	05/12/2025	Initial release