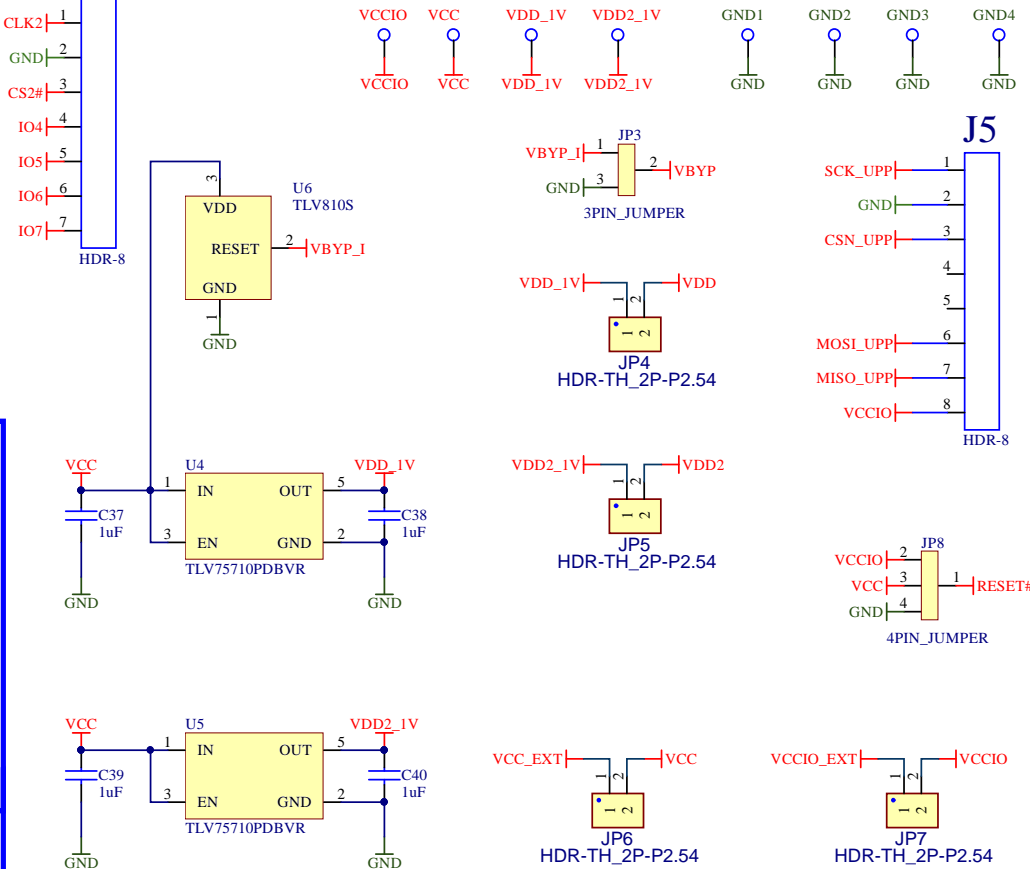
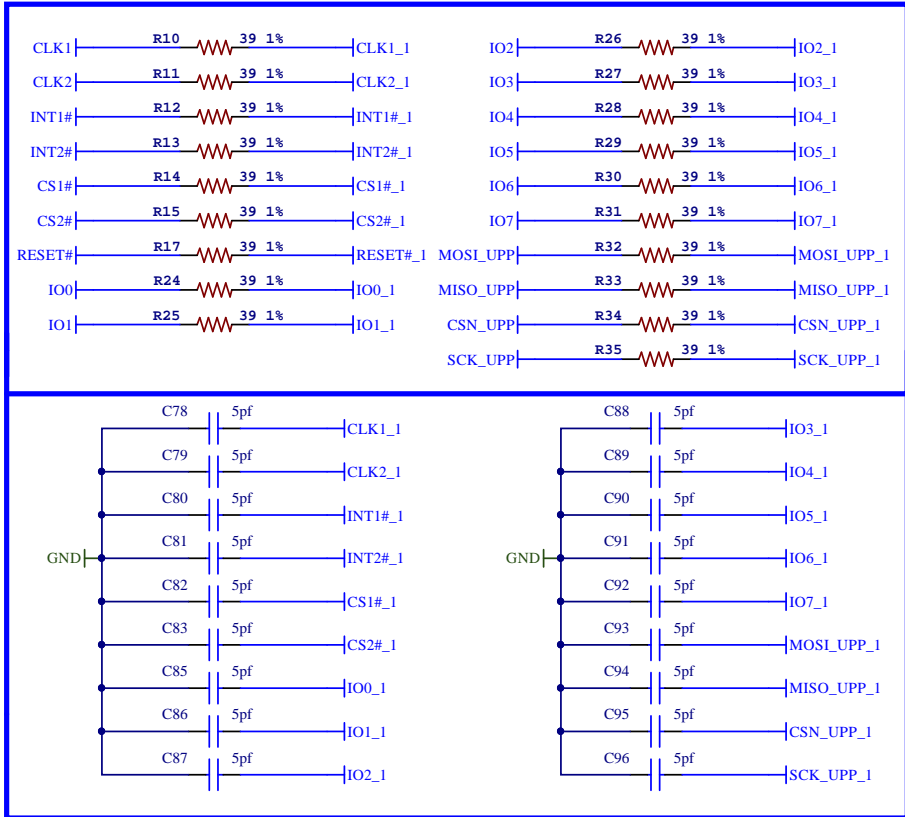
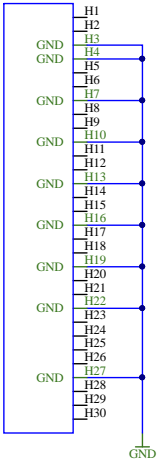
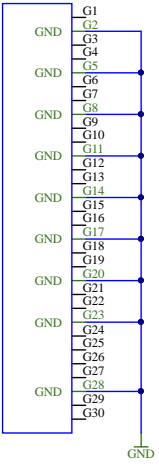
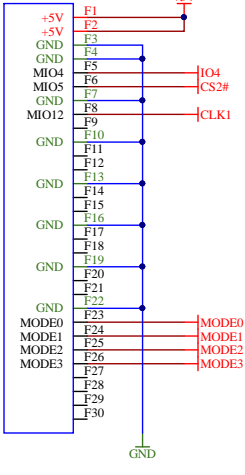
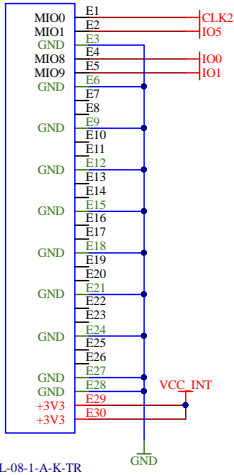
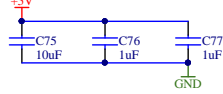
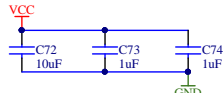
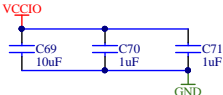
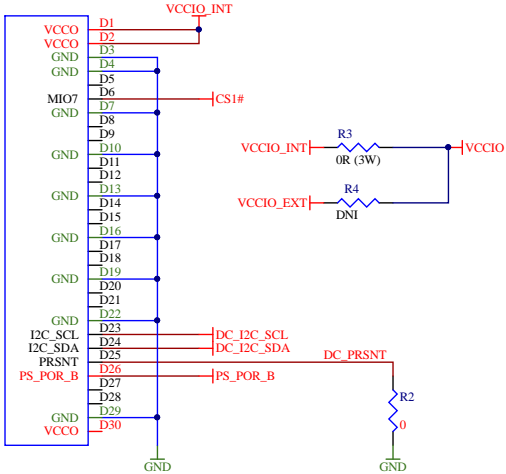
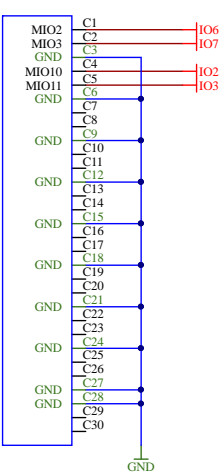
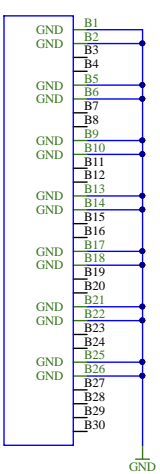
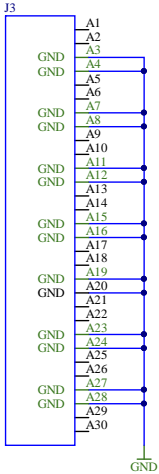


Source Termination 39 Ohms



		TITLE: 96BGA XILINX			
DESIGNED BY: Avalanche	DATE:	11/22/2022	CUST. P/N:		CUST. CONTACT:
	CHECK BY:	DATE:	CUSTOMER:		
APPROVE BY:	DATE:	11/22/2022	AVALANCHE		
	JOB#	QDS10624_AVL	SCALE: NONE	SIZE : B	REV 0.7
		DATE:	11/22/2022	SHEET: 2 OF 3	

Samtec Connector (240-pin,8x20)



Original Netname	New net name
PMC_MIO12_500	CLK1
PMC_MIO8_500	IO<0>
PMC_MIO10_500	IO<2>
PMC_MIO9_500	IO<1>
PMC_MIO7_500	CS1#
LS_PS_POR_B_PMC0	RESET#
PMC_MIO11_500	IO<3>
PMC_MIO0_500	CLK2
PMC_MIO4_500	IO<4>
PMC_MIO2_500	IO<6>
PMC_MIO1_500	IO<5>
PMC_MIO5_500	CS#2
LS_PS_POR_B_PMC0	RESET#
PMC_MIO3_500	IO<7>

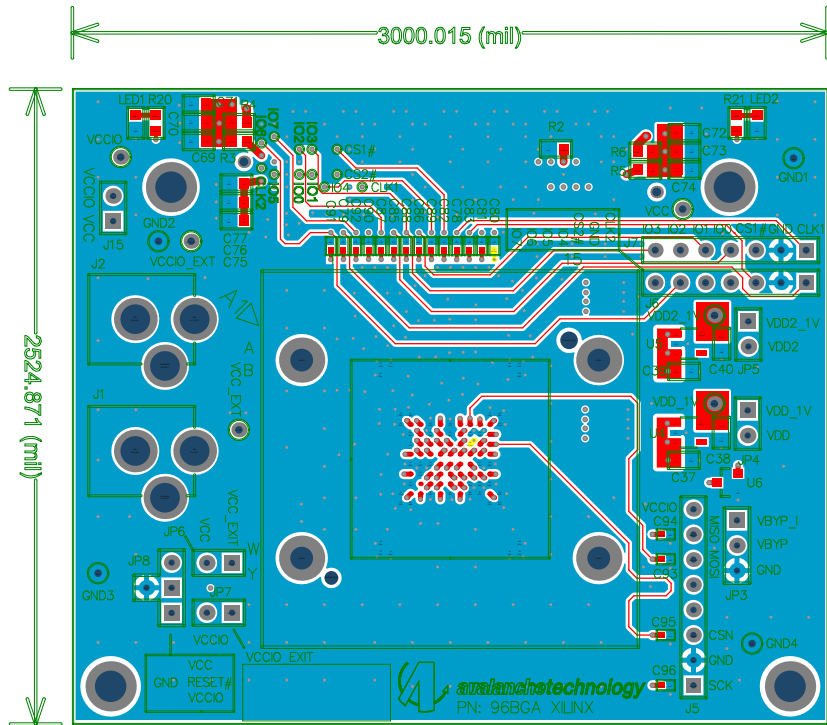
SEAM-30-02.0-L-08-1-A-K-TR



TITLE: 96BGA XILINX

DESIGNED BY: Avalanche	DATE: 11/22/2022	CUST. P/N:	CUST. CONTACT:
	CHECK BY:	DATE: 11/22/2022	CUSTOMER: AVALANCHE
JOB# QDS10624_AVL	APPROVE BY:	DATE: 11/22/2022	SCALE: NONE SIZE : B REV 0.7 SHEET: 3 OF 3

NOTE: FILE ARE FOR REFERENCE AND DOCUMENTATION ONLY NOT FOR REPRODUCE OR COPY.

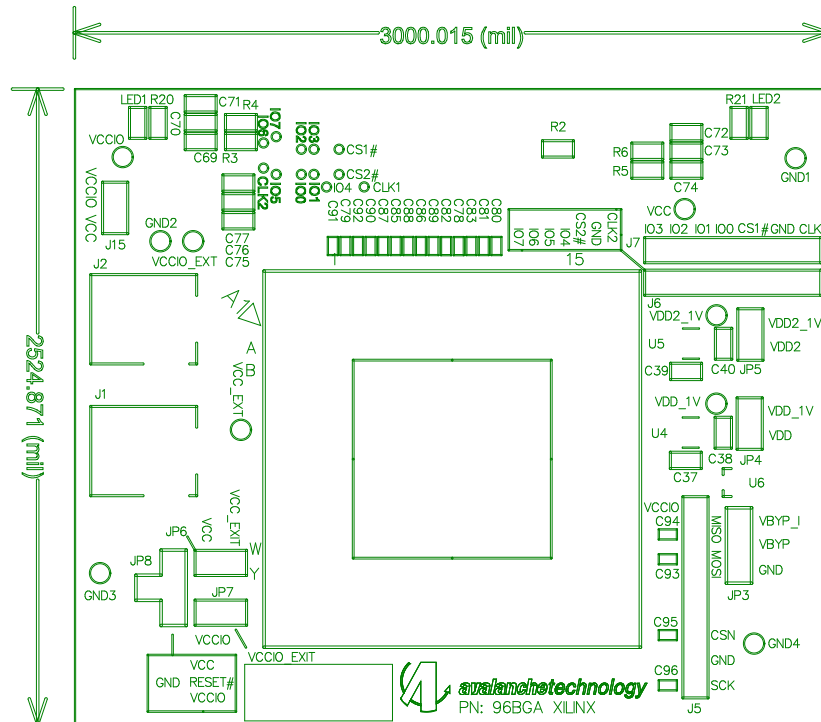


Title:	QDS10624_AVL_96BGA_XILINX_(V0.8)
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: DS10624_AVL_96BGA_XILINX_(V0.8)
ENG./Designer:	Avalanche
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED: 11/22/2022	
PADMASTER	DRILLMASTER
TOP	
TOP SILKSCREEN	

BOARD LAYER STRUCTURE:

LAYER 1	TOP
LAYER 2	GND1
LAYER 3	INTERNAL 1
LAYER 4	PWR1
LAYER 5	PWR2
LAYER 6	PWR3
LAYER 7	GND2
LAYER 8	BOTTOM

NOTE: FILE ARE FOR REFERENCE AND DOCUMENTATION ONLY NOT FOR REPRODUCE OR COPY.

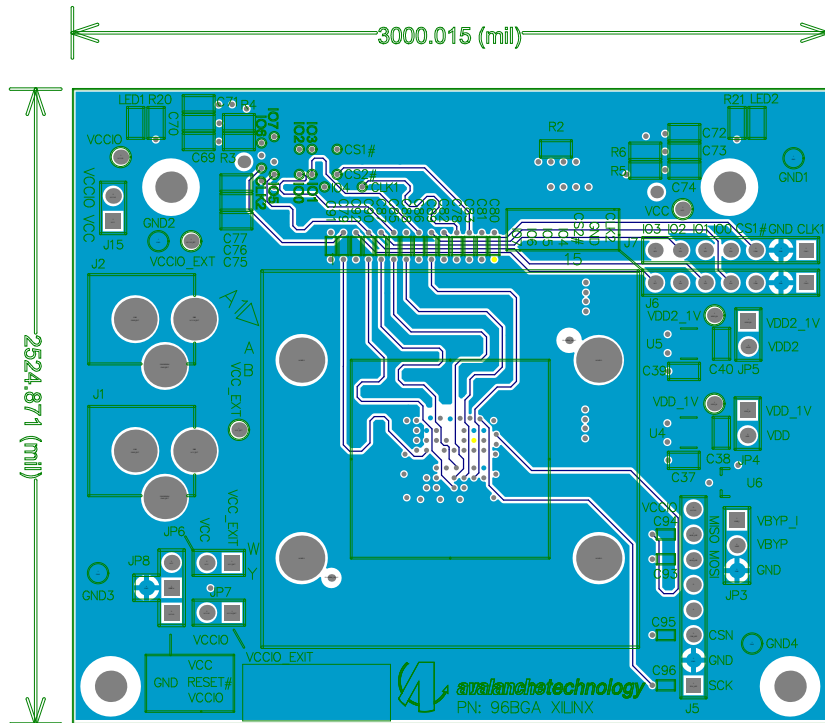


Title:	QDS10624_AVL_96BGA_XILINX_(V0.8)
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: DS10624_AVL_96BGA_XILINX_(V0.8)
ENG./Designer:	Avalanche
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED: 11/22/2022	
PADMASTER	DRILLMASTER
TOP SILKSCREEN	

BOARD LAYER STRUCTURE:

LAYER 1	TOP
LAYER 2	GND1
LAYER 3	INTERNAL 1
LAYER 4	PWR1
LAYER 5	PWR2
LAYER 6	PWR3
LAYER 7	GND2
LAYER 8	BOTTOM

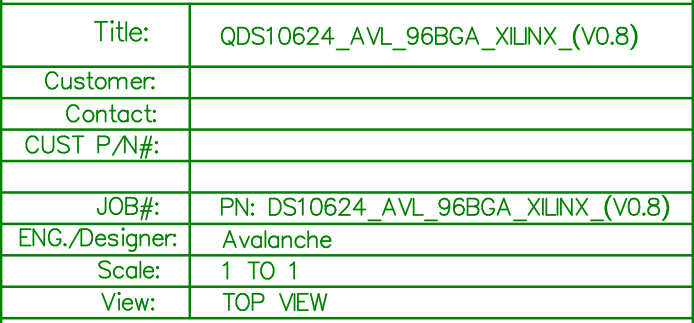
NOTE: FILE ARE FOR REFERENCE AND DOCUMENTATION ONLY NOT FOR REPRODUCE OR COPY.



Title:	QDS10624_AVL_96BGA_XILINX_(V0.8)
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: DS10624_AVL_96BGA_XILINX_(V0.8)
ENG./Designer:	Avalanche
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED: 11/22/2022	
PADMASTER	DRILLMASTER
INTERNAL1	
TOP SILKSCREEN	

BOARD LAYER STRUCTURE:

LAYER 1	TOP
LAYER 2	GND1
LAYER 3	INTERNAL 1
LAYER 4	PWR1
LAYER 5	PWR2
LAYER 6	PWR3
LAYER 7	GND2
LAYER 8	BOTTOM

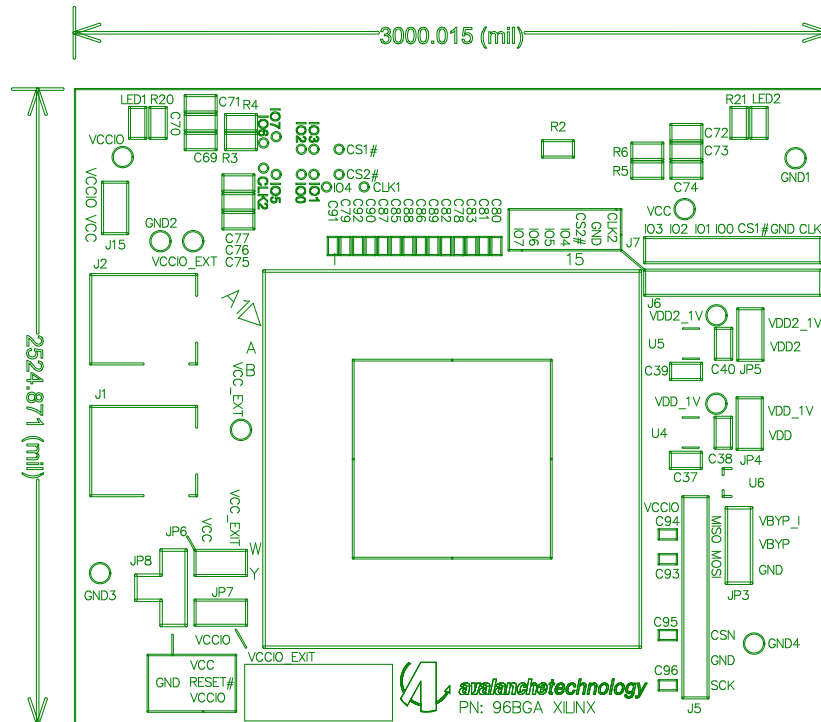


The first step in the process of identifying a problem is to recognize that there is a problem. This can be done by looking at the current situation and comparing it to what you want to achieve. Once you have identified the problem, the next step is to define the problem more clearly. This involves asking questions such as "What exactly is the problem?" and "Why is it a problem?" The third step is to generate potential solutions. This can be done by brainstorming ideas or researching existing solutions. The fourth step is to evaluate the potential solutions. This involves weighing the pros and cons of each solution and deciding which one is the best. Finally, the fifth step is to implement the chosen solution. This involves putting the solution into action and monitoring its progress.

BOARD LAYER STRUCTURE:

LAYER 1	_____	TOP
LAYER 2	_____	GND1
LAYER 3	_____	INTERNAL 1
LAYER 4	_____	PWR1
LAYER 5	_____	PWR2
LAYER 6	_____	PWR3
LAYER 7	_____	GND2
LAYER 8	_____	BOTTOM

NOTE: FILE ARE FOR REFERENCE AND DOCUMENTATION ONLY NOT FOR REPRODUCE OR COPY.



Title:	QDS10624_AVL_96BGA_XILINX_(V0.8)
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: DS10624_AVL_96BGA_XILINX_(V0.8)
ENG./Designer:	Avalanche
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED: 11/22/2022	
PADMASTER	DRILLMASTER
TOP SILKSCREEN	

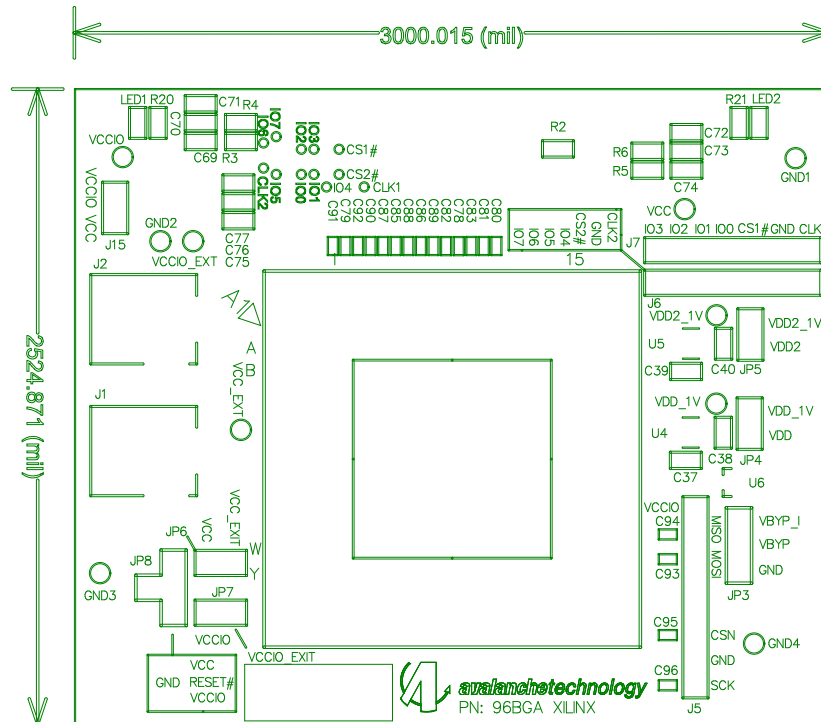
BOARD LAYER STRUCTURE:

LAYER 1	TOP
LAYER 2	GND1
LAYER 3	INTERNAL 1
LAYER 4	PWR1
LAYER 5	PWR2
LAYER 6	PWR3
LAYER 7	GND2
LAYER 8	BOTTOM

DATE PLOTTED:	11/22/2022
PADMASTER	DRILLMASTER
TOP SILKSCREEN	

LAYER 1	_____	TOP
LAYER 2	_____	GND1
LAYER 3	_____	INTERNAL 1
LAYER 4	_____	PWR1
LAYER 5	_____	PWR2
LAYER 6	_____	PWR3
LAYER 7	_____	GND2
LAYER 8	_____	BOTTOM

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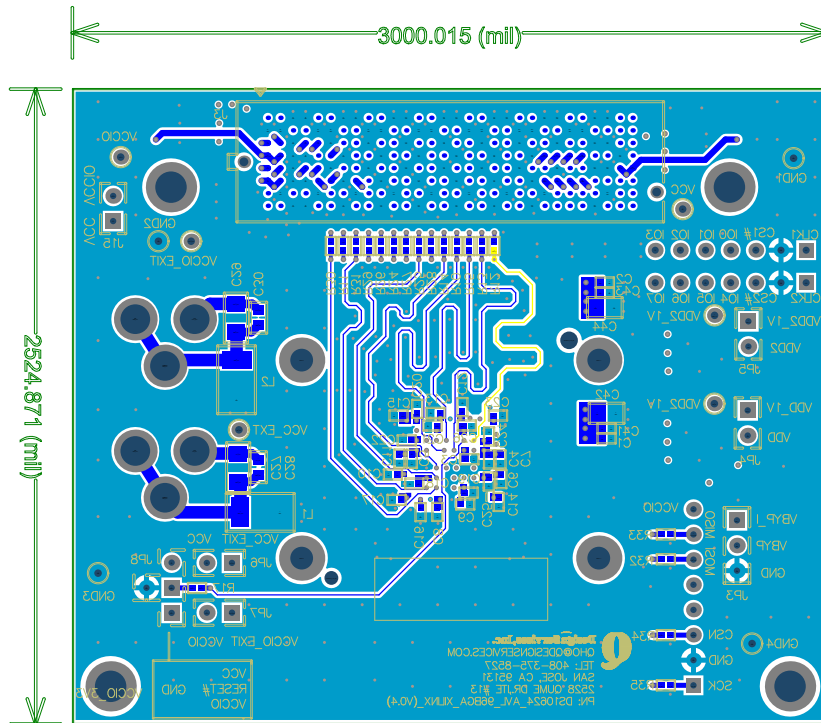


Title:	QDS10624_AVL_96BGA_XILINX_(V0.8)
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: DS10624_AVL_96BGA_XILINX_(V0.8)
ENG./Designer:	Avalanche
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED: 11/22/2022	
PADMASTER	DRILLMASTER
TOP SILKSCREEN	

BOARD LAYER STRUCTURE:

LAYER 1	TOP
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LAYER 3	INTERNAL 1
LAYER 4	PWR1
LAYER 5	PWR2
LAYER 6	PWR3
LAYER 7	GND2
LAYER 8	BOTTOM

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Title:	QDS10624_AVL_96BGA_XILINX_(V0.8)
Customer:	
Contact:	
CUST P/N#:	
JOB#:	PN: DS10624_AVL_96BGA_XILINX_(V0.8)
ENG./Designer:	Avalanche
Scale:	1 TO 1
View:	TOP VIEW
DATE PLOTTED: 11/22/2022	
PADMASTER	DRILLMASTER
	BOTTOM
	BOTTOM SILKSCREEN

BOARD LAYER STRUCTURE:

LAYER 1	TOP
LAYER 2	GND1
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