avalanchetechnology

The Silver Bullet: In Orbit Firmware Updates, Multiple Mission Images Now a Reality with a Single MRAM

Paul Chopelas, General Manager, Aerospace and Defense

SEE/MAPLD 2023

January 30, 2023

Avalanche Company Overview

Hi-Rel STT pMTJ MRAM since 2006

17 years STT MRAM Experience

Proprietary Selector

17 years STT MRAM Experience

Focused on Space and Hi-Rel Industrial

Hi-Rel Focused

Hi-Rel Industrial Heritage

Shipping volume to Industrial customers since 2019

Hi-Rel Focused

Domestic Technology

Domestic Technology

Granted

counting

Most Next-Gen/STT MRAM Patents Stateside

Growing Ecosystem

micross one source. one solution.

RENESAS BIG IDEAS FOR EVERY SPACE

falcon

XILINX

Protec GmbH

Lattice Semiconductor Corporation

RADIATION TEST SOLUTIONS

UMC

SONY

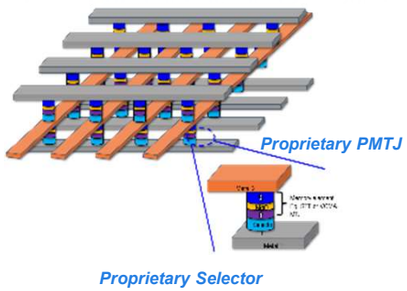
LA SEMICONDUCTOR

Growing Ecosystem

Growing Fab and Partner Ecosystem…

Avalanche Company Overview

Hi-Rel STT pMTJ MRAM since 2006



17 years STT MRAM Experience

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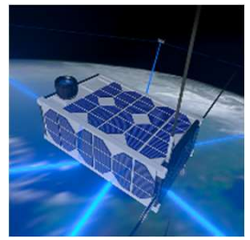

Hi-Rel Industrial Heritage

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Growing Fab and Partner Ecosystem…

The Avalanche's DARPA connection

Western Digital	**1996 - 2002**
GRANDIS	**2002 - 2008**
avalanchetechnology	**2008 - present**

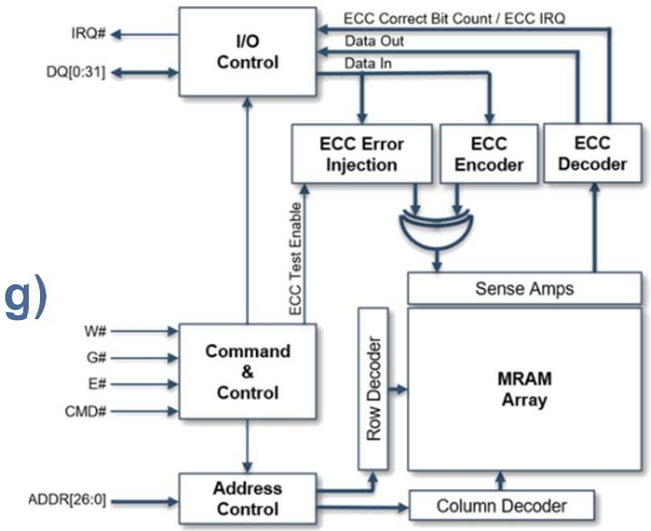
Dr. Yiming Huai – *CTO/VP of Technology*

- Yiming was a co-founder, board member, CTO and VP of Engineering of Grandis, Inc, a pioneer in Spin Transfer Torque MRAM (STT-MRAM). Founded in 2001.
- Huai successfully raised more than $30M in private and government funding to develop STT MRAM.
- Yiming has come full circle since the $14.7M in government funding from a DARPA program led by Dr. Dev Shenoy as Program Manager in 2008.
- Yiming came to Avalanche to achieve the goal of building a highly reliable dual use (industrial & space) MRAMs.

All Avalanche Executive are Semiconductor Industry Veterans – see more at:
(https://www.avalanche-technology.com/company/leadership/)

Best SWaP of any Hi-Rel Space NVMs

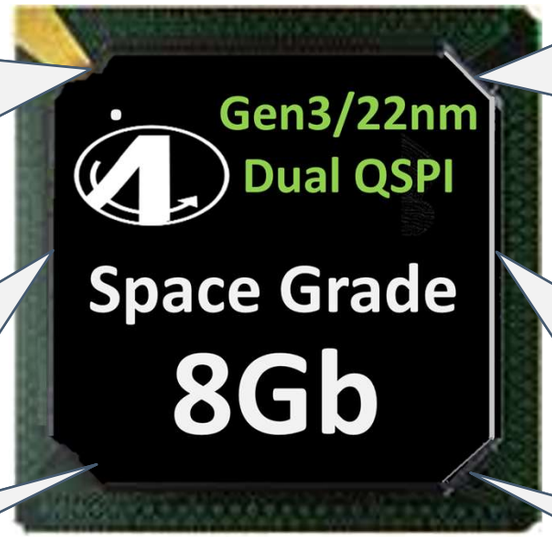
- **Innovations in cell, circuit & device architecture** over Toggle and early STT
- Designed for the **Highest Reliability:**
  - Robust **On-chip ECC with multibit correction**
  - **Error-free** non-destructive **read w/ unlimited endurance**
  - **Error-free writes** with **10^{16} endurance**
- **High Bandwidth Interface (711Mbps parallel/1.422Gbps streaming)**
- **Ultra Low Power**
- No Shielding Required vs legacy Toggle MRAM
- Supports unified memory architecture
  - **Architectural Simplification**



Avalanche MRAM Advantages in Space

Highest Endurance 10^{16} of any Space MRAM

Multiple I/F options
Parallel, Dual-QSPI, DDR, etc.



Lowest Power Consumption

RHBD Techniques
No Shielding Required

Highest bits/mm^2 of any Space MRAM

Flight Heritage

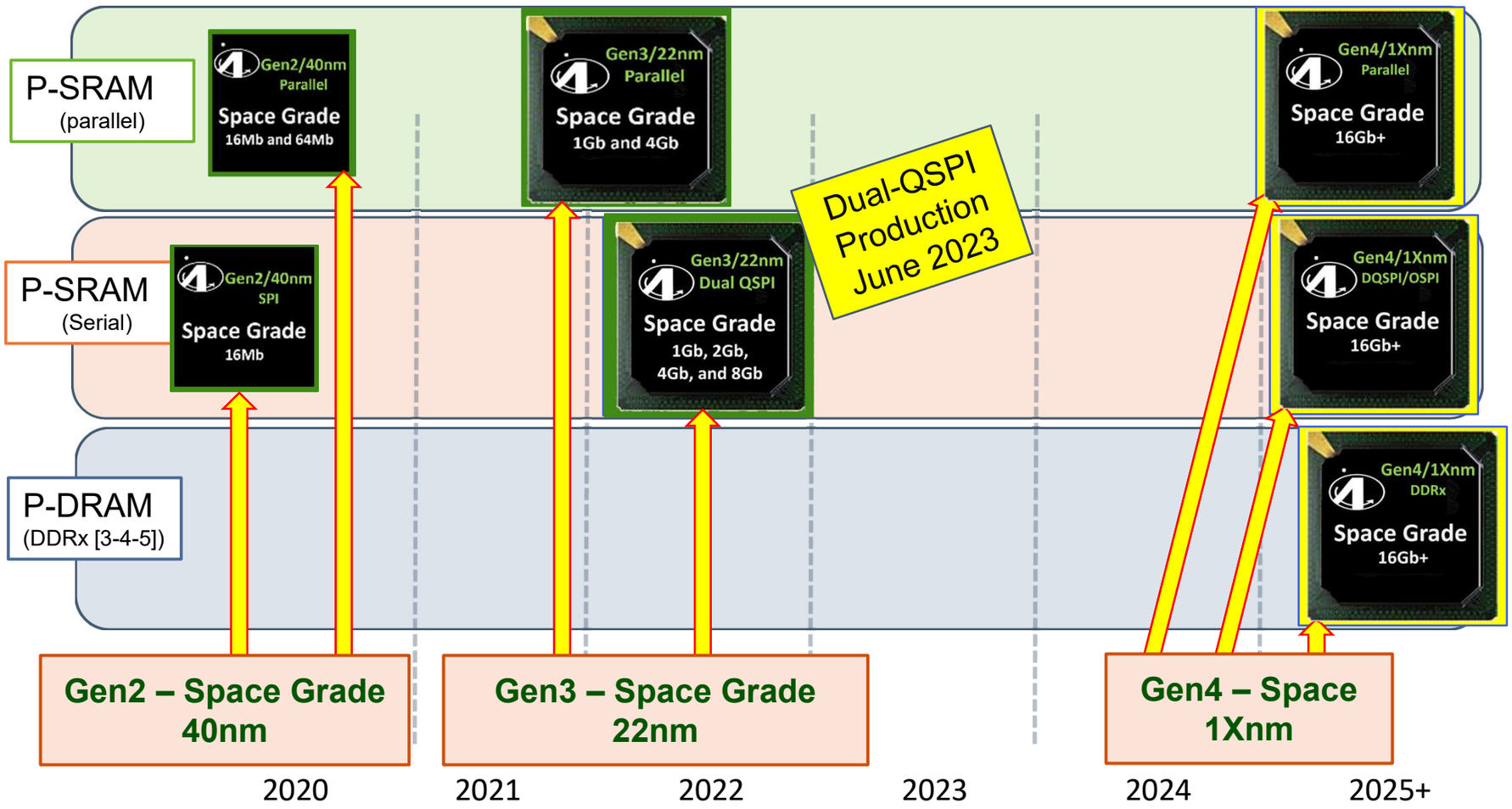
Gen 2 Achieved!

Gen 3 Soon

Inherently radiation tolerant memory array

[1] – Custom Interface

Avalanche Current and Future Roadmap



Preproduction
Production
Development
Planned

Gen3 SEE/TID Test Results & Planning

micross · APOGEE SEMICONDUCTOR · CAES PIONEERING ADVANCED ELECTRONICS · TEXAS A&M UNIVERSITY Cyclotron Institute

Device	Test Environment	Test Facility	Dates	Test Participants	Test Results
Test				Avalanche Technology	
P… Produ…					
Ma… Produ…					
	Flash X-ray	RTS	Summer ‘23	Micross	

Testing @ TAMU 4/20/23-4/21/23 Preview/Summary – 57 Runs over 16 Hours

Ion/LET	Ar/8.2	Cu/18.9	Kr/29.1	Ag/45.8	Xe/56.1	Ho/73.3

Fluence	1.00E+07	Flux	5.00E+04	1.00E+05

Test Modes	Standby	Read Loop	Write/Read Loop

Temp	25	60	120	Vcc	3.3V	Vcc-IO	3.3V	1.8V

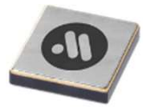
Summary Results	No Events, No Latchups, and No Errors from Ar/8.2 to Xe/56.1 At Ho/73.3 observed small current excursions at high temps

Complete report will be published by RTS in June ‘23

Earth to Mars – Avalanche MRAM covers spectrum

- Avalanche **MRAM technology & devices scalable** by radiation classification
- Avalanche productized **Space Grade as cost effective** COTS+ solution
- Enabling partners with **wafers & knowhow** to support extended flows

Mission Use Case	Company	Product Family	Qual Level & Screening	TID	SEE	Packaging Options	ITAR
Terrestrial	avalanchetechnology / RENESAS	Industrial Grade	JEDEC	<10KRad	<8MeV	Plastic - RoHS	No
Avionics, Missile, LEO	avalanchetechnology	Space Grade	JEDEC + 48hr burnin	<75KRad	~45MeV	Plastic - Leaded & RoHS	No
GEO	micross one source. one solution.	QED	PEMS, QML, & Custom	100KRad	~75MeV	Plastic - Leaded	Yes
GEO, Missile, Strategic	micross one source. one solution.	RadHard	QML, Custom	>300KRad	~75MeV	Plastic, Hermetic, Die, MCM	Yes



FIRMWARE OVER THE AIR (FOTA) UPDATES

Ingredients for FOTA

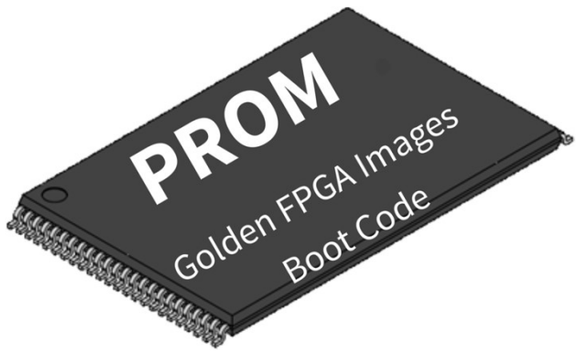
Support for Golden Images
- Reliable fallback mechanism for an “update anomaly”

Support for Large Densities
- Storing multiple FPGA images is only part of the FOTA story…
- …updating the RTOS (Linux) and the Applications are driving today’s density requirements
- …a customer is using a Versal AI Core w/ 64Gb (8 x 8Gb) for Full Linux PLUS regular AI/ML Model Updates

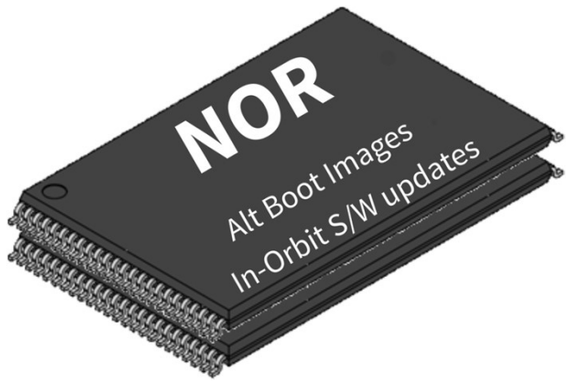
No Update Limit Count
- 10^{16} endurance means that you can write (continuously) to the same byte for ~15 years without wearing out
- Not a realistic scenario, but now you can consider our MRAMs as unlimited endurance – no “virtual” about it

Architectural Simplification with a Unified Memory model
- Multiple domains and regions makes flight system architectures simpler than terrestrial systems

Discrete Memory Domains – Legacy Implementations



ROM/PROM
No software overrides
Golden Image/Boot Loaders



Write Protected
Software override to Store
New Images up to size

[Optional] Volatile Execute Memory for Storing Transient Data

Unified Memory : Multiple Domains, Multiple Regions, Single Device

Today's Implementation:

Your Designs with Avalanche

VALIDATION AND DEMONSTRATION

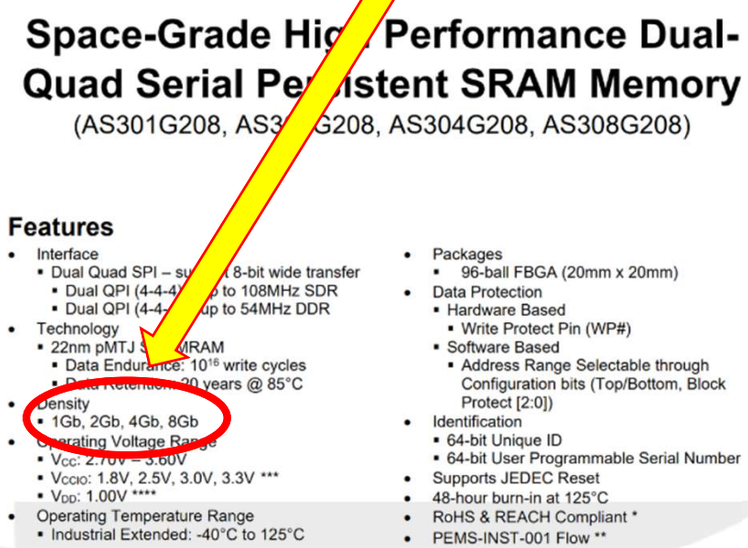
Versal ACAP Boot Memory Addressing Limits

From: Versal ACAP System Software Developers Guide (UG1304)

Table: Boot Mode Search Limit

Boot Mode	Search Offset Limit
OSPI (single, dual-stacked)	8 Gb
QSPI24 (dual-parallel)	256 Mb
QSPI24 (single, dual-stacked)	128 Mb
QSPI32 (dual-parallel)	8 Gb
QSPI32 (single, dual-stacked)	4 Gb
SD0 (3.0), SD1 (2.0), SD1 (3.0), or eMMC1	8191 FAT files (default)
eMMC1 (raw)	eMMC device size

Note: When using OSPI or QSPI dual-stacked mode, the BootROM ca…ly access the lower QSPI or OSPI addressable flash memory space for boot. After boot, the PLM can access the upper QSPI or OSPI… additional image storage.



Space-Grade Hig… Performance Dual-Quad Serial Pe…istent SRAM Memory

(AS301G208, AS3…G208, AS304G208, AS308G208)

Features

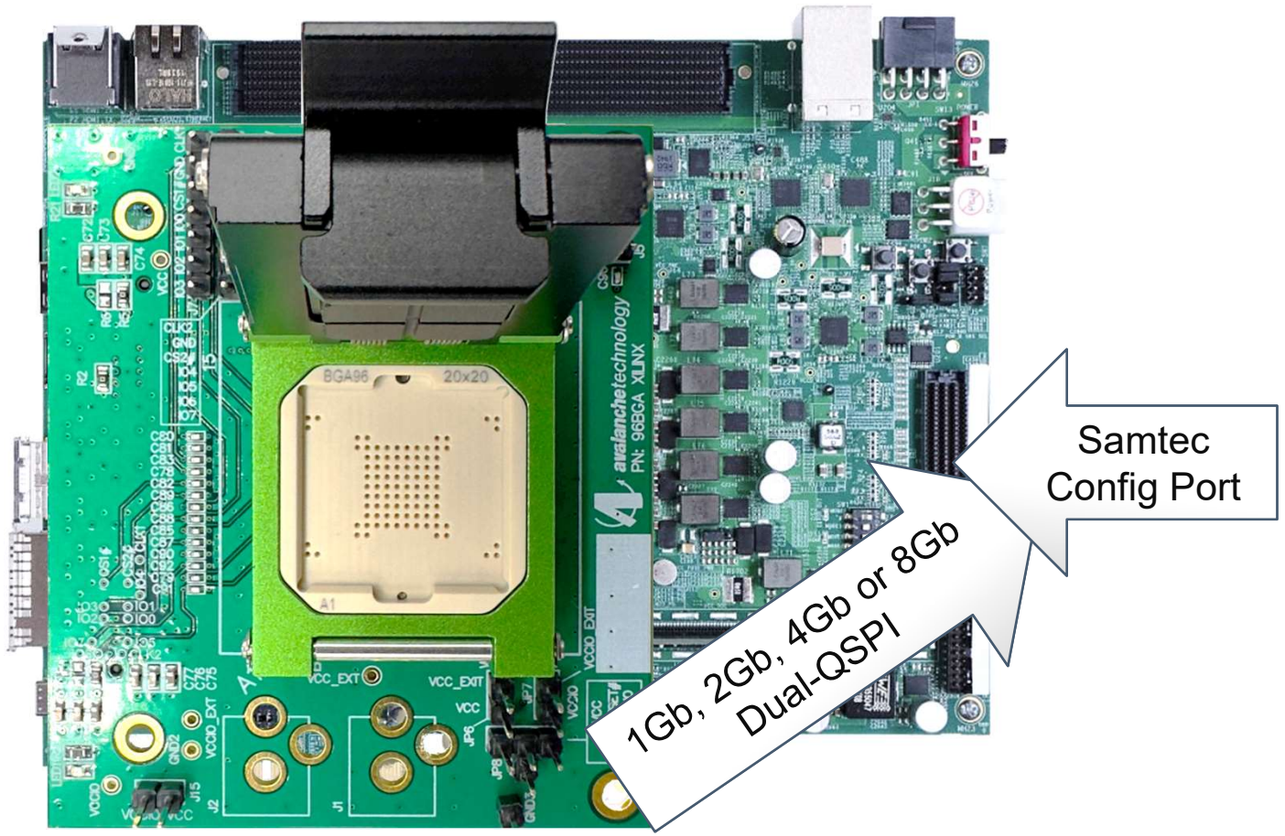
- Interface
  - Dual Quad SPI – su… 8-bit wide transfer
    - Dual QPI (4-4-4) …p to 108MHz SDR
    - Dual QPI (4-4-…up to 54MHz DDR
- Technology
  - 22nm pMTJ S…MRAM
    - Data Endurance: 10^{16} write cycles
    - Data Retention: …20 years @ 85°C
- Density
  - 1Gb, 2Gb, 4Gb, 8Gb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.0V, 3.3V ***
  - V_{DD}: 1.00V ****
- Operating Temperature Range
  - Industrial Extended: -40°C to 125°C
- Packages
  - 96-ball FBGA (20mm x 20mm)
- Data Protection
  - Hardware Based
    - Write Protect Pin (WP#)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Identification
  - 64-bit Unique ID
  - 64-bit User Programmable Serial Number
- Supports JEDEC Reset
- 48-hour burn-in at 125°C
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

Validating the Versal Boot on a VCK190

Device	Series	Total	Images in 8Gb
VP2802	Versal Premium	3.0 Gbits	2.7
...	...	...	...
VC1902	**Versal AI Core**	**884 Mbits**	**9.3**
...	...	...	...
VM2202	Versal Prime	432 Mbits	19
...	...	...	...
VE2002	Versal AI Edge	44 Mbits	187

Table shows 4 family members from a total of 39 family members

Source - Versal ACAP Technical Reference Manual (AM011)



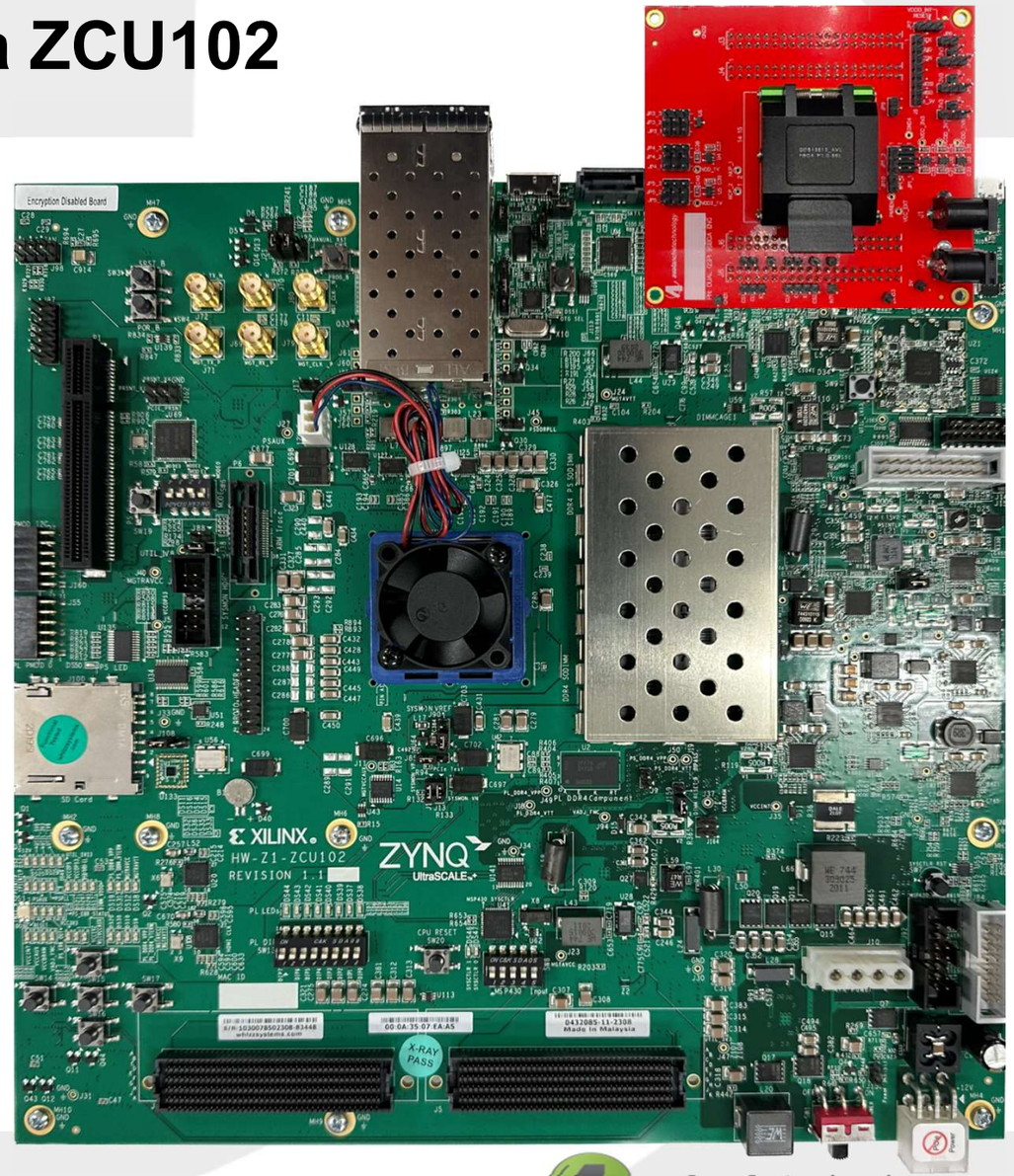
Validating the UltraScale+ Boot on a ZCU102

Zynq UltraScale+ MPSoCs

Device	Mbits/Image	Images/Gbit
ZU17	277.3	3.7
...	...	...
ZU6	**202.3**	**5.1**
...	...	...
ZU1	22.7	45.2

Table shows 3 family members 26

Source - Zynq UltraScale+ Device Technical Reference Manual (UG1085)

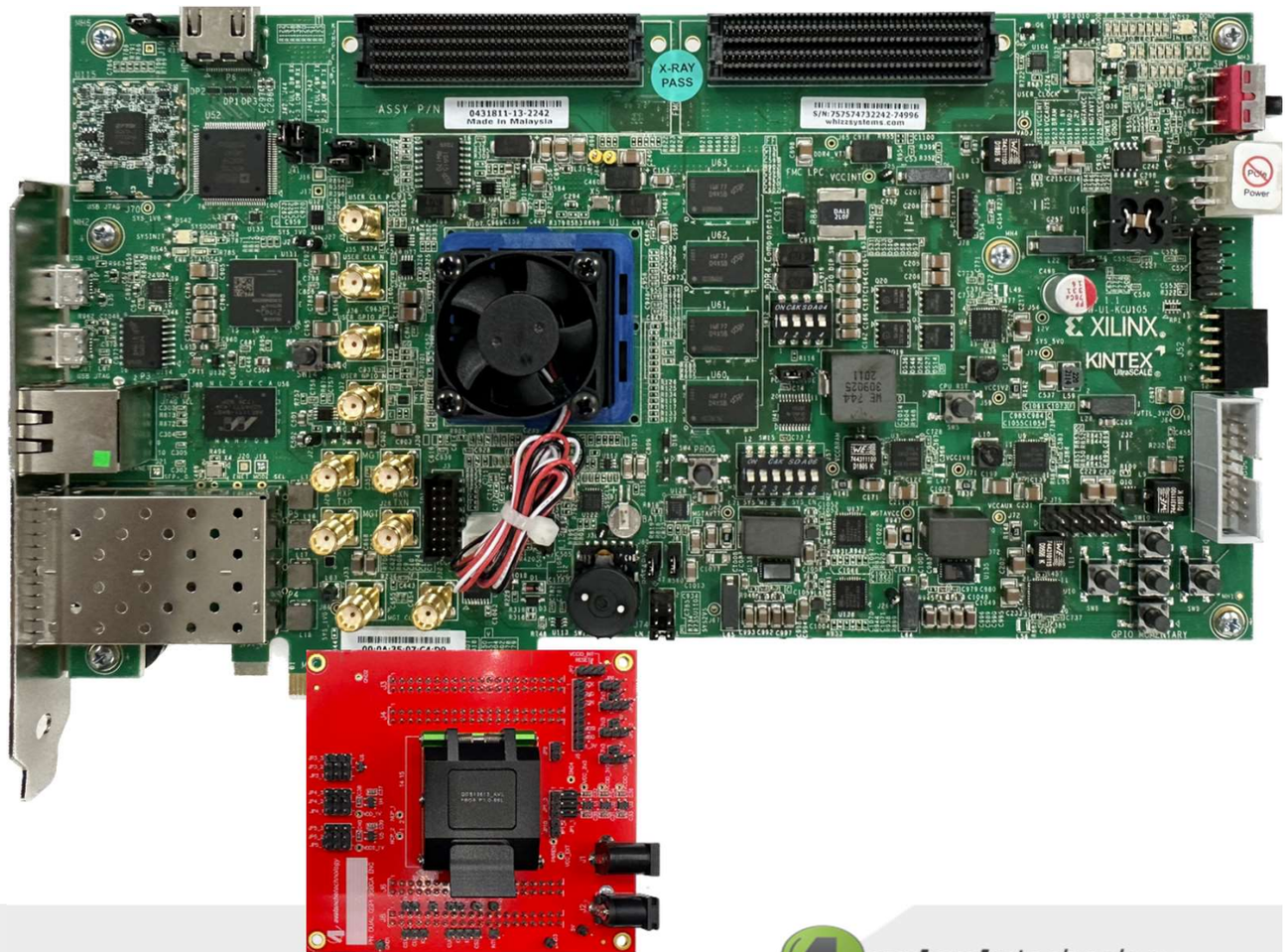


Validating the UltraScale Boot on a KCU105

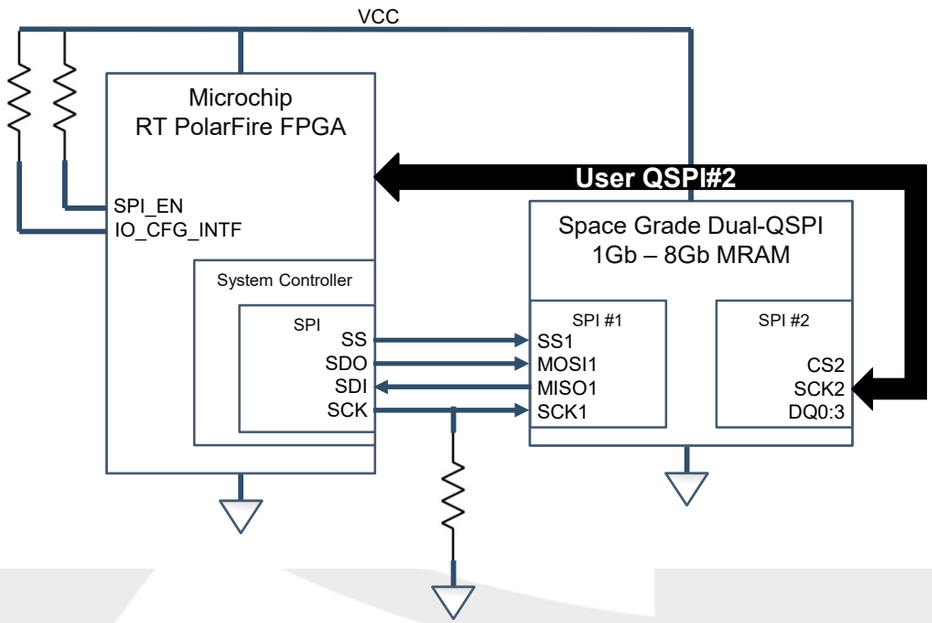
Kintex UltraScale FPGAs

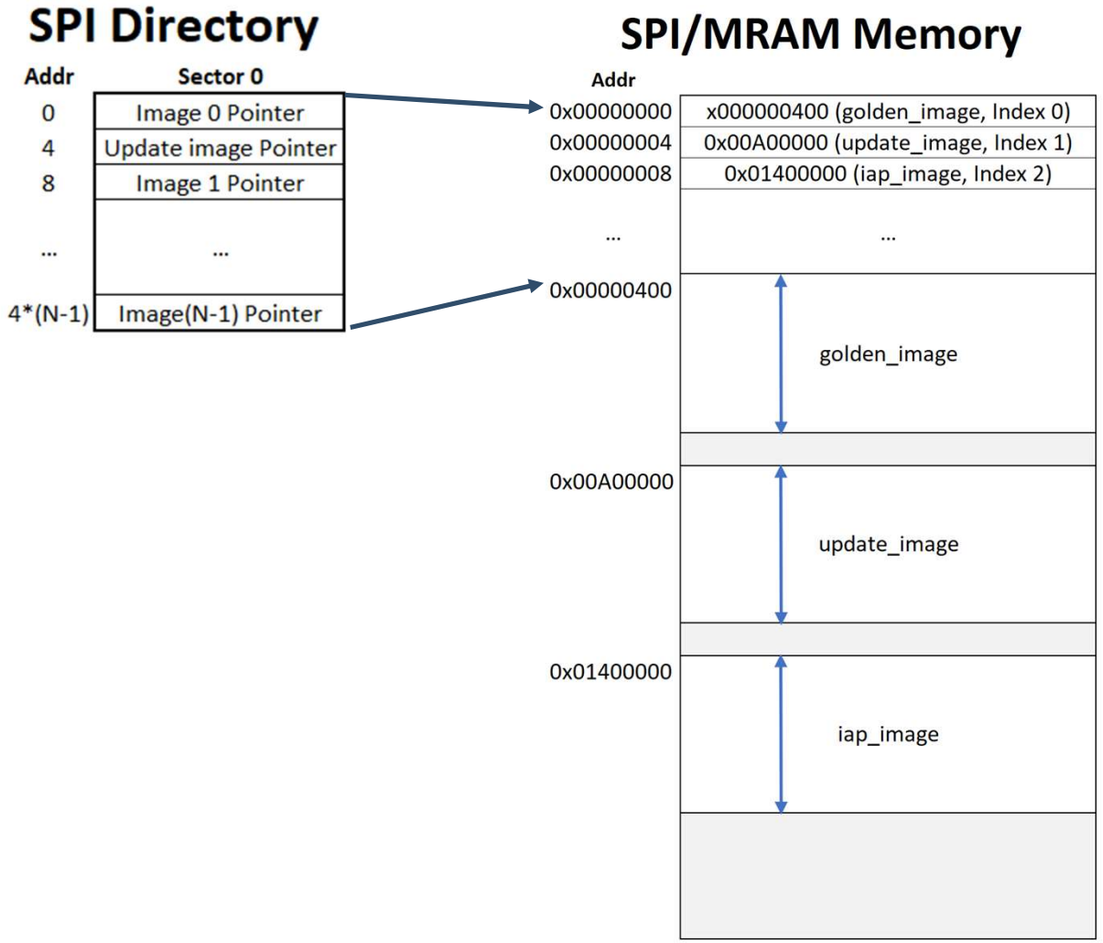
Device	Mbits/Image	Images/Gbit
KU085	368	2.8
...	...	...
KU060	**184**	**5.6**
...	...	...
KU040	122	8.4

Table shows 3 family members 7 UltraScale+ Kintex Members
Source - UltraScale Architecture Configuration - User Guide (UG570)



Updating Microchip's RT PolarFire on-board Flash with MRAM





Available to Order Today

Gen3 Parallel

1Gb & 4Gb
in Production

Parallel Dev Kit

For Space Grade w/ JEDEC flow, order from approved distributors:

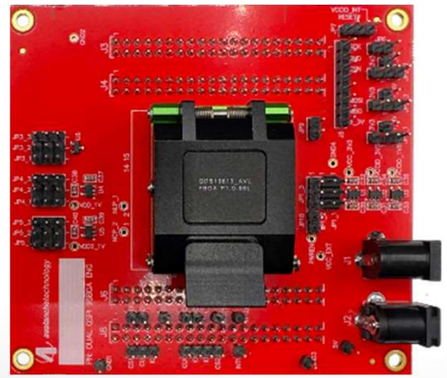
falcon electronics Protec GmbH Vertrieb elektronischer Bauteile

For PEMS, QML flows in plastic, hermetic, die/wafers, work with:

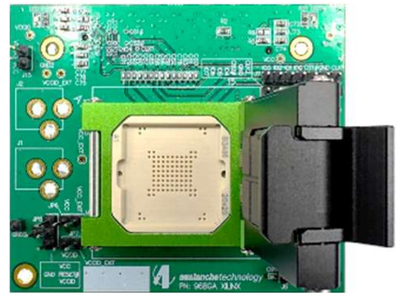
micross one source. one solution.

Gen3 Serial

1Gb, 2Gb, 4Gb, & 8Gb
in Production June-'23



Dual-QSPI Dev Kit



Versal Boot Module

Summary…

Best SWaP

- **Highest Density** (up to 8Gb)
- **Lowest Power**
- No Shielding Required
- COTS+ screening flows

Unified Memory

- Low latency, I/F like SRAM
- **Boot large images + RTOS + working mem**
- Flexible, robust write protection
- **Architectural simplification**

Hi-Rel by Design

- **ECC w/ Multibit Correction**
- **Highest Endurance**
- Inherently RadHard Cell
- RHBD for CMOS Protection

micross one source. one solution.®

On-Shore / QML

- Domain Experts in RadHard & Testing
- **40+ years in PEMS & QML quals**
- US Wafer Banks for Supply Assurance
- Avalanche will use Micross Packaging

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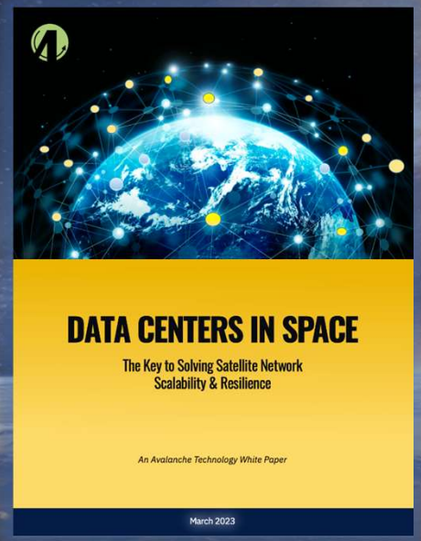
Thank You!

avalanchetechnology

Paul Chopelas, General Manager, Aerospace and Defense
paul@avalanche-technology.com

Check out our Whitepapers and Blogs



Firmware Over-The-Air Updates and Multiple Mission Images Now a Reality for AMD Adaptive SoCs Used in Space

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