



# Serial Dual QSPI P-SRAM™ for Lattice LCMXO3XX-6900C FPGA Evaluation Kit User Guide AK3XXG208LATCCSOC

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**Table 1: Revision History**

<b>Revision No.</b>	<b>Date</b>	<b>History</b>
1.0	12/19/2022	Initial Release

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## 1. Overview

The Avalanche Serial Dual QSPI P-SRAM™ for Lattice LCMXO3L/LF-6900C FPGA evaluation kit enables the users to evaluate Avalanche Serial Dual QSPI P-SRAM™ product using a Lattice LCMXO3L/LF-6900C FPGA evaluation kit connected to Avalanche daughterboard via Avalanche proprietary FPGA based Asynchronous SRAM interface. The Serial Dual QSPI P-SRAM™ for Lattice LCMXO3L/LF-6900C FPGA evaluation kit communicates with the computer and is powered by the host computer's USB interface using a micro-USB cables type B connector.

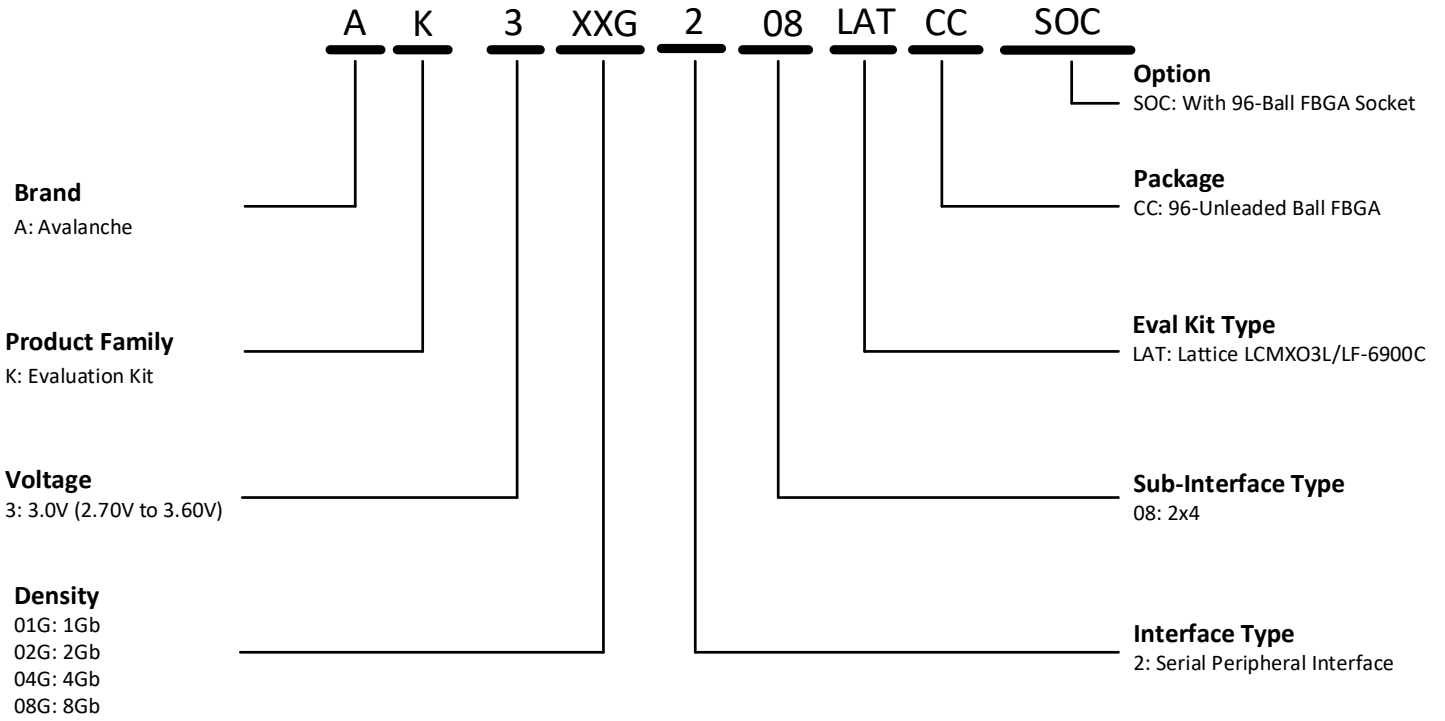
## 2. Avalanche P-SRAM™ Product Support & Evaluation Kit Ordering Options

The Avalanche P-SRAM™ daughterboard with a socket can be populated with one of the following Serial Dual QSPI P-SRAM™ devices:

**Table 2: Avalanche Serial Dual QSPI P-SRAM™ Product Support & Evaluation Kit Ordering Options**

Part #	Density	Voltage	Organization	Package	Evaluation Kit Ordering Options
AS301G208-0108X0MCC	1Gb	2.7 V to 3.6V	Dual QSPI	96-Pin FBGA	AK301G208LATCCSOC
AS302G208-0108X0MCC	2Gb	2.7 V to 3.6V	Dual QSPI	96-Pin FBGA	AK302G208LATCCSOC
AS304G208-0108X0MCC	4Gb	2.7 V to 3.6V	Dual QSPI	96-Pin FBGA	AK304G208LATCCSOC
AS308G208-0108X0MCC	8Gb	2.7 V to 3.6V	Dual QSPI	96-Pin FBGA	AK308G208LATCCSOC

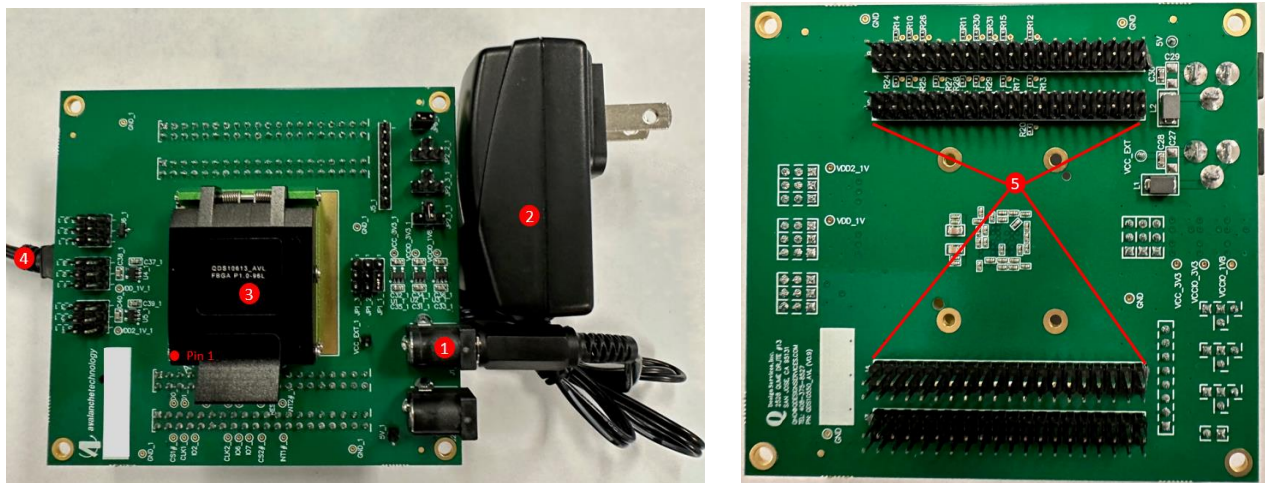
### 3. Evaluation Kit Ordering Options



**Figure 1: Evaluation Kit Ordering Information**

## 4. Evaluation Kit Package Contents

1. An Avalanche daughter board (3.5 x 3.5 inches) with a 96-FBGA socket
2. A Lattice LCMXO3L/LF-6900C FPGA board
3. A micro-USB cable type B
4. A 3.3V 1.8A AC/DC power supply cord

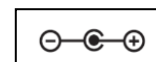


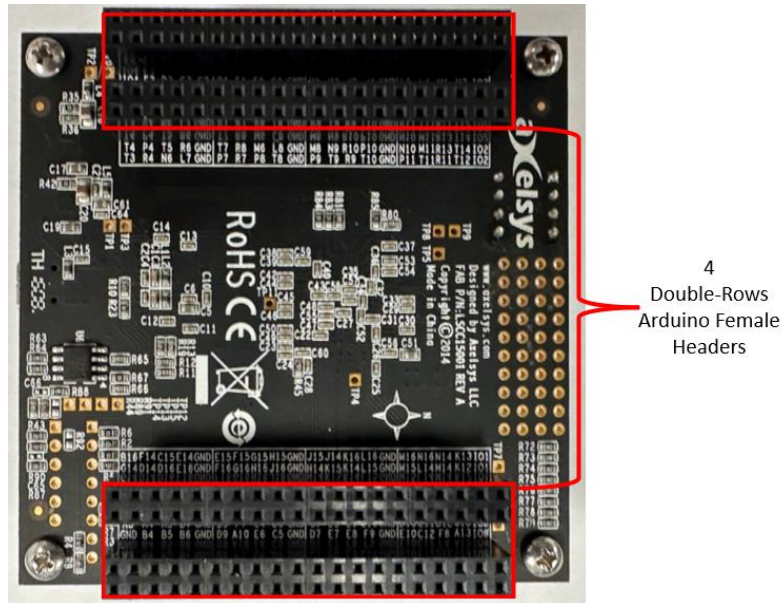
**Figure 2: Serial Dual QSPI P-SRAM™ Daughter Board with a 96-FBGA Socket (Front & Back)**

**Table 3: Evaluation Kit Setup Description**

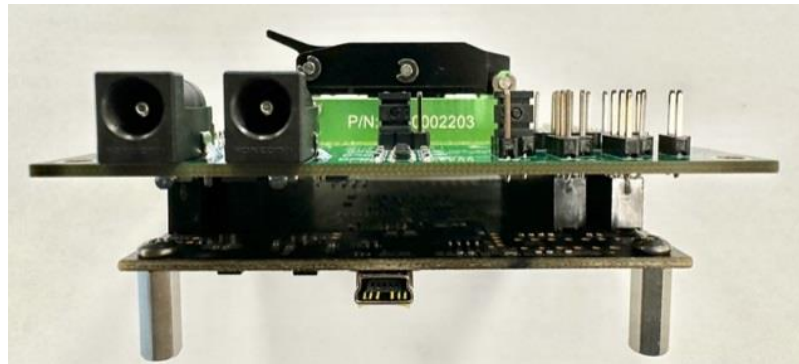
Callout Number	Description
1	Power Barrel Connector Jack*
2	3.3V 1.8A AC/DC power supply cord
3	Avalanche 96-Ball FBGA socket
4	USB type Mini-B cable connecting from Lattice LCMXO3L/LF-6900C FPGA board to PC host
5	4 double-row Arduino male headers connecting to Lattice LCMXO3L/LF-6900C FPGA board

Note: \*Plug polarity on the Power Barrel Connector Jack: P = Center Positive





**Figure 3: Lattice LCMXO3L/LF-6900C FPGA board (back side) with 4 Double-Rows Arduino Female Headers**



**Figure 4: Serial Dual QSPI P-SRAM™ Daughter Board Attaching to Lattice Board**

*Note: a Lattice LCMXO3L/LF board requires to have 4 double-rows of Arduino female headers installed to connect it to the Avalanche daughter board.*

## 5. Getting Started

The following steps are necessary to operate the kit.

### 5.1 Requirements

- A PC system with one available USB 2.0/3.0 port
- Windows 10 with 32/64-bit Operation System
- FTDI USB Window drivers

- Avalanche application software
- Avalanche Serial Dual QSPI P-SRAM™ for Lattice LCMXO3L/LF-6900C FPGA evaluation kit

## 5.2 FTDI USB Drivers Installations

Communication between the Lattice LCMXO3 board and a PC via the USB connection cable requires installation of the FTDI USB hardware drivers. Loading these drivers enables the PC to recognize the Lattice board. Click [here](#) to download the drivers.

*Note: first install the FTDI drivers and then connect the Lattice LCMXO3 board to the PC*

## 5.3 Avalanche Application Software

Click [here](#) to download the software package in zip format. The zip file contains two files: “Dual\_QSPI\_test.exe” and “Config.txt”.

## 5.4 Connecting the Evaluation Kit to the PC

Perform the step-by-step instructions in the following order to configure and connect the evaluation kit to the PC:

### Power Sequence – Connect Power

1. Connect the provided 3.3V 1.8A power supply cord to power outlet
2. Turn on Avalanche daughter board by connecting the 3.3V power connector to daughter board’s connector jack
3. Turn on the Lattice board by connecting the Lattice LCMXO3 to the PC using the USB Mini-B cable. The PURPLE power LEDs on the Lattice board should stay on after connection.

*Note: the Avalanche daughter board requires dual-power supply sources: power from the 3.3V 1.8A supply cord and power from the Lattice LCMXO3’s USB Mini-B cable. To ensure the Avalanche Serial Dual QSPI P-SRAM device to be powered up correctly, user must follow a correct order of step 1, 2 and 3.*

### Power Sequence – Disconnect Power

1. Turn off Avalanche daughter board by disconnecting the 3.3V power connector to daughter board’s connector jack
2. Turn off the Lattice board by disconnecting the USB Mini-B connector from the Lattice board’s USB Mini-B socket.

*Note: the Avalanche daughter board requires dual-power supply sources: power from the 3.3V 1.8A supply cord and power from the Lattice LCMXO3’s USB cable. To ensure the Avalanche Serial Dual QSPI P-SRAM device to be powered down correctly, user must follow a correct order of step 1 and 2.*



## 5.5 Running Avalanche Test Program

The Lattice LCMXO3 board is pre-loaded with proprietary Avalanche FPGA bitfile and an executable test program. The Avalanche test software consists of two files:

1. Config.txt
2. Dual\_QSPI\_Test.exe

To run the Avalanche test software, double click on “Dual\_QSPI\_Test.exe”

The configuration file consists of six user-defined lines. Below is an example of a config.txt file:

- Def\_port = 1
  - Use “1” as the default COM port.
- Run\_test = y/n
  - y: automated test. The test starts automatically once the “Dual\_QSPI\_Test.exe” is invoked.
  - n: user selected option test. The user can start the test manually.
- Start\_Address = 0
- Num\_Bytes = 32
- Def\_Pattern = 7
  - 7 = Incrementing Data Pattern

```
Avalanche Technology Dual-QSPI 3V Test Program V3.4.2_EXT

Connecting to default port mentioned in config.txt ...
Device Connected

Avalanche Technology Dual-QSPI 3V Test Program V3.4.2_EXT

Test Menu
a. Write Sequential
b. Read Sequential
c. Read Compare Sequential
d. Write Read Compare Sequential
e. Write any Register
f. Read any Register
g. Read ID
h. Read Status
i. Select Dual QSPI lane
x. Exit

Selection ?
```

**Figure 5: Test Menu**

- Functional Test Selection
  - a: Write Sequential
  - b: Read Sequential
  - c: Read-Compare Sequential
  - d: Write-Read-Compare Sequential
  - e: Write Any Register
  - f: Read Any Register
  - g: Read Device ID
  - h: Read Status Register
  - i: Select Dual QSPI Lane
  - x: Exit

```

Device Connected

Avalanche Technology Dual-QSPI 3V Test Program V3.4.2_EXT

Test Menu
a. Write Sequential
b. Read Sequential
c. Read Compare Sequential
d. Write Read Compare Sequential
e. Write any Register
f. Read any Register
g. Read ID
h. Read Status
i. Select Dual QSPI lane
x. Exit

Selection ? i

Enter lane to test (Default 0):

Avalanche Technology Dual-QSPI 3V Test Program V3.4.2_EXT

Test Menu
a. Write Sequential
b. Read Sequential
c. Read Compare Sequential
d. Write Read Compare Sequential
e. Write any Register
f. Read any Register
g. Read ID
h. Read Status
i. Select Dual QSPI lane
x. Exit

Selection ? d

Enter Starting Address (Default 0):
Enter Number of bytes (Default 32):
Data Pattern type??:
  1) All Zeros                10) All 0xAA
  2) All Ones                 11) All 0x55
  3) 0xAA, 0x55              12) 0x55, 0xAA
  4) 0xFF, 0x00              13) 0x00, 0xFF
  5) Shifting One Left       14) Shifting One Right
  6) Shifting Zero Left     15) Shifting Zero Right
  7) Incrementing Sequence   16) 0x0F, 0xF0
  8) Decrementing Sequence   17) 0xF0, 0x0F
  9) Random

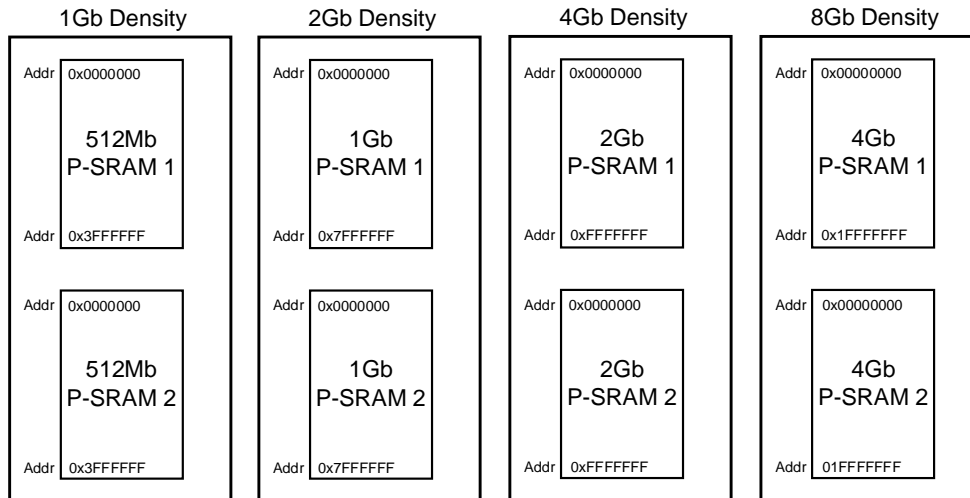
(Default 7):
Mode??:
  0) Single Mode
  1) QUAD Mode
(Default 0):
SDR/DDR??:
  0) SDR
  1) DDR
(Default 0):
Write IO Mode??:
  0) 1-1-1
  1) 1-4-4
(Default 0):
Write/Fast Write??:
  0) Write (0x2)
  1) Fast Write
(Default 0):
Read IO Mode??:
  0) 1-1-1
  1) 1-1-4
  2) 1-4-4
(Default 0):
Read/Fast Read??:
  0) Read (0x3)
  1) Read (0x13)
  2) Fast Read (0x0b)
(Default 0):
Operation      : SDR Write (0x2) 111
Operation      : SDR Read 111
Starting Address : 0x00000000
Total Size      : 0x00000020
Tx Size         : 0x00000020
Pattern         : Incrementing Sequence

Write Read Compare Done Error 0
  
```

**Figure 6: Write Read Compare Sequential Test Example**

## Write Read CompareTest Example – Option d

**Step 1** – select option i: lane 0 is selected



**Figure 7: Address Range per Lane**

An Avalanche Serial Dual QSPI P-SRAM connects two Quad SPI devices (P-SRAM 1 & P-SRAM2) as indicated in Figure 4. Each device has a separate memory address range and can be tested independently. Lane 0 is referenced to P-SRAM 1 and Lane 1 is referenced to P-SRAM 2.

**Step 2** – select option d: Write Read Compare Sequential is selected

**Step 3** – Enter Starting Address: address 0 is selected. User can choose any address location within the maximum memory space per lane

**Step 4** – Enter Number of Bytes tested: 32-Byte is selected

- For 1Gb: maximum number of bytes (in hex value) = 0x4000000 per lane
- For 2Gb: maximum number of bytes (in hex value) = 0x8000000 per lane
- For 4Gb: maximum number of bytes (in hex value) = 0x10000000 per lane
- For 8Gb: maximum number of bytes (in hex value) = 0x20000000 per lane

**Step 5** – Select Data Pattern Type: Incrementing Sequence Data Pattern is selected

**Step 6** – Select Transfer Mode: 0 (SPI 1-1-1) mode is selected

**Step 7** – Select SDR or DDR mode: 0 (SDR) mode is selected

**Step 8** – Select Write Operation Mode: 0 (SPI 1-1-1) mode is selected

**Step 9** – Select Write Command Opcode: 0 - Command Opcode 0x02 is selected

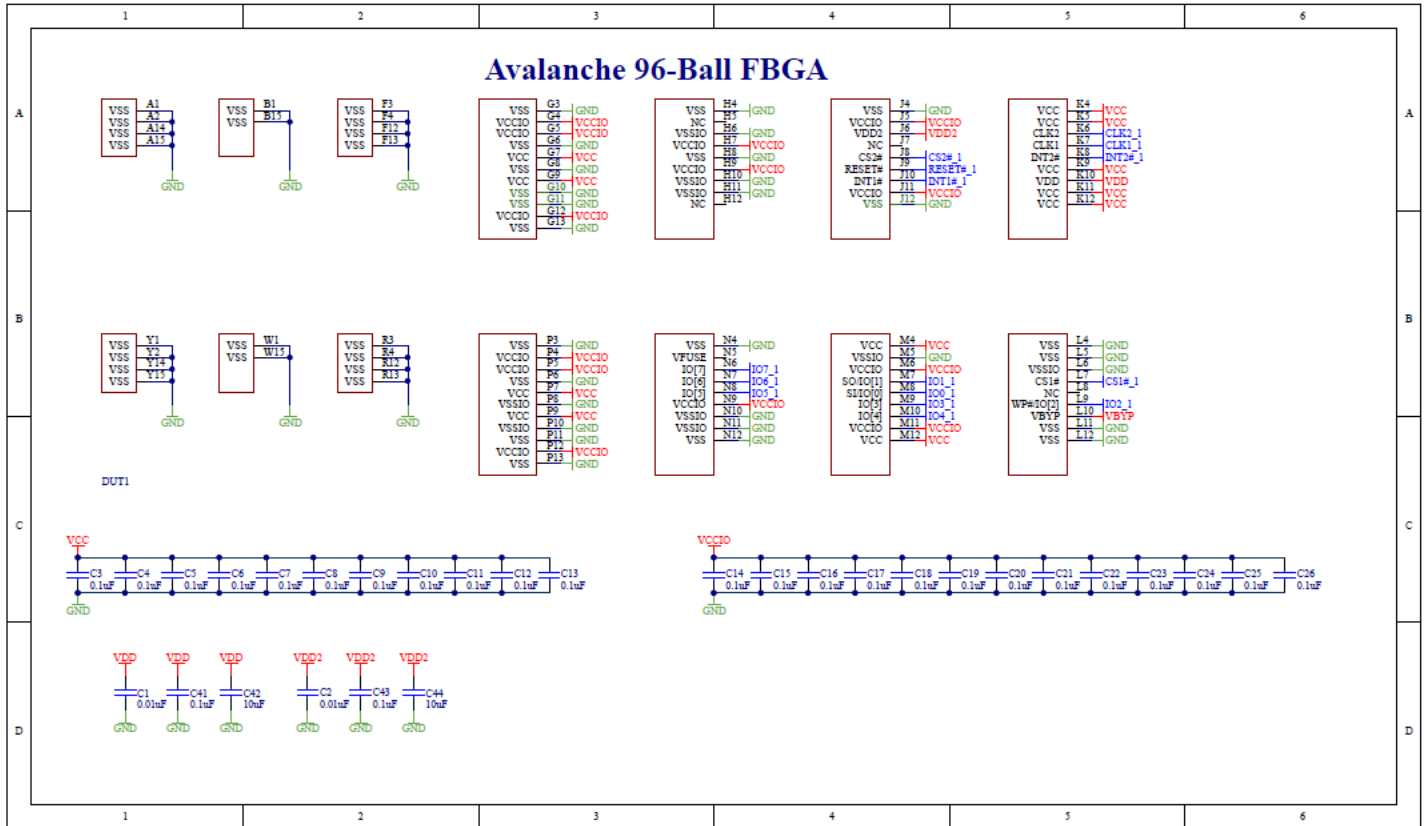
**Step 10** – Select Read Operation Mode: 0 (SPI 1-1-1) mode is selected

**Step 9** – Select Read Command Opcode: 0 - Command Opcode 0x03 is selected

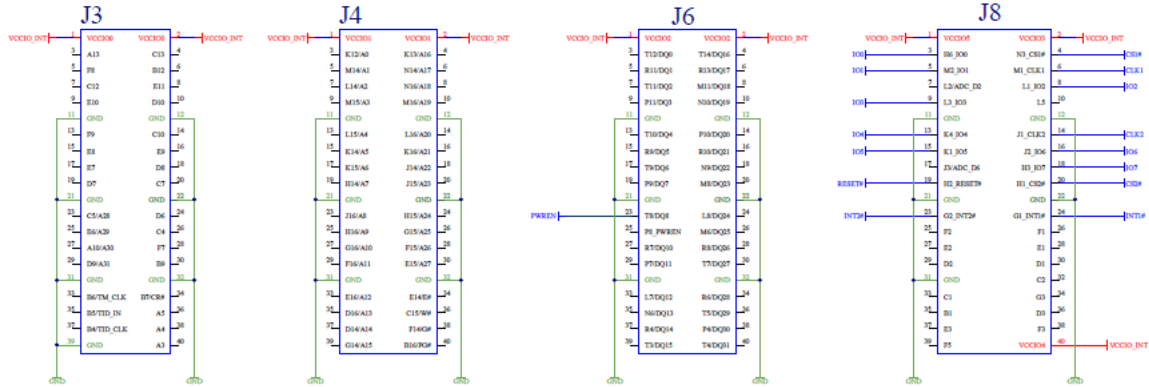
The Write Read Compare test gets executed and test result shows 0 error.

## 6. Schematics

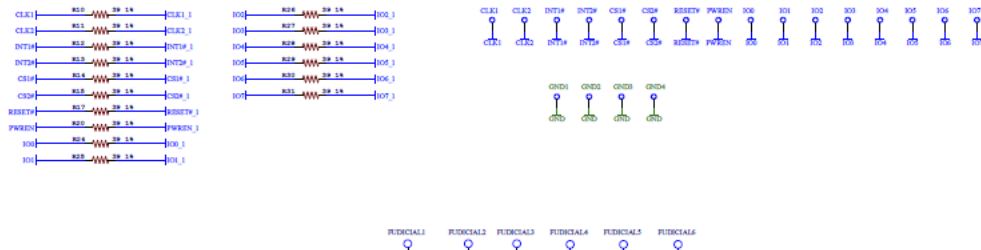
### AK3XXG208LATCCSOC – Schematic

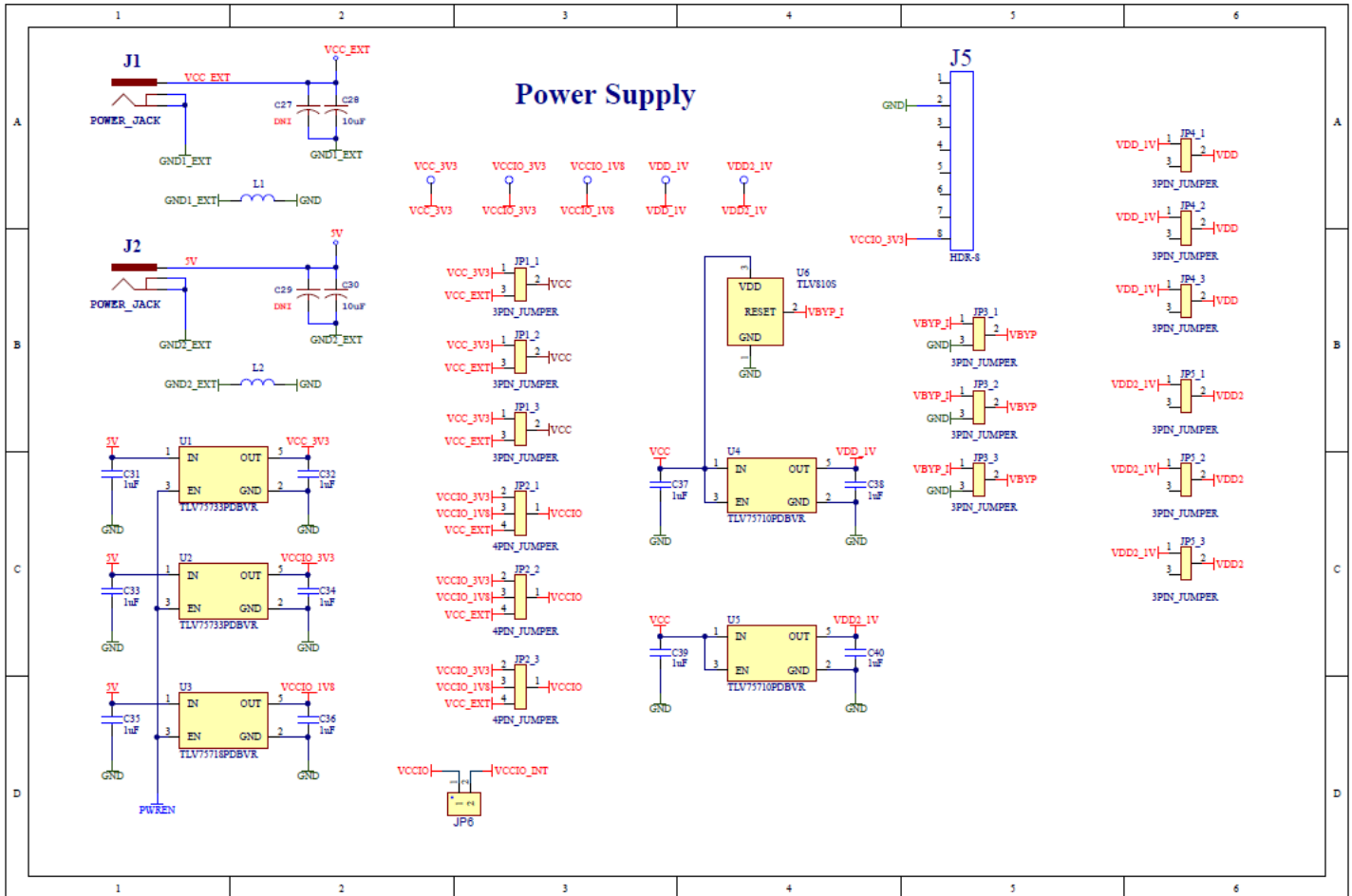


**96-Ball FBGA Connection to Lattice MACHX03 Development Kit.**



**Source Termination 39 Ohms**







## 7. BOM

### AK3XXG208LATCCSOC – BOM

Qty	Value	Part
7	TP	+5V0, IOREF, RSTB, VCAP, VCC, VIN, VOUT
1		BR1
5	10nF	C2, C11, C13, C23, C25
2	4.7uF	C12, C14
4	NL	C19, C20, C21, C22
2	1uF	C24, C26
1	2X10_ML	CN7
1	2X8_ML	CN8
1	2X15ML	CN9
1	2X17ML	CN10
2	HDR2X35	CN11, CN12
1	CY14B101LA/NA_54PIN_TSOPX16	IC4
1	CY14B101LA/NA_54PIN_TSOPX16	IC5
2	3PIN_JUMPER	JP3, JP4
1	3.3V ENABLE	JP12
2	BLM18SG121TN1D	L1, L2
1	RED	LED2
43	39 1%	R1, R4, R7, R18, R21, R24, R27, R30, R33, R36, R39, R42, R45, R48, R51, R54, R57, R60, R63, R66, R69, R72, R75, R78, R81, R84, R87, R90, R93, R96, R99, R102, R105, R108, R111, R114, R117, R120, R123, R126, R129, R132, R135
80	DNI	R2, R3, R5, R6, R8, R9, R11, R19, R20, R22, R23, R25, R26, R28, R29, R31, R32, R34, R35, R37, R38, R40, R41, R43, R44, R46, R47, R49, R50, R52, R53, R55, R56, R58, R59, R61, R62, R64, R65, R67, R68, R70, R71, R73, R74, R76, R77, R79, R80, R82, R83, R85, R86, R88, R89, R91, R92, R94, R95, R97, R98, R100, R101, R103, R104, R106, R107, R109, R110, R112, R113, R115, R116, R118, R119, R122, R125, R128, R131, R134
6	120	R10, R121, R124, R127, R130, R133
1	2K	R12
2	0	R13, R16
1	105K, 1%	R14
1	30.9K, 1%	R15

Qty	Value	Part
1	28.7K, 1%	R17
1	MCP1825T-ADJE/DC	U3
43	39 1%	R1, R4, R7, R18, R21, R24, R27, R30, R33, R36, R39, R42, R45, R48, R51, R54, R57, R60, R63, R66, R69, R72, R75, R78, R81, R84, R87, R90, R93, R96, R99, R102, R105, R108, R111, R114, R117, R120, R123, R126, R129, R132, R135
80	DNI	R2, R3, R5, R6, R8, R9, R11, R19, R20, R22, R23, R25, R26, R28, R29, R31, R32, R34, R35, R37, R38, R40, R41, R43, R44, R46, R47, R49, R50, R52, R53, R55, R56, R58, R59, R61, R62, R64, R65, R67, R68, R70, R71, R73, R74, R76, R77, R79, R80, R82, R83, R85, R86, R88, R89, R91, R92, R94, R95, R97, R98, R100, R101, R103, R104, R106, R107, R109, R110, R112, R113, R115, R116, R118, R119, R122, R125, R128, R131, R134
6	120	R10, R121, R124, R127, R130, R133
1	2K	R12
2	0	R13, R16
1	105K, 1%	R14