avalanche technology

Platforms Enabled by Hi-Rel MRAM

Space Computing Conference / July 29th 2025

Paul Chopelas
General Manager, Aerospace and Defense

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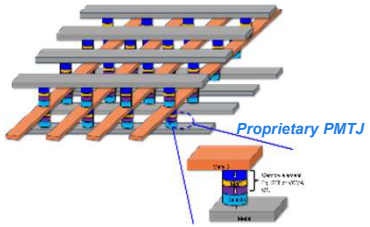
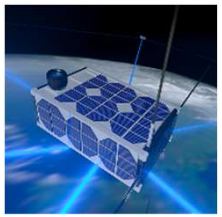
Avalanche Company Overview

Hi-Rel STT pMTJ MRAM since 2006



19+ years STT MRAM Experience

Focused on Space and Hi-Rel Industrial



Hi-Rel Industrial Heritage

Shipping volume to Industrial customers since 2019

Hi-Rel Focused

Domestic Technology

325
Granted Patents
& counting

Most Next-Gen/STT MRAM Patents Stateside

Growing Ecosystem

Growing Fab and Partner Ecosystem…

Avalanche's DARPA connection

Western Digital	**1996 - 2002**
GRANDIS	**2002 - 2008**
avalanche technology	**2008 - present**

Dr. Yiming Huai – *CTO/VP of Technology*

- Yiming was a co-founder, board member, CTO and VP of Engineering of Grandis, Inc, a pioneer in Spin Transfer Torque MRAM (STT-MRAM). Founded in 2001.
- Huai successfully raised more than $30M in private and government funding to develop STT MRAM.
- **Yiming has come full circle since the $14.7M in government funding from a DARPA program led by Dr. Dev Shenoy as Program Manager in 2008.**
- **Yiming came to Avalanche to achieve the goal of building a highly reliable dual use (industrial & space) MRAMs.**

All Avalanche Executive are Semiconductor Industry Veterans – see more at:
(https://www.avalanche-technology.com/company/leadership/)

Avalanche High-Rel MRAM Differentiator for Space & Missiles

Production Proven Products Today built on world class 22nm bulk CMOS process

Avalanche's MRAM solutions deliver all these attributes in one product line

Endurance

Endure **10^{16} write cycles / Unlimited read cycles** ensuring consistent performance

Performance

Faster read and write speeds with **low latency** compared to traditional memory; **scalable** without a proportional increase in complexity

Radiation

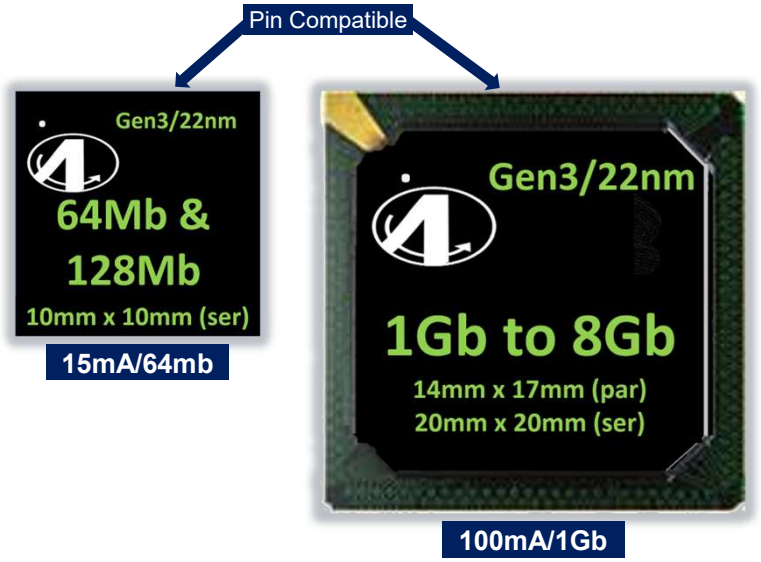
Bulk CMOS with radiation tolerant techniques. **TID >300kRad** and **SEE performance of ~75MeV cm²/mg**

Reliability

Engineered and tested for **harsh conditions** like space with exposure to high levels of **radiation** and **extreme temperatures. Built-in multi-bit ECC correction.**

Efficiency

Consumes **significantly less power** compared to traditional memory both in standby mode and read / write operations



With Volumes Comes Reliability (as of July 2025)

Total MRAM Devices Shipped = **1,690,829**

Total MRAM Terabits Shipped = **40.16 Tbits**

Industrial Devices = **1,676,461**

Industrial Terabits = **16.994 Tbits**

Space Grade Devices = **14,368**

Space Grade Terabits = **23.165 Tbits**

<u>To put that in perspective:</u>

it takes **379,534** x 64Mb Legacy MRAMs to store 23.165 Tbits

MRAM Radiation Summary[1]

SEL Immune[2]:

- 44 LET; Tested at 3.6V, 105°C & 125°C
- 62 LET; Tested at 3.0V, 105°C & 125°C
- 83 LET; Tested at 2.7V, 105°C & 125°C

SEFI/SEU Immune:

- 83 LET; Tested at 2.5V, Room Temp
- Dynamic testing (Write/Read/Compare loop)

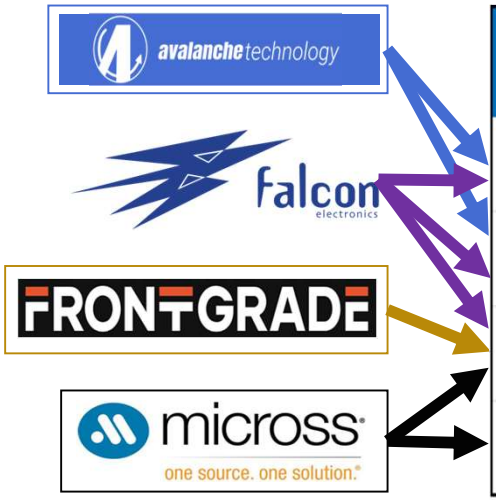
New design guide coming - Recommendations for design community

[1] – Testing performed by Frontgrade on Parallel MRAM Device

[2] – 4 parts statically tested, 1 part dynamically tested

Product Qual Levels for Gen 3 – Scalability by Mission Requirement

- Scalable Densities & Qual/Screening levels – from Earth to Mars!
- Customers have many pin-compatible (by package) upscreened options through Falcon, Frontgrade and Micross



Qual	Package	Temp	Let (MeV-cm^2/mg)	TID (Krad)	Burn In	Qual Syandards
Space Grade	Plastic	-40°C to 125°C	<= 55	75*	48 Hrs	JESD47H.01
Space Grade-E	Plastic	-40°C to 125°C	<= 75	100*	168 Hrs	JESD47H.01
PEMS I, II, III	Plastic	-40°C to 125°C	<= 75	100-300*	Custom	NASA-INST-0001
QML	Ceramic	-55°C to 125°C	75+	300*	Custom	QML-M to V

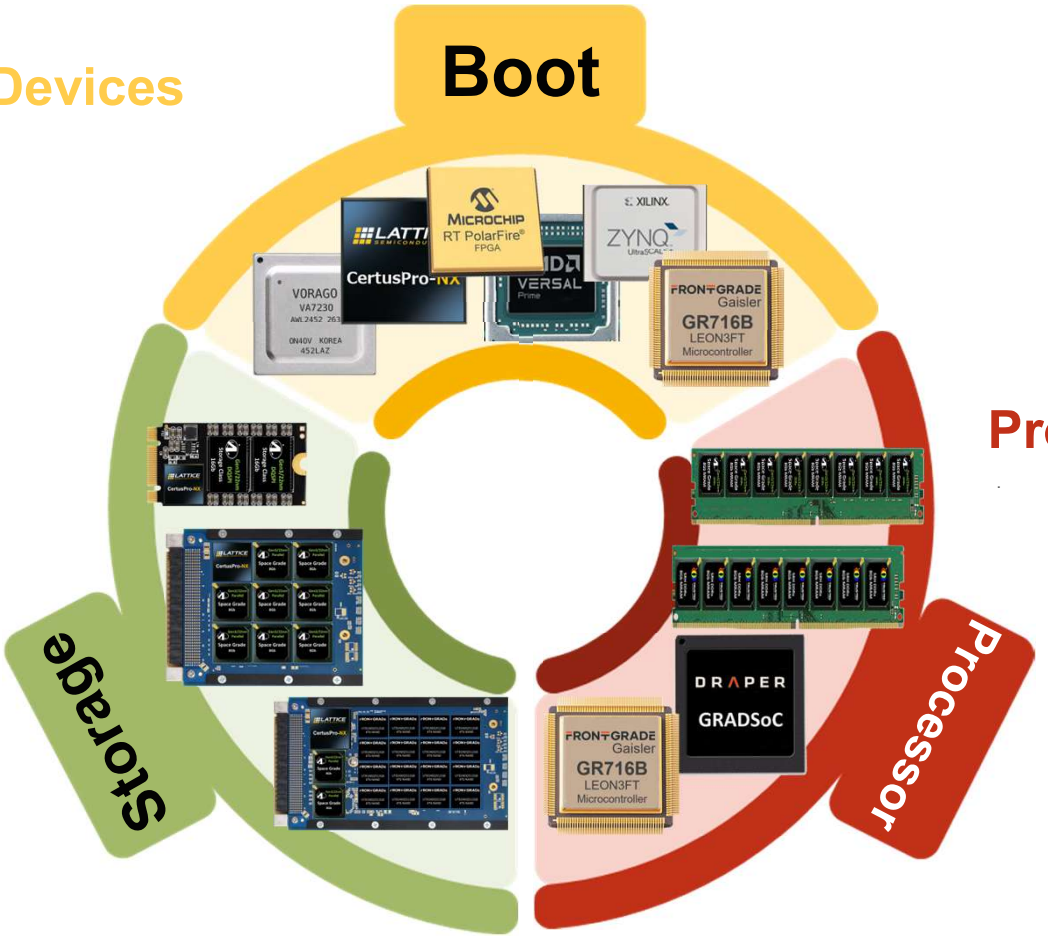
* Radiation performance tested durng Qualifaction and Characterization phase.

** Radiation/Qual reports for an indivdual lot are available through datapacks on quals above JESD47H.01

Aerospace Solutions – Enabling the Orbital Internet

De-risking each space mission – Avalanche offers the only reliable, scalable and low power memory solutions for satellites, rocket missions and data centers in space

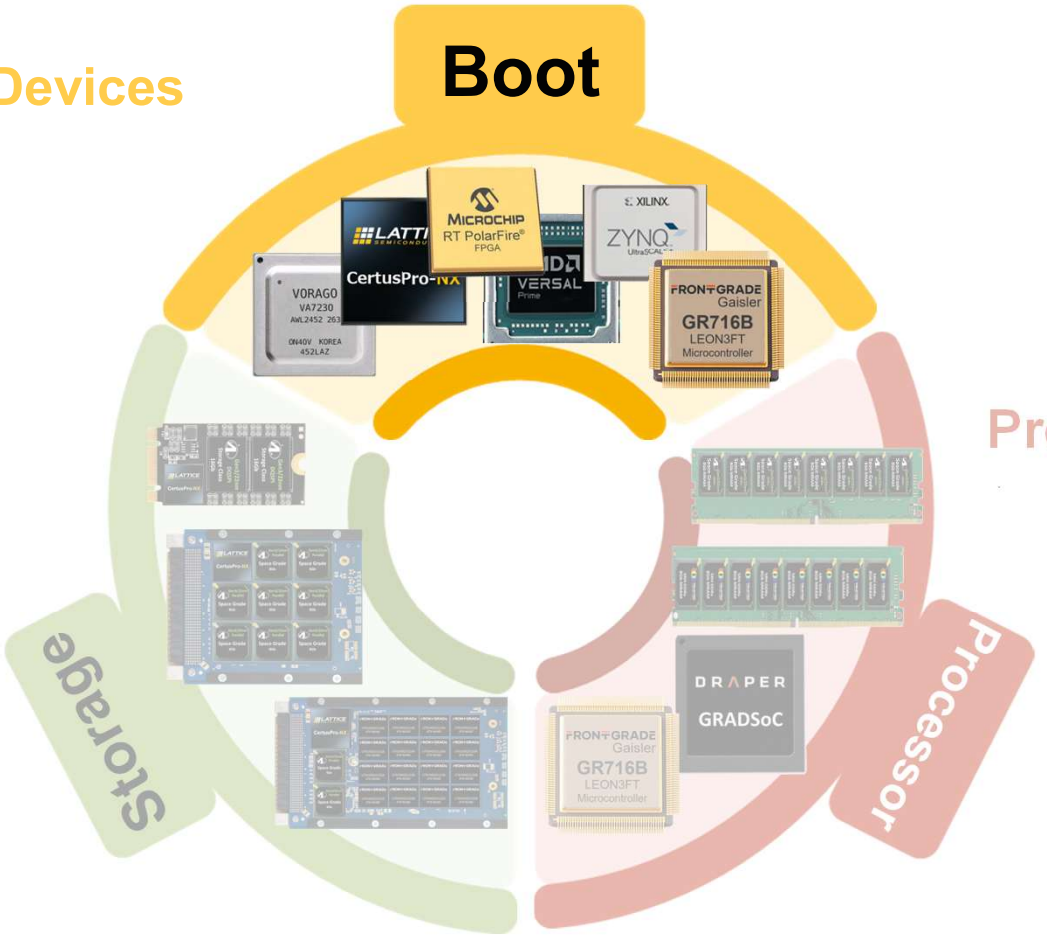
Boot Devices



Hi-Rel Storage

Highly Reliable Booting

Boot Devices

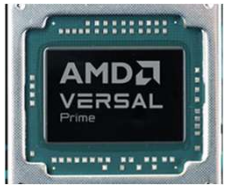


Processor Memory

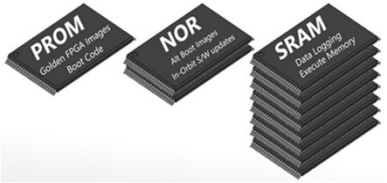
Hi-Rel Storage

AMD Xilinx | Enabled Booting and nvStorage for Devices

Software defined platforms for Space – respond to threats in real time



Historically Supported By



+ Radiation Mitigation & Control Circuitry

Now

- **No redundancy, mitigation** or **control** needed
- Dramatically **simplified HW & SW architecture**, **rapid boot**
- **In Orbit FOTA support**: multi-mission adaptability enabled
- Due to **high-endurance** (**wear leveling not needed)**, a Linux EXT4 drive format may be used with **no flash-file-system** for **higher system speed**.

Support Resources Available

Family	Petalinux Support				Fabric Only
	23.2	23.1	22.2	22.1	No O/S
Versal	✓	✓	✓	✓	✓
Ultrascale+	✓	✓	✓	✓	✓
Ultrascale	✓	✓	✓	✓	✓

Development Kit & Reference Design Available

GEN 3

Space Grade Dual QSPI P-SRAM™ Kit for Xilinx

Orderable Part Numbers:
Kit: AK30X208XILCCSOC
Socket: ABGA96-1-20x20
*One socket included with each kit

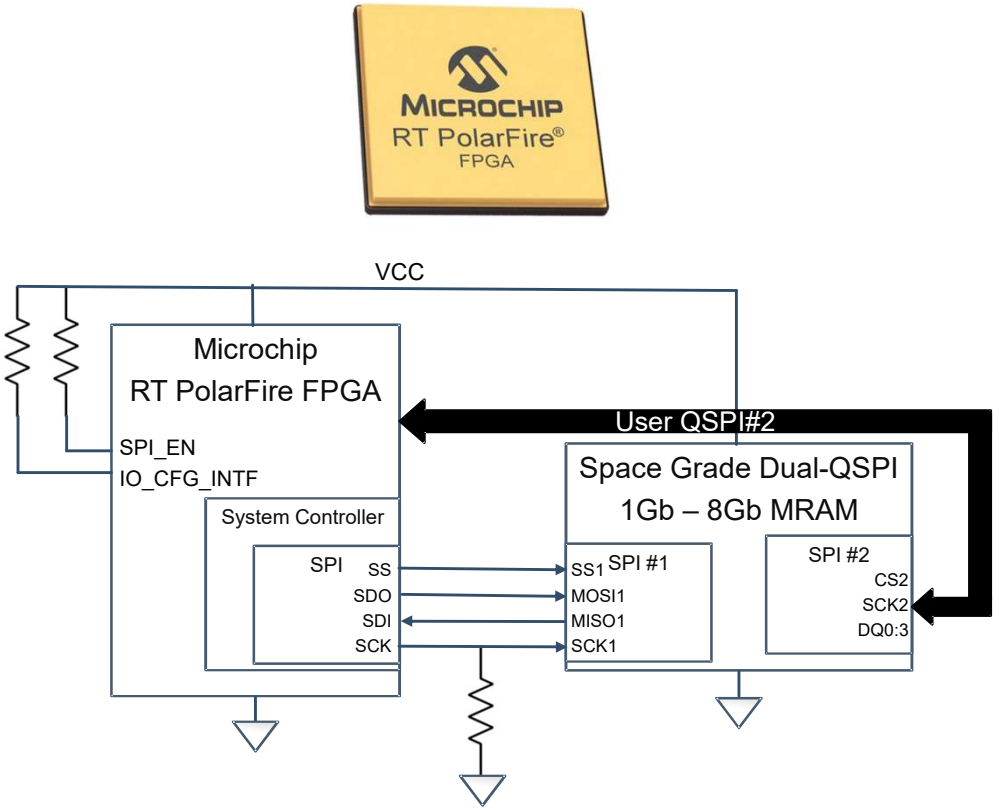
Development Kit: Boot Drivers; User Guide; Sample Code

Reference Design: Schematic, Board Layout, Gerber, BOMs

Microchip | Enabled Auto-Updating RT PolarFire's Flash

Auto-Updating RT PolarFire FPGAs with MRAM

- RT PolarFire use **SFDP (Serial Flash Discoverable Parameters)** – part of the **JESD216** standard
- Avalanche DQSPI MRAMs do not support SFDP
- However, Avalanche DQSPI MRAMs have **successfully auto-updated the RT PolarFire's on-board flash** using its **extended address register**



Vorago | Reliable Booting for ARM-M4 Family of SoCs

Pin Compatible Boot Solutions

Compact Images
10x10mm FBGA

Multi Mission Images
20x20mm FBGA

Config Bit Stream

Serial I/F

VA41630
RH ARM M4 MCU

VA7230
RT Edge Processing MPU

Frontgrade/Lattice | Enabling Booting for FPGAs/SoCs

Pin Compatible Boot Solutions

Compact Images
10x10mm FBGA

Multi Mission Images
20x20mm FBGA

Config Bit Stream

Serial I/F

UTC24CP1008	**UT32M0R500**
FPGA	SoC

Frontgrade | Enabling Booting & Working Memory for Gaisler GR716 LEON3FT Processor

Config Bit Stream

Serial

Config Data

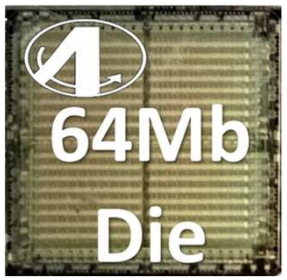
Config & Mem Interface

& Working Mem

Dual QSPI

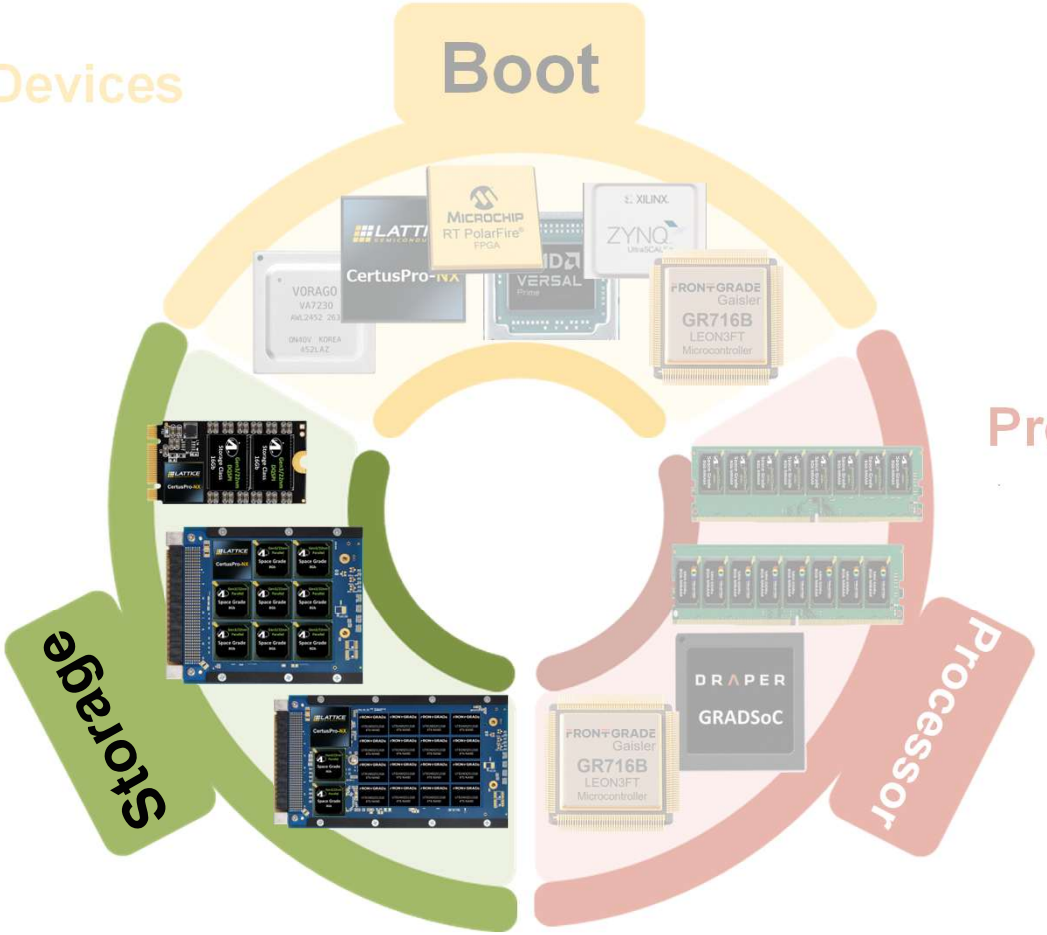
64Mb and 128Mb

Gen3/22nm



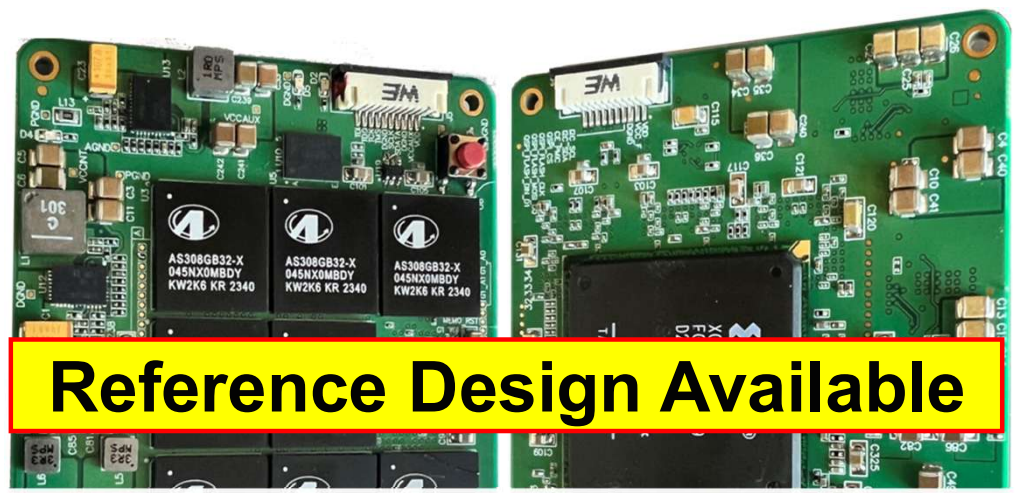
Highly Reliable Storage

Boot Devices



Hi-Rel Storage

Storage Solutions for Space



Reference Design Available

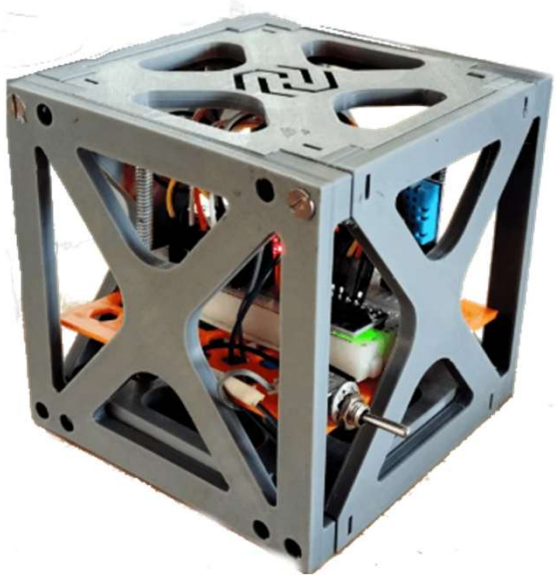
Avalanche provides reference design with low level drivers

Partnership with EIDETICOM enabled plug and play NVMe stack

Storage Solutions for Space and Military

Scanning satellites in LEO need data buffers.

VNX-Plus Data Buffer for LEO Satellites (8GB MRAM)



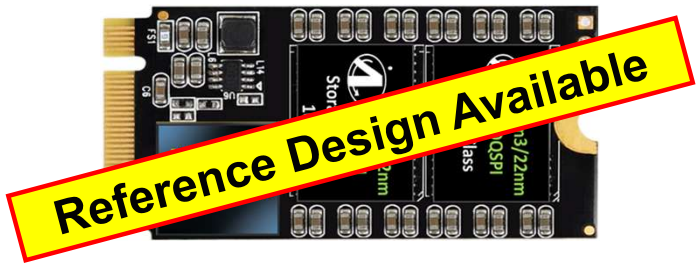
Module will be available as an evaluation card and as a reference design.

Storage Solutions for Space and Military

Communication Satellites in MEO need Hybrid drives

3U VPX Hybrid Data Storage (32Gb MRAM/1TB NAND)

Storage Solutions for Hi-Rel Avionics

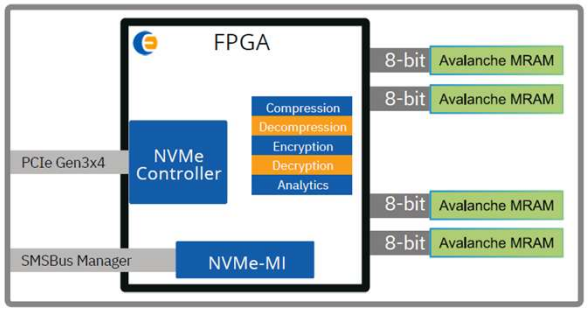


- High Density (up to 4GB today)
- Highest Endurance (10^{16} write cycles)
- High Reliability (Embedded ECC)
- Soft Error Immune
- Standard PCIe Gen 3 Interface
- Multiple Channels
- Low Latency
- No Wear Leveling Required

Specification	
FPGA	Lattice Certus Pro-NX 4 Banks of 8Gb x 8 Bits
On Board MRAM	Avalanche STT MRAM Upgradable to o 8GB (default 4GB) Transfer rate 0.8Gb/sec total bandwidth
Host Interface	PCIe Gen3x4 M.2 Connector Software Upgradable to NVMe Interface
Data Logging Features	Infinite instant non-volatile writes with no wear leveling
Development Features	JTAG connector for access to FPGA and debug tools Voltage Monitoring
Power Supply Monitoring	Fault condition reporting
Cooling	M.2 drive optimized for cooling without a heatsink
Electrical	On-card power delivered from M.2 supplies. Typical power consumption ~5W
Environmental	Operating temperature: -40 to 125 C
Quality	IPC-A-610Class 2. RoHS Compliant
Form Factor	M.2 Compliant 44mm drive form factor. Height 1.5mm
Available Accelerators	Compression, Encryption, Analytics

Key Features

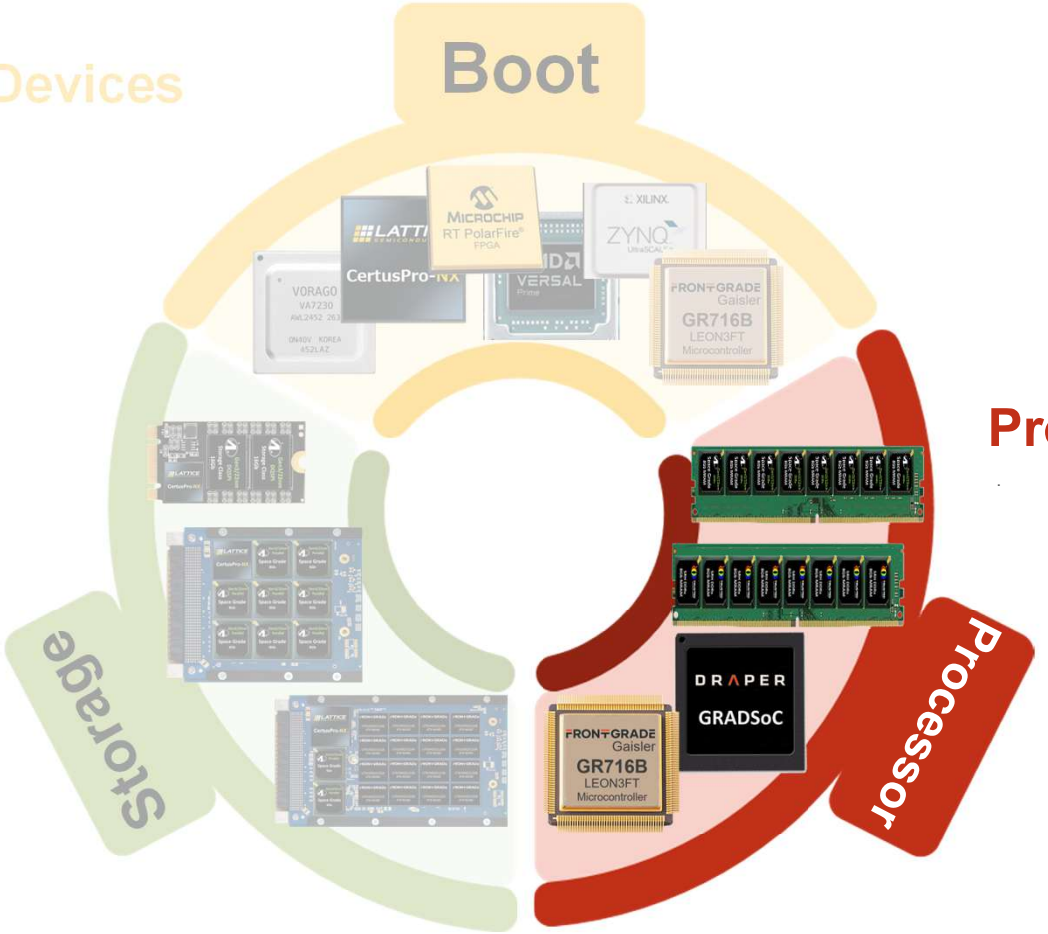
PCIe Gen3 | **NVMe** | **Up to 8GBytes MRAM** | **Lattice FPGA With 100k Logic Elements**



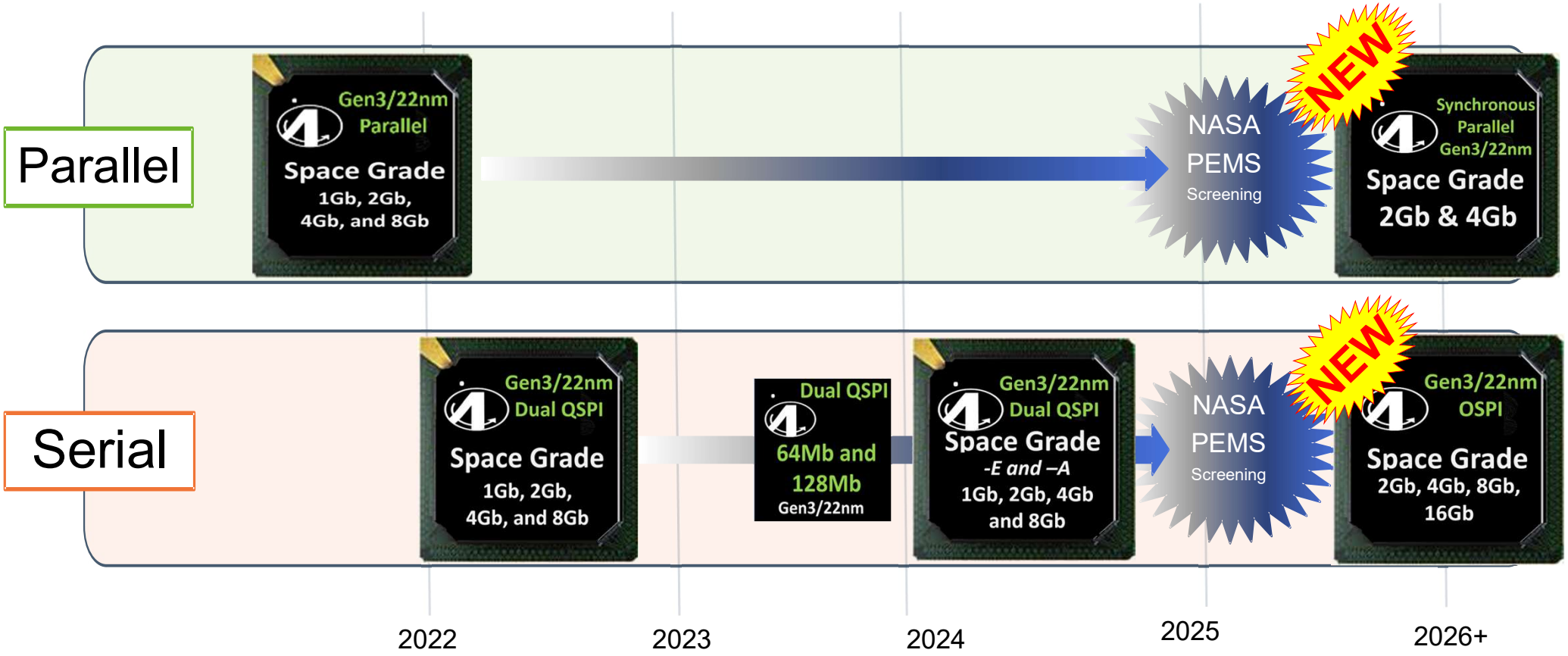
Highly Reliable Processor Memory

Boot Devices

Hi-Rel Storage



Avalanche Parallel/Serial MRAM/Processing Product Roadmap Update



Support Resources @ www.avalanche-technology.com

Datasheets, models, reference designs

Boot module: Petalinux drivers, User Guide (Versal boot)
Gen 3 reference designs
IBIS & Verilog models

Radiation test reports

Gen 2 test report accessed via website (NASA)
Gen 3 reports available by request

Visionary White Papers

Innovation enabled by Avalanche
Data Centers in Space…
…why the key to satellite scalability and resilience
NEW: AI Computing in Space

Newsletters

Quarterly, register on main page

Brochures

Overall MRAM tech for hi-rel apps
Space Grade products

Space-centric Blogs

Datacenter in Space series
Why our MRAM is ideal for space

Gen 3 Dev Kit Options for DQSPI – 64Mb to 8Gb

High Density DQSPI (1Gb to 8Gb) – 96-ball (20x20mm)

Dual QSPI P-SRAM™ Dev Kit

- **Complete eval kit** uses Lattice MACHX03 FPGA board connected to Avalanche MRAM daughterboard via standard QSPI I/F & Arduino connector.
- Host control w/ embedded ARM via micro-USB port.
- Part number: AK30x208LATCCSOC

For evaluation & prototyping of h/w to interface with our high-density devices to most FPGAs & SoCs, minus those that use VCK190 like Versal. Optimized for multiple mission images.

Dual QSPI P-SRAM™ Plug In Card for Xilinx VCK19X Board

- **Plug-in card** for existing Xilinx/AMD VCK19X dev kits.
- Supports rapid booting of Xilinx/AMD Versal & UltraScale+
- Connects via Samtec connector
- Part number: AK30x208XILCCSOC

For evaluation & prototyping of hw to those that use VCK190 like Versal

Low Density DQSPI (64Mb & 128Mb) – 56-ball (10x10mm)

- **Complete eval kit** uses Lattice LCMXO3L/LF-6900C FPGA board connected to Avalanche socketed daughterboard via proprietary Asynchronous SRAM I/F.
- Host control w/ embedded ARM via micro-USB port.
- Part number: AK30X208LATCTSOE

For evaluation & prototyping of h/w to interface with our low-density devices to FPGAs & SoCs with compact mission image requirements.

Advanced Boot Solutions Enabling SW-Defined Platforms

Avalanche Technology Announces Support for NASA PEMS Qualifica and Screening

In response to unprecedented demand for extended qualification & screening flows, Avalanche rolls out pin compatible NASA PEMS options for enabling Dual QSPI MRAM family.

FREMONT, CA, April 8, 2024 — Avalanche Technology, the leader in next generation MRAM technology, announced today the launch of a new product derivative to address the growing demand from the aerospace and defense community for extended qualification and screening solutions, particularly NASA PEMS INST-0001.

Leveraging Avalanche's Gen 3 Space Grade MRAM products being broadly adopted by the defense industrial base and commercial space customers, the new pin compatible PEMS qualified and screened versions of the popular Dual QSPI MRAMs will roll out mid-year.

alanche Technology Selected to Support Mercury's First Space-Qu Processing Board Using AMD's Xilinx Versal AI Core

mercury systems.

Mercury is leveraging Avalanche's PSRAM(TM) products to build the next family of SWaP optimize orbit software-defined processing platforms

FREMONT, Calif., Nov. 8, 2023 /PRNewswire-PRWeb/ — Avalanche Technology, the leader in next generation MRAM technology, announced today that its Persistent-SRAM (P-SRAM) products were by Mercury Systems for the new SCFE6933, a next-generation processor board that will enable fa processing of data in orbit. The high-density 8Gb DQSPI Space Grade Persistent SRAM with furthe scalability is the ideal companion to the AMD (Xilinx) Versal Adaptive SoC platform that is feature platform.

Thank You

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