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Avalanche Boot Solutions for Xilinx Versal

Using our single 8Gb MRAM to Boot Versal + RTOS + working mem

Paul Chopelas, General Manager, Aerospace and Defense

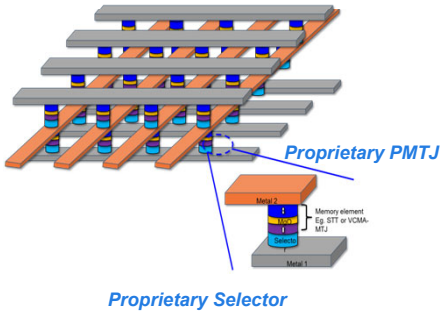
Sept. 20, 2022

Agenda

- Company Overview & Technology Background
- What did Avalanche do differently?
- Radiation lollapalooza
- Unified Memory Model
- Making the Sausage
- Booting a Versal
- Demo with VCK190
- Summary – Q&A

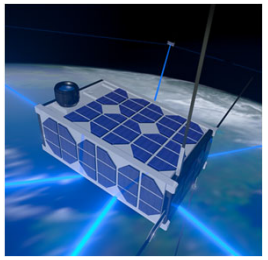
Avalanche Company Overview

Hi-Rel STT pMTJ MRAM since 2006



15+ years STT MRAM Experience

Focused on Space and Hi-Rel Industrial



Hi-Rel Industrial Heritage

Shipping volume to Industrial customers since 2019

Hi-Rel Focused

Domestic Technology

325 Granted Patents & counting

Most Next-Gen/STT MRAM Patents Stateside

Growing Ecosystem

micross one source. one solution.
RENESAS BIG IDEAS FOR EVERY SPACE
Falcon electronics
XILINX
MICROCHIP
APOGEE SEMICONDUCTOR™
Protec GmbH Vertrieb elektronischer Bauteile
Lattice Semiconductor Corporation
NanoXplore
RADIATION TEST SOLUTIONS
UMC
SONY
Linear ASICs Inc.

Growing Fab and Partner Ecosystem…

Focused Markets and Applications

Products custom designed for each segment – *ALL with High-Reliability in mind*

Retention/Hi Temp — Efficiency/Power — Speed/Latency

A & D

- Space Storage
- Automation
- Security System
- Navigation
- System Log
- Black Box

Industrial

- Smart Meter
- POS
- Touch Sensors
- Set-top Boxes
- Data Loggers
- MFP, CNC, PLC

Storage

- SSD Controllers
- Storage/RAID
- Controllers
- Buffers
- NV Cache
- Server Processor

IoT

- Wearables
- Smart TVs
- Intelligent Sensors
- Home Security

Notes:
1/2/3: Source Gartner Semiconductor Forecast 2018

What's Different?

Non-NDA Version

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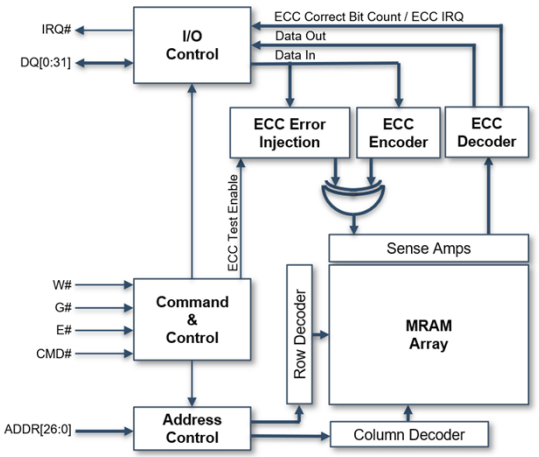
The Result: What Makes Avalanche MRAM Different?

The Best SWAP-C (Size, Weight, Power, Cost) profile of any High-Reliability NVMs, especially for Space!

- Supports unified memory architecture
- Designed for the **Highest Reliability:**
  - Robust **On-chip ECC with multi-bit correction**
  - **Error-free** non-destructive read w/ unlimited endurance
  - Error-free writes with:
    - **10^{16} endurance for space**
    - **10^{14} endurance for industrial**
- **Ultra Low Power** (as low as 10mA per Gb)
- Compact differential MRAM Structure (2 MRAMs per bit)
- Terrestrial applications can leverage Hi-Rel benefits!!



Gen3/22nm Data Retention[1]

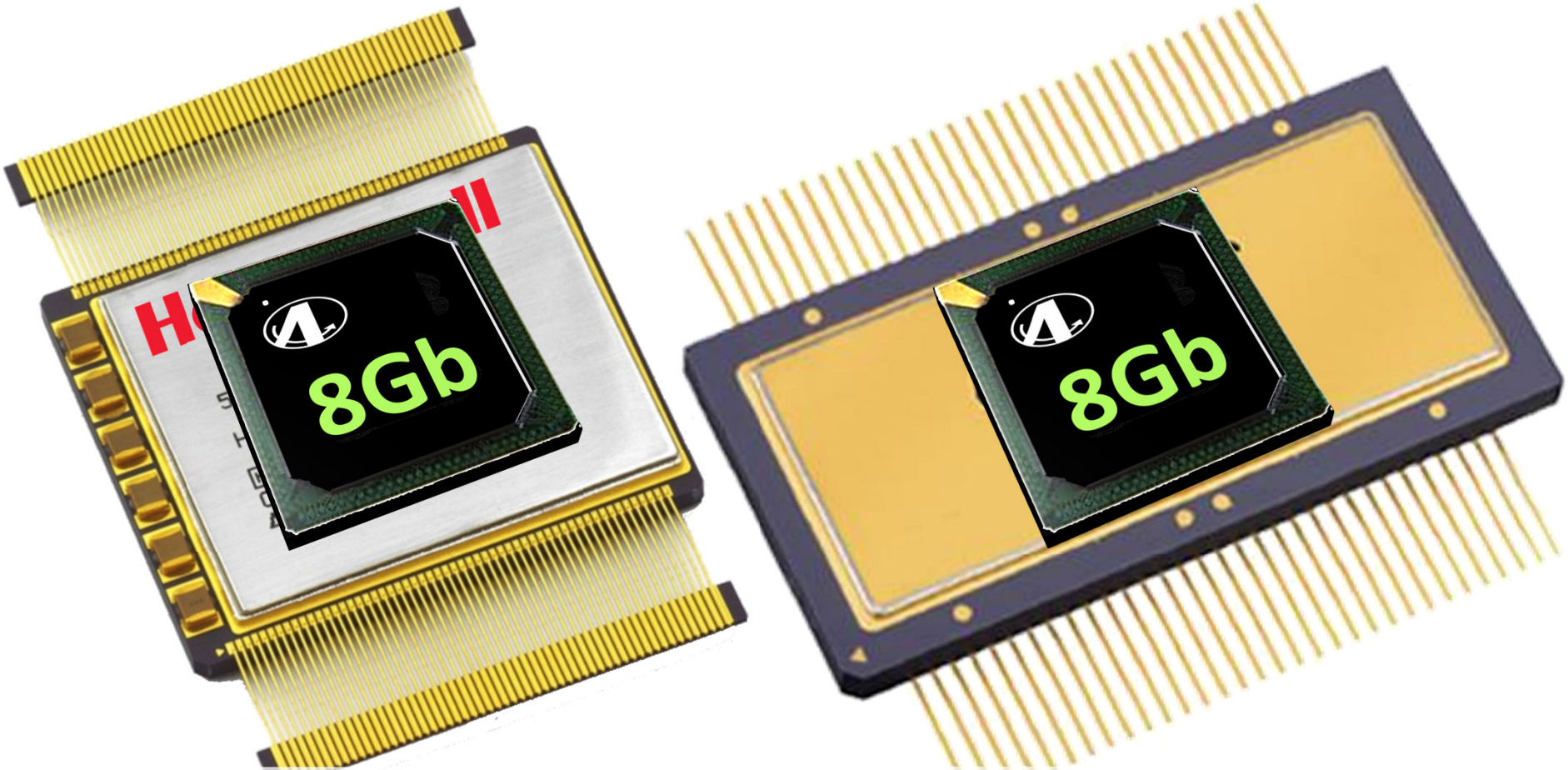
Parameter	Tempurature	Minimum	Units
Data Retention	125° C	10	Years
	105° C	10	
	85° C	1,000	
	75° C	10,000	
	65° C	1,000,000	

85°C is a common satellite system temp

[1] – Gen3 Space Grade Parallel MRAM – Table 16 'Endurance and Data Retention'

Avalanche MRAMs are designed to outlast the operating life of the system!

SWAP-C Improvement for Space **64Mb vs 8Gb**



FBGA = 1200mm^2 vs 400mm^2 (33%)

128x density = 384x bit/mm^2

64Mb @ 100mA[1] vs **8Gb** @ 90mA

> 100x more power efficient

[1] - Recommended to run at half-rate to cut power by 50%

Radiation lollapalooza

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Screening, TID, SEE Levels at-a-glance

Company	Grade	Qual Level	ITAR	TID	SEE	Form Factor
Avalanche, Renesas	Industrial	Jedec	No	<10KRad[1]	<8MeV	Plastic Package
Avalanche	Space-Grade	Jedec+48H Post Burnin	No	<75kRad[1]	~Leo	Plastic Package
Micross	RadTolerant, Rad-Hard, Custom	QML, Custom	Yes	>300kRad	~75MeV	Plastic, Hermetic, Die, Wafer, MCM

1 - In-package TID Limiter

Heterogeneous Integration & Specialty Flow Support

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Space Grade

Speed: 45ns
Temp: -40 to 125°C
Endurance: 10^{16}
Retention: 10 years

TID: <75KRad
Flow: Space Grade
Qual: JEDEC w/ 48Hr Burn-in
Product: Plastic (RoHS/Pb Balls)
ITAR: No

micross
one source. one solution.™

RadHard

Speed: 45ns
Temp: -55 to 125°C
Endurance: 10^{16}
Retention: 10 years

TID: >300KRad
Flow: QML, Space, MIL Ind, Custom
Qual: QML Q,V,H,K,Y, & Custom
Product: Hermetic, Die/Wafer, Plastic
ITAR: Yes

Avalanche & best of breed partners - support for DoD Community - Space and RadHard

Gen3 SEE/TID Results & Upcoming SEE/TID Plans

Device	Test Environment	Test Facility	Dates	Test Participants	Test Results
Redacted for open meeting *(working on open release of all radiation test information from 3rd parties)* *If you are interested in receiving this data, please reach out to* *Kristine@avalanche-technology.com*					

Unified Memory Model

Non-NDA Version

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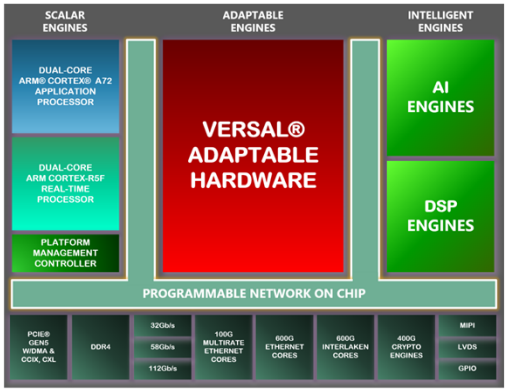
Unified Memory Example - Xilinx Versal & Avalanche MRAM

Yesterday



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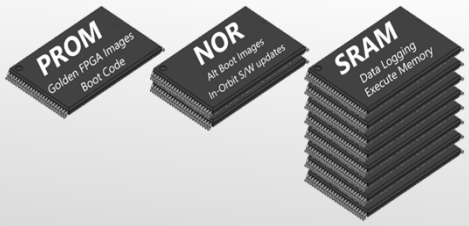
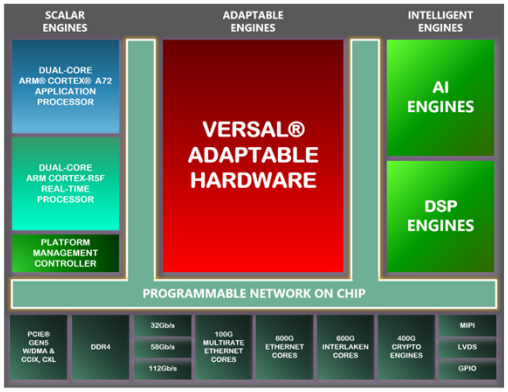


Avalanche Enabling Today

[1] Virtual ROM/PROM (Read Only) – can be any size, up to full MRAM capacity
[2] Virtual FLASH (Write Protectable) – can be up to remaining size of MRAM
[3] Persistent SRAM (data preserved on power fail) – remaining capacity minus PROM + NOR

Unified Memory Example - Xilinx Versal & Avalanche MRAM

Yesterday



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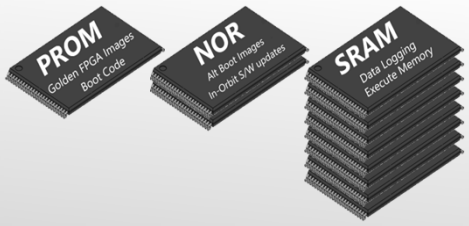
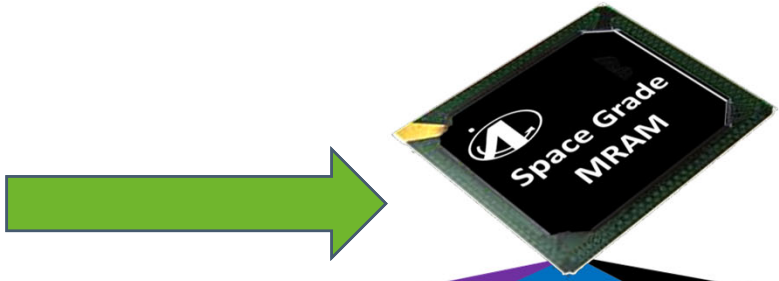


Read Only
No software overrides

- Direct Programming Method demonstrated
  - Config images + RTOS
- Indirect Programming Method in development
- Support Deliverables (Oct & Nov):
  - Quick Start Guide & Article
  - Plug in card for Xilinx VCK190 & Alpha Data boards

Avalanche Enabling Today



Remainder of Array is Persistent Read/Write

PROM[1]
Golden FPGA Images
Boot Images
Read Only

NOR[2]
Alt Boot Images, RTOS, etc.
In-Orbit S/W updates
Write Protectable

P-SRAM[3]
Data Logging
Execute Memory
Read/Write

[1] Virtual ROM/PROM (Read Only) – can be any size, up to full MRAM capacity
[2] Virtual FLASH (Write Protectable) – can be up to remaining size of MRAM
[3] Persistent SRAM (data preserved on power fail) – remaining capacity minus PROM + NOR

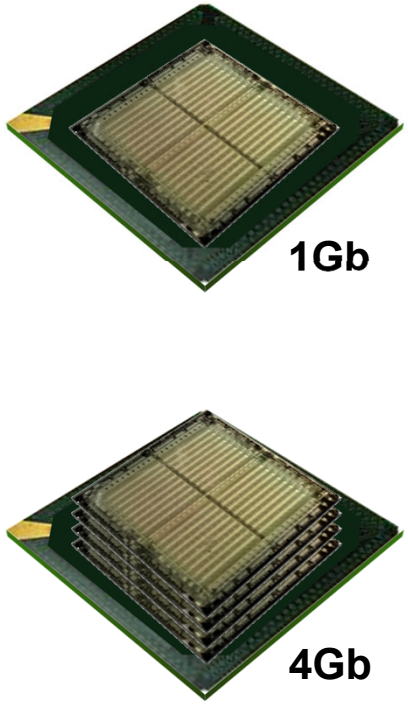
Write Protected
Software override up to Read-Only Area

Parallel, Serial and DDR MRAM device architecture

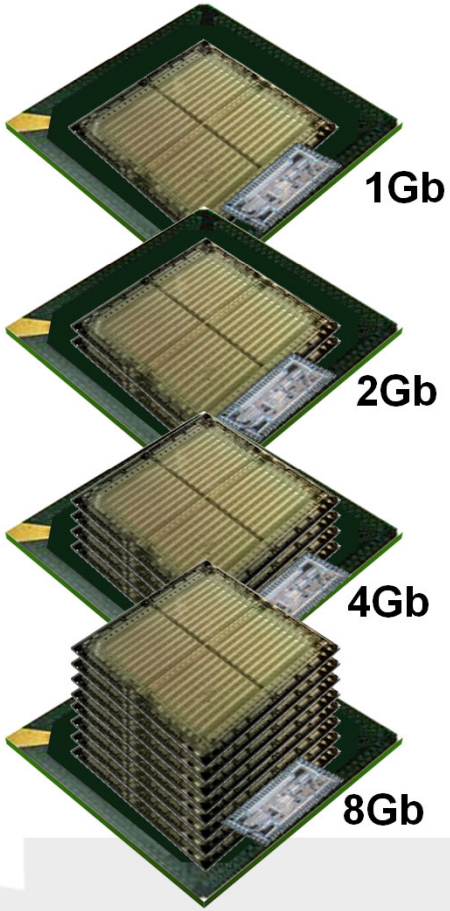
1Gb Tile is Stackable

Adding in-package chiplet to “streaming interface”

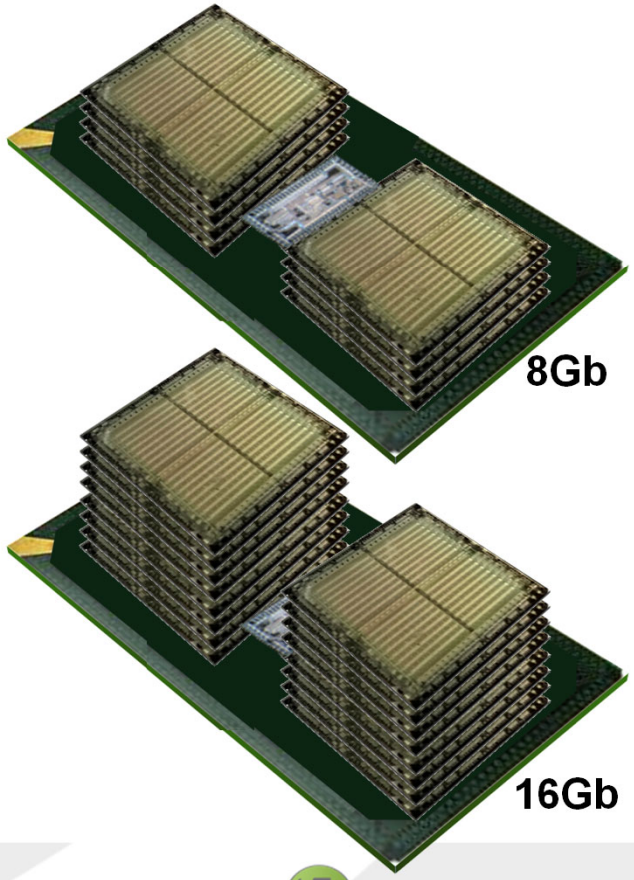
Parallel



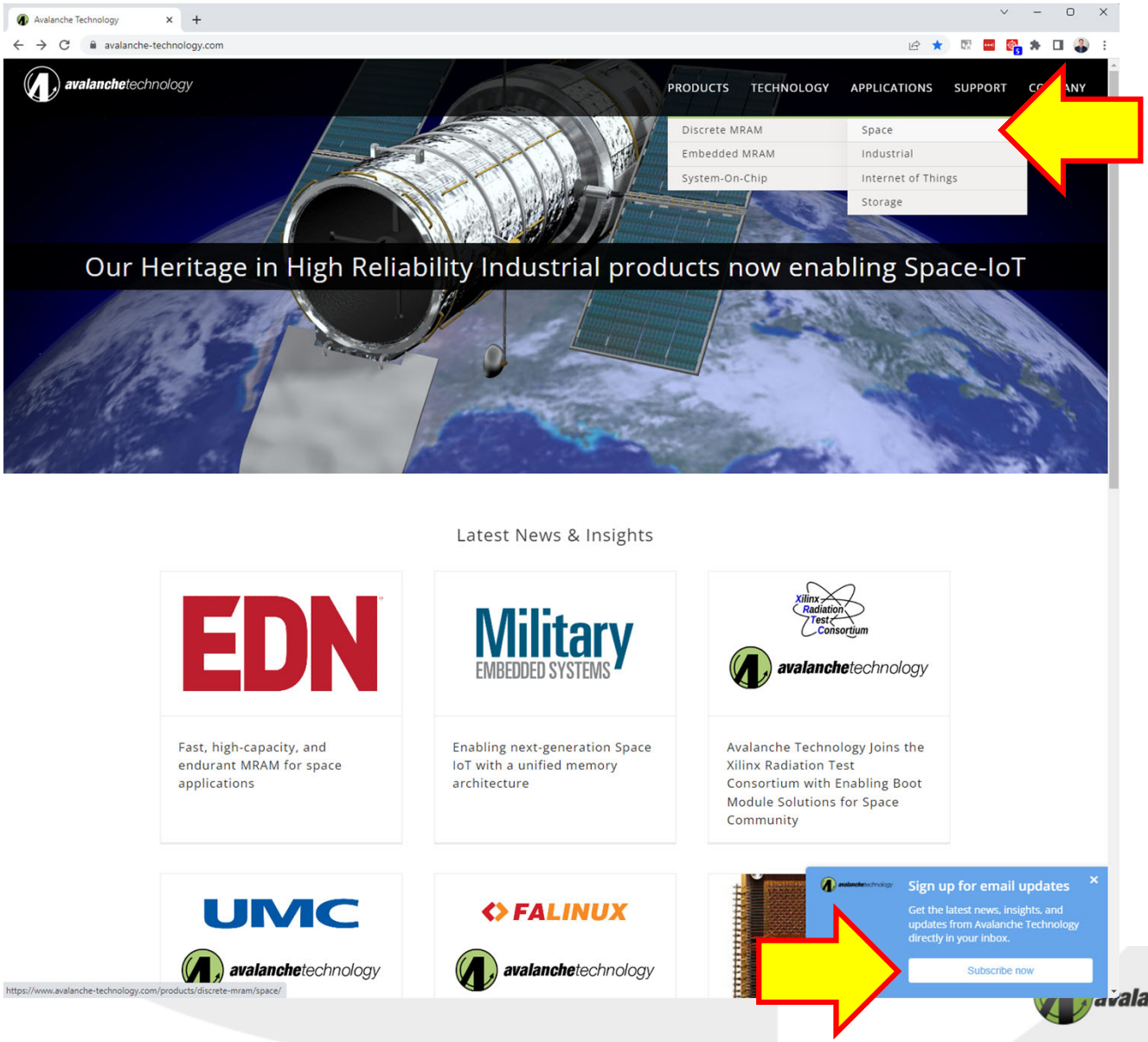
Dual QSPI



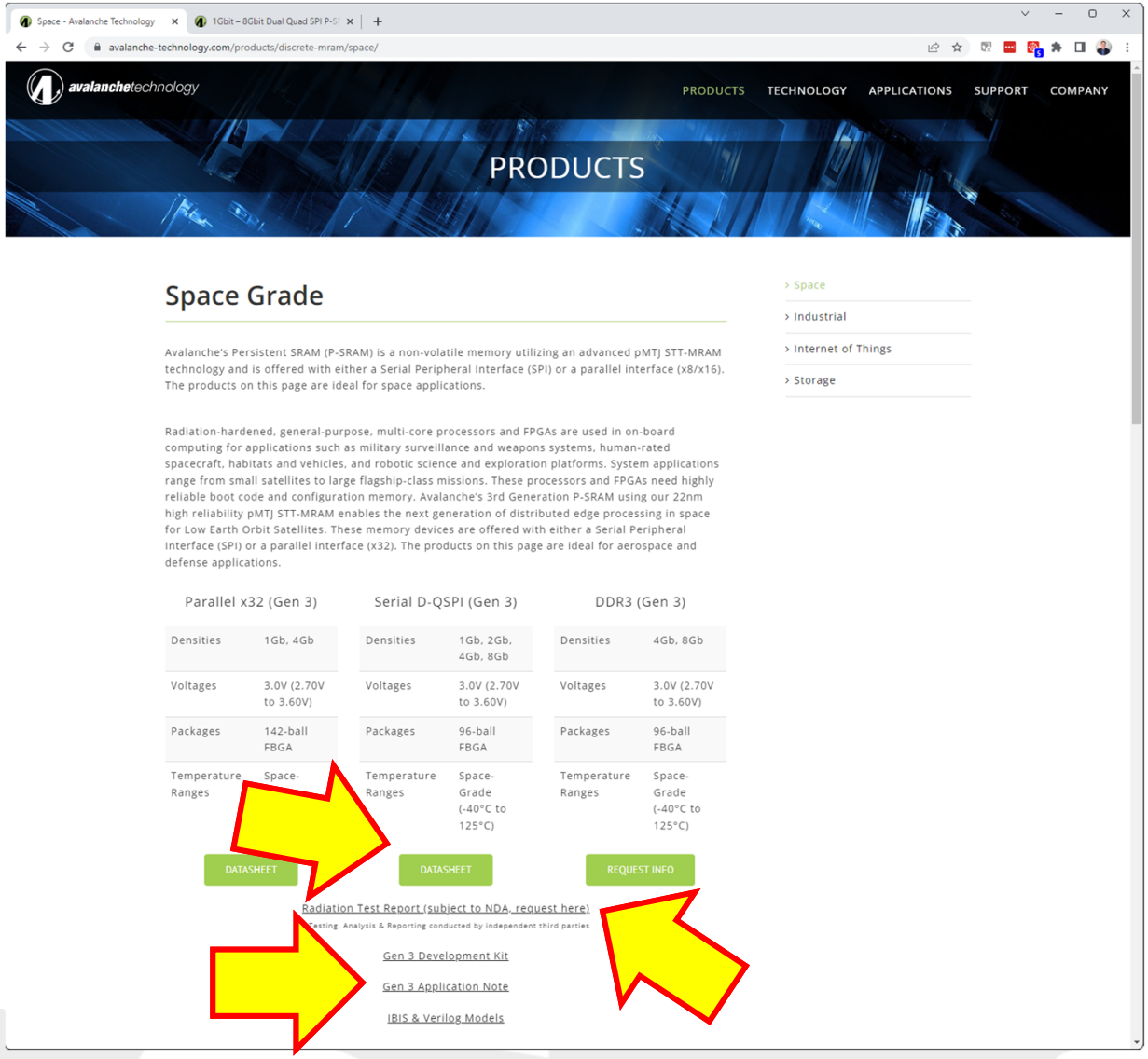
DDR3



Avalanche P-SRAM Space-Grade Devices



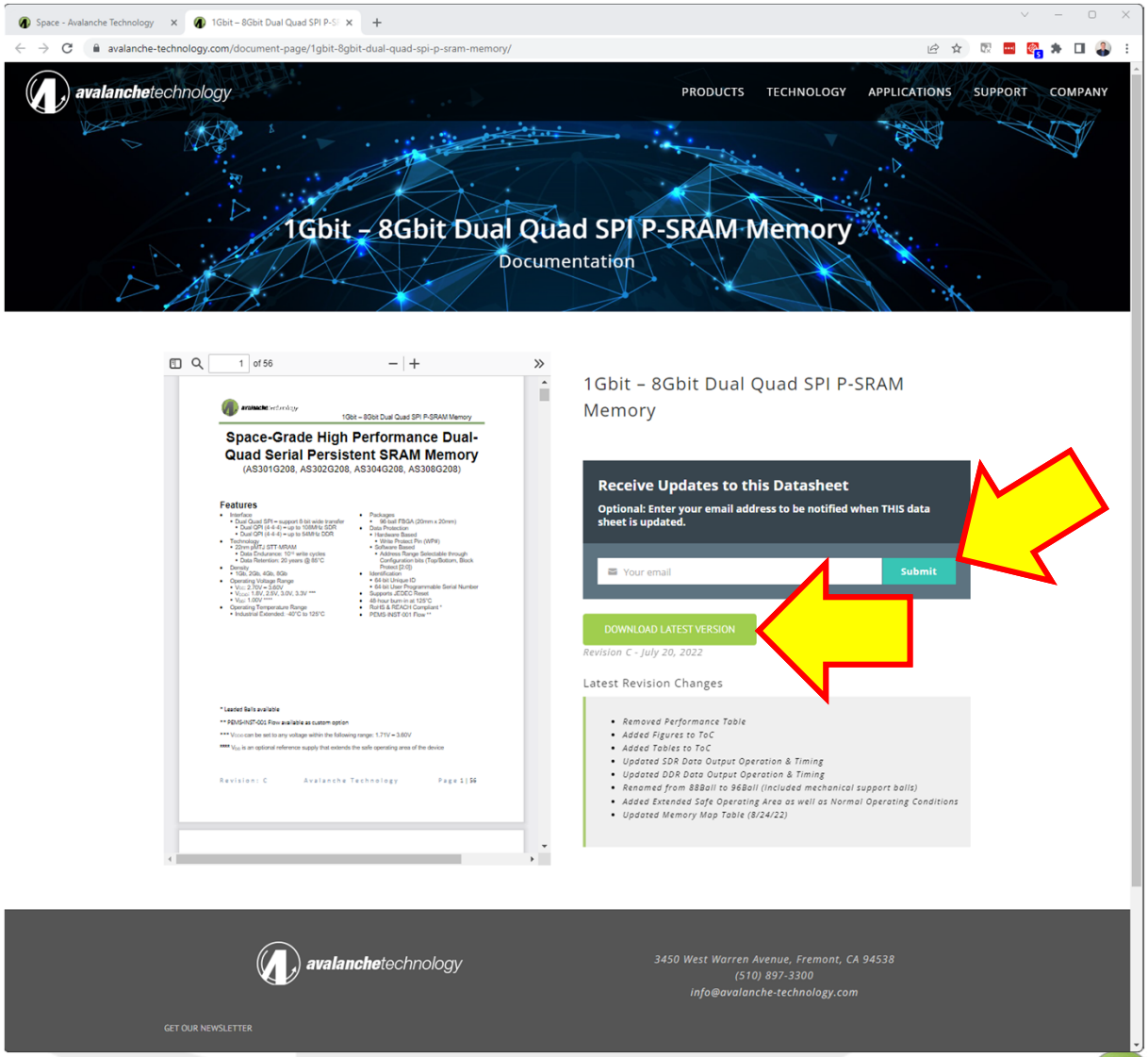
Gen3 Space-Grade Dual-QSPI Devices



Support Collateral includes:

- Datasheets
- Dev Kits
- App Notes
- IBIS & Verilog Models
- Reference Designs

Gen3 Space-Grade Dual-QSPI Datasheet



Parallel Devices

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Spin Programmable Solutions

Space Grade Parallel Persistent SRAM Memory

(AS301GB32, AS304GB32)

Features

- Interface
  - Parallel Asynchronous x32
- Technology
  - pMTJ STT-MRAM
    - Virtually unlimited Endurance and Data Retention (see Table 16)
- Density
  - 1Gb, 4Gb
- Memory Array Organization
  - 1Gb
    - 33,554,432 x 32
  - 4Gb
    - 134,217,728 x 32
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.0V, 3.3V ***
  - V_{DD}: 1.00V ****
- Operating Temperature Range
  - -40°C to 125°C
- Packages
  - 142-ball FBGA (15mm x 17mm)
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

* Leaded Balls available

** PEMS-INST-001 Flow available as custom option

*** V_{CCIO} can be set to any voltage within the following range: 1.71V – 3.60V

**** V_{DD} is an optional reference supply that extends the safe operating area of the device

Figure 5: Functional Block Diagram

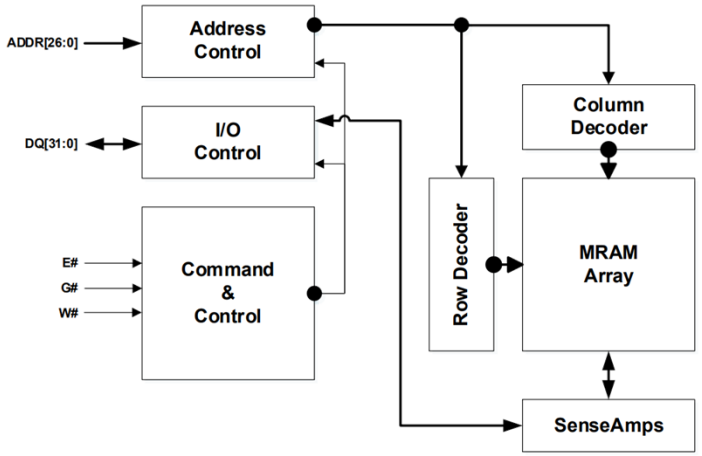

Table 4: Modes of Operation

Mode	E#	G#	W#	Current	DQ[31:0]
Not Selected	H	X	X	I_{SB}	Hi-Z
Output Disabled	L	H	H	I_{READ}	Hi-Z
Output Disabled	L	X	X	I_{READ}	Hi-Z
Read Word	L	L	H	I_{READ}	Data-out
Write Word	L	X	L	I_{WRITE}	Data-in

Notes:
H: High (Logic '1')
L: Low (Logic '0')
X: Don't Care
Hi-Z: High Impedance

Gen3 Space-Grade Dual-QSPI Densities/Architecture

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1Gbit – 8Gbit Dual Quad SPI P-SRAM Memory

Space-Grade High Performance Dual-Quad Serial Persistent SRAM Memory

(AS301G208, AS302G208, AS304G208, AS308G208)

Features

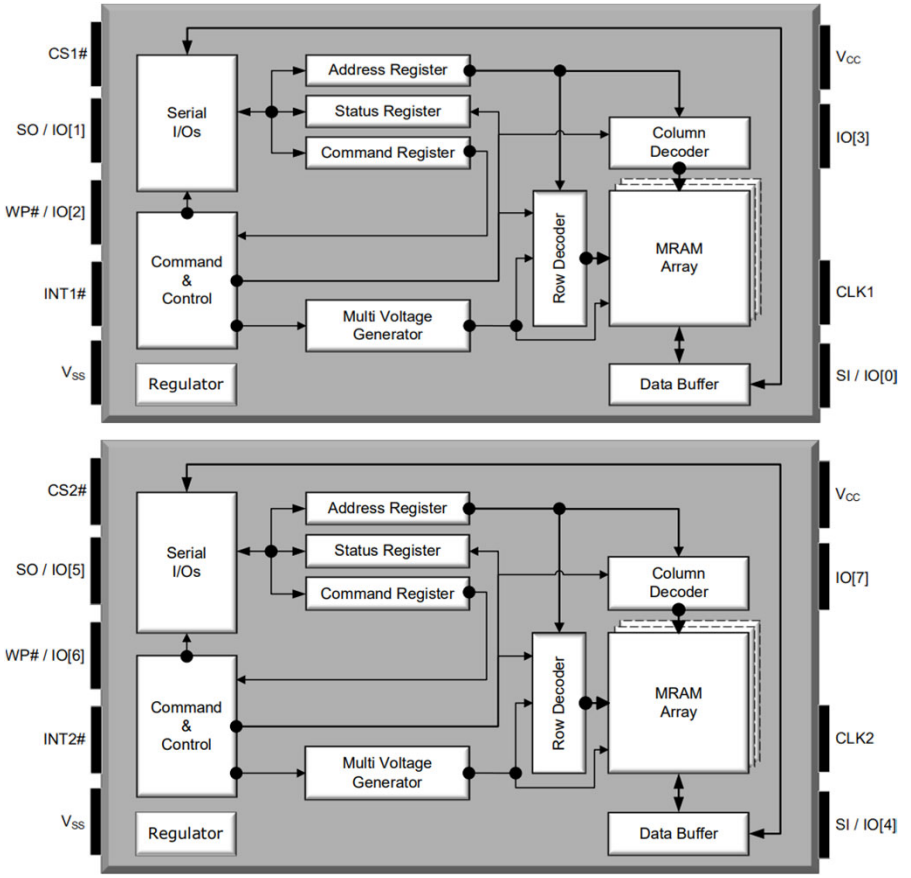
- Interface
  - Dual Quad SPI – support 8-bit wide transfer
    - Dual QPI (4-4-4) – up to 108MHz SDR
    - Dual QPI (4-4-4) – up to 54MHz DDR
- Technology
  - 22nm pMTJ STT-MRAM
    - Data Endurance: 10^{16} write cycles
    - Data Retention: 20 years @ 85°C
- Density
  - 1Gb, 2Gb, 4Gb, 8Gb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.0V, 3.3V ***
  - V_{DD}: 1.00V ****
- Operating Temperature Range
  - Industrial Extended: -40°C to 125°C
- Packages
  - 96-ball FBGA (20mm x 20mm)
- Data Protection
  - Hardware Based
    - Write Protect Pin (WP#)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Identification
  - 64-bit Unique ID
  - 64-bit User Programmable Serial Number
- Supports JEDEC Reset
- 48-hour burn-in at 125°C
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

* Leaded Balls available

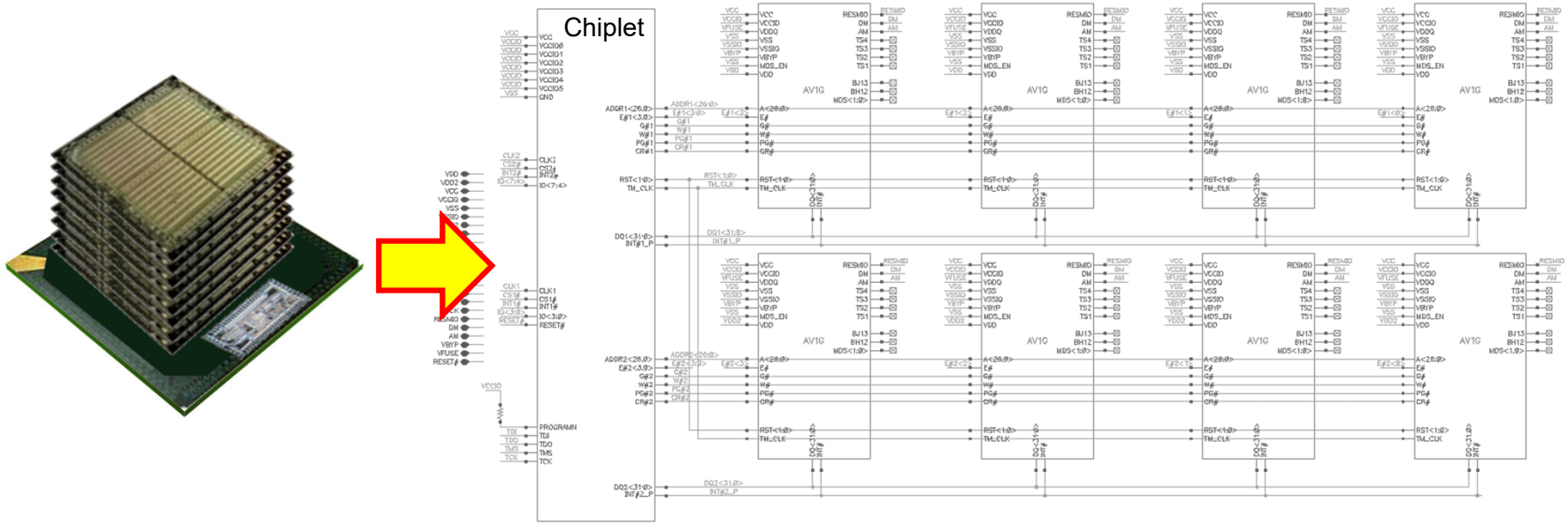
** PEMS-INST-001 Flow available as custom option

*** V_{CCIO} can be set to any voltage within the following range: 1.71V – 3.60V

**** V_{DD} is an optional reference supply that extends the safe operating area of the device



Gen3 Space-Grade Dual-QSPI Construction



Retire Risk by Creating New Variants with a Packaging Exercise

Booting a Versal

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Versal Primary Boot Modes w/ QSPI, DQSPI, or OSPI

#2

#1

Mode	MODE[3:0] Pins	PMC I/O Pins	Secure Boot Capable	Data Bus Width	Description
Interfaces controlled by external devices					
JTAG	0000	Dedicated I/O	No	1-bit	Dedicated JTAG interface
SelectMAP	1010	MIO[51:28, 25:14]	Yes	8-bit, 16-bit, 32-bit	SelectMAP bidirectional parallel data bus interface
Interfaces controlled by on-chip controllers					
OSPI	1000	MIO[12:0]	Yes	8-bit	Octal SPI interface supports single and dual-stacked flash devices
QSPI24	0001	MIO[12:0]	Yes	1-bit, 2-bit, 4-bit (single or dual-stacked) 8-bit (dual-parallel)	Quad SPI interface supports the 24-bit (3-byte) flash addresses [1]
QSPI32	0010	MIO[12:0]	Yes	1-bit, 2-bit, 4-bit (single or dual-stacked) 8-bit (dual-parallel)	Quad SPI interface supports the 32-bit (4-byte) flash addresses. 32-bit flash addressing is required to address flash devices that are greater than 128 Mb. [1]
eMMC1 (4.51)	0110	MIO[12:3,0]	Yes	1-bit, 4-bit, 8-bit	eMMC interface supports eMMC 4.51 at 1.8V
SD0 (3.0)	0011	MIO[49:37]	Yes	4-bit	SD interface supports SD 3.0 with a required SD 3.0 compliant external level shifter
SD1 (2.0)	0101	MIO[51:50,33:28, 26]	Yes	4-bit	SD interface supports SD 2.0
SD1 (3.0)	1110	MIO[51:50, 36:26]	Yes	4-bit	SD interface supports SD 3.0 with a required SD 3.0 compliant external level shifter

Notes:

1. For Quad SPI single flash or dual-stacked flash setups, only a subset of the MIO interface pins listed are required and the MIO interface pins can be used for other peripherals. See the boot interface diagrams for more information.

Versal Boot Memory Addressing Limits

Jvsq >$Ziwwep$EGET$W}wxiq $Wsjx{ evi$Hizipstiww$Kymhi$YK5748-

Table: Boot Mode Search Limit

Boot Mode	Search Offset Limit
OSPI (single, dual-stacked)	8 Gb
QSPI24 (dual-parallel)	256 Mb
QSPI24 (single, dual-stacked)	128 Mb
QSPI32 (dual-parallel)	8 Gb
QSPI32 (single, dual-stacked)	4 Gb
SD0 (3.0), SD1 (2.0), SD1 (3.0), or eMMC1	8191 FAT files (default)
eMMC1 (raw)	eMMC device size

Note: When using OSPI or QSPI dual-stacked mode, the BootROM ca ly access the lower QSPI or OSPI addressable flash memory space for boot. After boot, the PLM can access the upper QSPI or OSPI additional image storage.

Space-Grade Hig Performance Dual-Quad Serial Pe istent SRAM Memory

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Features

- Interface
  - Dual Quad SPI – su 8-bit wide transfer
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- Technology
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    - Data Endura ce: 10^{16} write cycles
    - 20 years @ 85°C
- Density
  - 1Gb, 2Gb, 4Gb, 8Gb
- Operating Voltage Range
  - V_{CC}: 2.70V – 3.60V
  - V_{CCIO}: 1.8V, 2.5V, 3.0V, 3.3V ***
  - V_{DD}: 1.00V ****
- Operating Temperature Range
  - Industrial Extended: -40°C to 125°C
- Packages
  - 96-ball FBGA (20mm x 20mm)
- Data Protection
  - Hardware Based
    - Write Protect Pin (WP#)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect [2:0])
- Identification
  - 64-bit Unique ID
  - 64-bit User Programmable Serial Number
- Supports JEDEC Reset
- 48-hour burn-in at 125°C
- RoHS & REACH Compliant *
- PEMS-INST-001 Flow **

Programming the MRAM

- Avalanche MRAM (P-SRAM) is modeled after an SRAM that is Non-Volatile
  - Block erases, wear-leveling, wait-states aren't required + robust ECC built-in
  - Simply write to the locations that need to be updated
- **Lab/Clean Room:** After solder-reflow/assembly the MRAM can be programmed by:
  - Standard U-Boot Protocol (i.e. - upload to DRAM, blast to QSPI)
  - (Direct) programmed using a JTAG-like adapter
    - ~10 minutes to program 8Gb

  - (Indirect) programming method by loading bootstrap via (Direct) and reboot to small Versal firmware to provide higher speed upload of 8Gb
    - ~40 seconds to program 8Gb
- **In-System/On-Orbit Programming:**
  - Standard in-system firmware updates per System Policies
    - ~40 seconds to program 8Gb

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Demo Today

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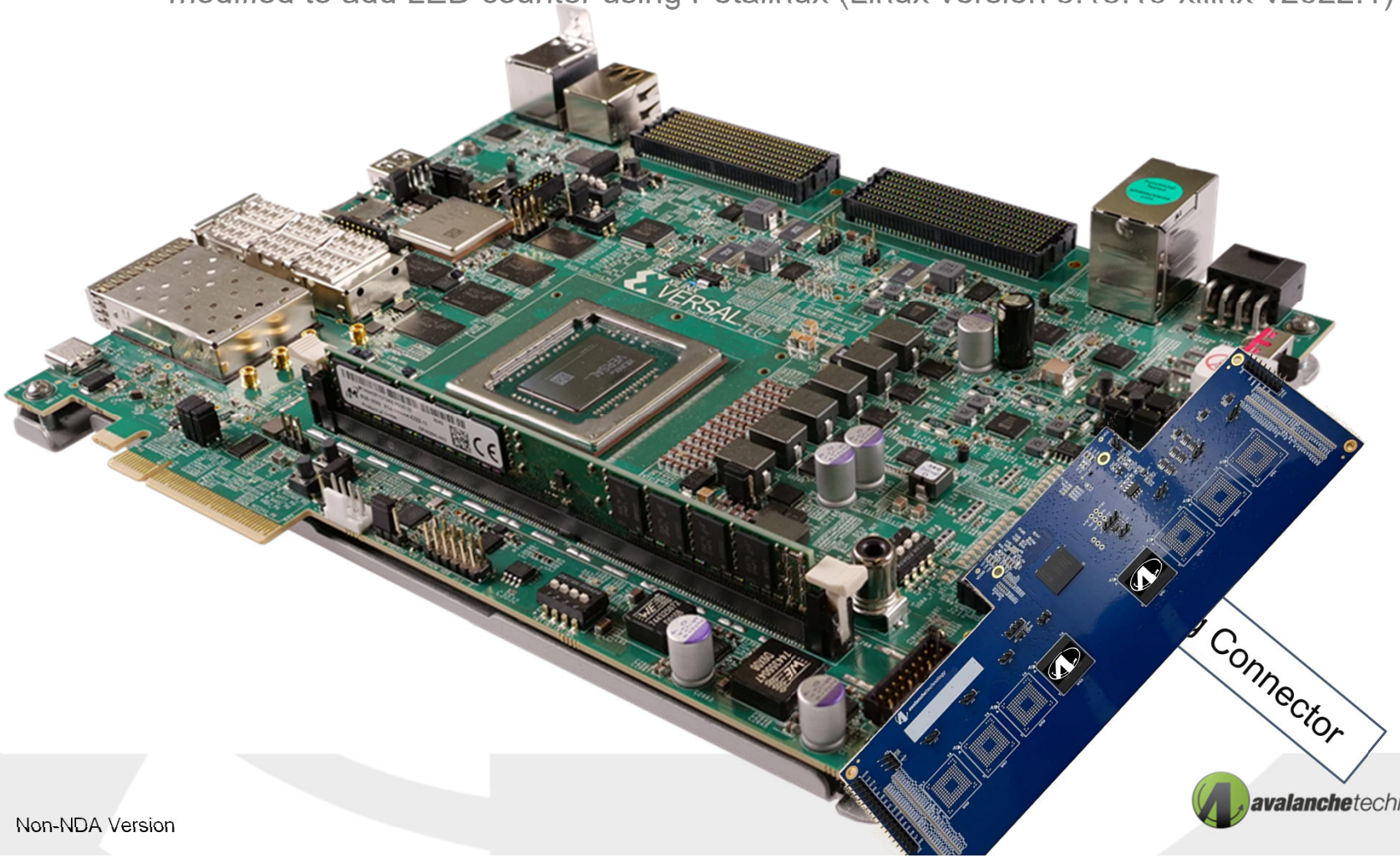
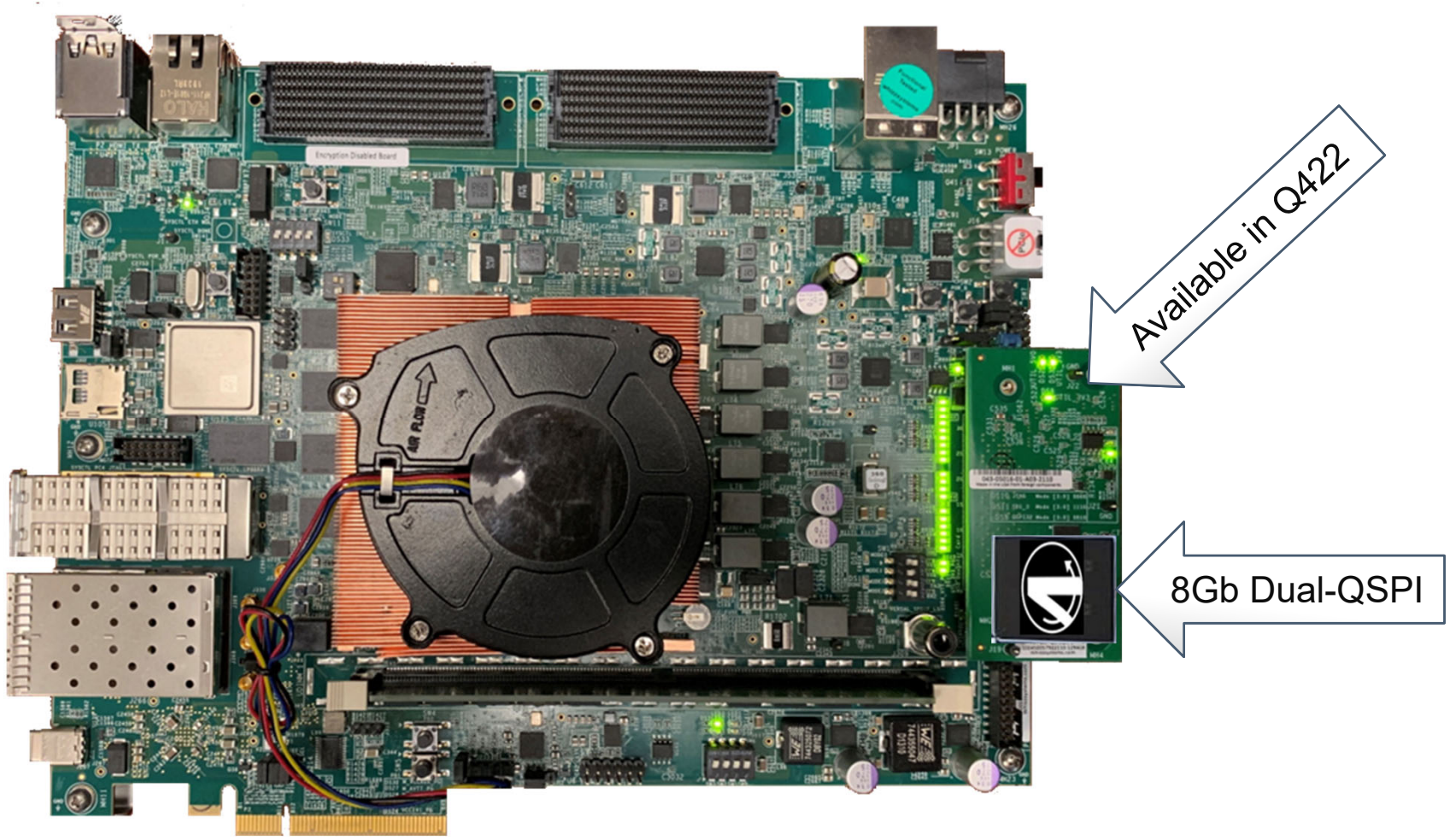
Demo of VCK190

- U-Boot Programming of MRAM using Dual-QSPI emulator
- Application is “GPIO Demo” from *Versal ACAP Embedded Design Tutorials*
    - modified to add LED counter using Petalinux (Linux version 5.15.19-xilinx-v2022.1)



Avalanche Boot Module supporting Alpha-Data[1] & VCK190



[1] – New Alpha-Data card may require interposer board

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Summary

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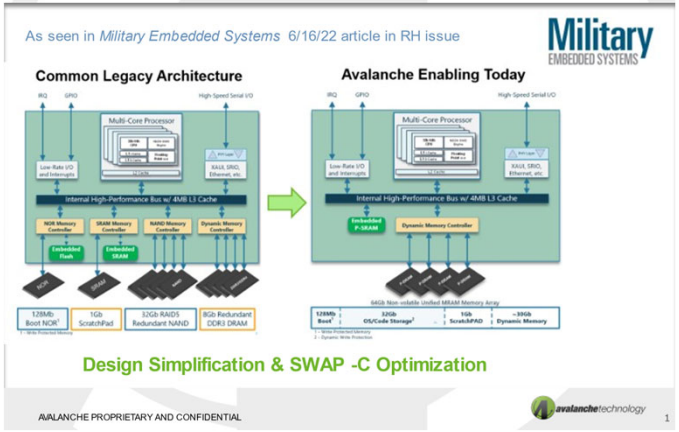
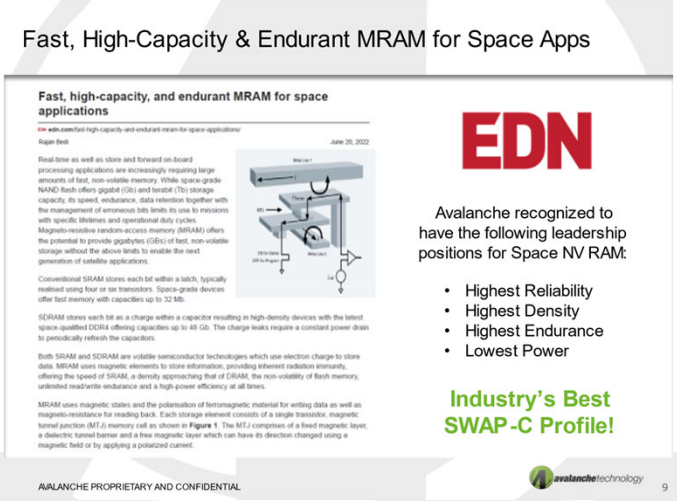
Important Program & Industry Validation

Industry Articles

Enabling Next-Gen Space IoT with Unified Memory Architecture



Fast, High-Capacity & Endurant MRAM for Space Apps



Unsolicited Customer Feedback

"Avalanche has maybe one of the coolest parts of the year, a finally-good-density MRAM that is inherently rad-tolerant and seems tailor-made for booting Versal devices."

Tech Fellow – Defense Prime

"For years I tried to fly other company's power-point slide decks, but I've failed. Avalanche is unique in this industry as they are delivering products and their promises."

CEO of Defense Prime

"Avalanche's 8GB QSPI device has the potential to address Xilinx's current gap of multiple configuration images, OS image storage as well as run-time flash memory. I highly endorse Avalanche Technology's efforts and their enthusiasm to provide a validated solution."

Space Architect, FPGA Vendor

"You guys nailed it. We could not do what we need to without this device."

HW Engineer, Defense Prime

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Newsletter – released on 6/9

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June 2022 Updates

Highlights

Tired of supply chain issues with extended lead times and increased pricing on industrial Non-Volatile RAM (FRAM, BBSRAM, MRAM)? Avalanche Technology has a broad production offering of Industrial MRAM solutions from 1Mb to 64Mb in serial and parallel interfaces, pin for pin compatible with many in the industry, and our distribution partner, Mouser, has most options in stock or up to 6-weeks in lead time. Please reach out to us if you need assistance in cross referencing these devices at info@avalanche-technology.com.

Third Generation Space Grade STT-MRAM now sampling! Breaking barriers in density, reliability and endurance, these devices are driving a paradigm shift in architectural use cases and SWAP-C optimization, particularly for Space applications. From 1Gb to 8Gb parallel and dual Quad SPI interfaces available this summer to 16Gb DDR3 by year end, this non-volatile memory offering is blurring the lines with traditional storage technologies, increasingly used to boot advanced processors, FPGA's & even real time operating systems in addition to working memory and L4 cache.

Rad Tolerant SoC family announced for LEO system monitoring and configuration applications. Continuing to drive innovation and enable SWAP-C optimized access to Space, Avalanche will be rolling out a family of flexible SoC's targeted at the increasing IoT needs for satellite constellations, offering time to market advantages through re-use. Additional information can be found here.

Update Notifications for Technical Documentation - To ensure our customers are kept up to date with refreshed and new technical support material, we are maintaining a contact database for those who wish to receive proactive updates about datasheet revisions. You can respond to this newsletter or let us know at any time that you would like to be included. Also, when requesting datasheet downloads from our website going forward, you will receive a prompt for optional inclusion to this notification list.

READ MORE INSIGHTS

Whitepapers

Powering Aerospace and Defense - Learn why MRAM has a clear advantage in Aerospace and Defense applications. Besides being radiation tolerant, MRAM boasts unlimited endurance and handles extreme temperatures, ensuring data retention.

Powering the Industrial Internet of Things - Learn about the transformation of Industrial IoT, where decision making is rapidly moving from the cloud to the nodes, unlocking the potential to increase efficiency exponentially.

Product Status & Datasheets

Discrete MRAM

- **Gen 3 Space Grade (in pre-production):**
  - High density (1Gb+), 22nm process, SWAP-C optimized
  - High Endurance (10^{35}), Embedded ECC, Low Power (10mA/1Gb), High Retention (1,000 years @ 85degC), No Shielding Required
  - Radiation Test Report available upon request & NDA
  - Parallel x 32 Datasheet – Rev U
  - Serial Dual-Quad SPI Datasheet – Rev B
- **Gen 2 Space Grade & Industrial Grade (in production):**
  - Densities of 1Mb to 64Mb, 40nm process, Low Leadtimes
  - High Endurance, High Performance (35ns), Low Power, Embedded ECC
  - Industrial Grade:
    - Serial Ultra Low Power Datasheet - Rev L
    - Serial High-Performance Datasheet - Rev P
    - Serial SPI Datasheet - Rev F
  - Space Grade:
    - Radiation Test Report available online, no shielding required
    - Serial Space Grade Datasheet - Rev P
    - Parallel x8 Datasheet - Rev T
    - Parallel x16 Datasheet - Rev T
    - Parallel x16 Space Grade Datasheet - Rev U
- **Embedded MRAM:**
  - **eMRAM (8 to 64Mb):**
    - eMRAM Datasheet - Rev C
  - **eSRAM (8 to 64Mb):**
    - eSRAM Datasheet - Rev A

Application Notes & additional documentation available on our website.

New IBIS & Verilog Models

IBIS Model updates for our Space Grade Serial products (Dual Quad SPI support added) can be found here.

Application Notes & Additional Documentation available on our website.

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Recap: Avalanche P-SRAM Advantages Space

- Inherently Radiation Tolerant Non-Volatile memory
- **Highest Data Endurance (10^{16})** of any space MRAM
- **Highest Density (bit per mm^2)** of any space MRAM
- **Lowest Power Consumption (10mA/Gb)** of any space MRAM
- **Lowest Total Cost of Ownership** for space NVM
- **Highest Retention** of any space MRAM (1,000 years @ 85degC)
- **Unified Memory Support** – boot FPGA, RTOS, working mem, storage
- **No Shielding Required** vs those with space heritage
- **TMR Techniques** employed for SEE mitigation
- Multiple interface options – Parallel, Serial, DDR3
- Flight Heritage in 2022!

Thank You

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